ALTAIR

DIGITAL POWER DESIGNER USER GUIDE

Altair Embed® 2025.2

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Use of Master and Slave in hardware-specific block descriptions

Embed and Embed Digital Power Designer support hardware devices that use the words master and slave to describe relationships in bus modes, communication protocols, and connections. We recognize that these words are inappropriate and offensive. We are evaluating how to change these words without introducing technical confusion.

Resources for learning Altair Embed / Digital Power Designer™

The following resources are available to help you become expert users:

- Interactive webinars
- Sample diagrams
- Training

Videos

The online Learning Center contains virtual instructor-led courses including courses for Altair Embed (search for "Embed" in the search bar to see all the currently available courses). A growing collection of videos that offer quick and easy ways to learn basic concepts in Embed and the Digital Power Designer. If you are a new Embed / Digital Power Designer user, a good video series to start with is: Buck Converter Design Series.

Sample diagrams

Your Embed / Digital Power Designer software includes a directory of fully documented sample diagrams which can be found. These diagrams are divided into sections similarly to the block set itself. The simulation section in the Digital Power examples is particularly extensive and groups the examples under converter and control characteristics and configurations as well as under groupings of the sub-categories in the simulation section of the block set. Additionally there are application examples and target specific examples under TI Developer's kits and STM32 developer's kits.

To access sample diagrams

- Click on **Examples → Digital Power**.

Training

Altair® offers training sessions for learning and gaining expertise in Embed/Digital Power Designer. Training sessions are conducted in Lowell, MA, as well as at customer sites and as online webinars.

Technical support

Altair technical support teams are expert Embed users and can provide assistance and advice for most problems you may encounter. Typically, technical support provides assistance in solving specific problems rather than providing training on how to use Embed / Digital Power Designer.

The table below indicates the support available for Embed / Digital Power Designer.

Support	How to access
Online forums	Click here to go to the online forums.
Email support	Send an email to embed-support@altair.com and include the following: • Briefly describe your issue • Attach the diagram in question • Specify the version of the software that you are using
Phone support	Click here to contact your local support office.

Blogs

Blogs are available at Altair Embed blogs Altair Embed blogs by selecting blog as the content type and may have content of interest to the user. New blogs will be continually added for different Embed topics.

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Disclaimer

The simulations, component values and eventually the code generated, as well as the overall functionality of the diagrams developed within the Embed / Digital Power Designer are indicative only and aimed to assist the power supply design engineer in the many phases of analog and digital power supply design.

The responsibility of selecting the correct parameters and component values is explicitly left with the power supply design engineer. The purpose of the Embed / Digital Power Designer is to provide the digital power design engineer, or user of the software, with a comprehensive tool to assist in the design and understanding of power supplies and other digital power applications.

Altair, their representatives and subcontractors take no responsibility for the selection of incorrect parameters and / or components due to calculations or simulations generated within Embed / Digital Power Designer, or for any damage or personal harm which may occur due to the selection of incorrect parameters and / or components.

At the time of testing this release of the Embed / Digital Power Designer, all calculations, based upon the given assumptions and limitations, were believed to be correct. However, it is the responsibility of the power supply design engineer to verify any calculations and simulations used in a design or as a teaching tool. Altair, its representatives and its subcontractors take no responsibility for any damage, in any form, which may occur due to incorrect calculations or incorrect reported outputs of the design suite, nor for any incorrect use of this software.

All detailed assumptions and/or limitations of this tool must be taken into account before applying any of the calculated values to a given design. These assumptions and limitations are outlined in the various readme blocks throughout the Embed / Digital Power Designer installed software under the digital power menu within the Embed environment. Although care has been taken to outline as many of the assumptions and limitations as possible, the assumptions listed are not guaranteed to be a complete list of assumptions and limitations. Correct performance must be verified independently on all hardware designed by the user or other hardware which relates to calculations performed within this software.

As is always best practise, all designs must be thoroughly tested on the destined hardware and verified for correct performance, in all expected life-cycle conditions, by the power supply design engineer.

Introduction

The Altair Embed / Digital Power Designer (in this user guide also denoted as DPD) is an add-on to the standard block set of Embed with application-specific blocks for analog and digital power applications. The various sections of Embed / Digital Power Designer can be used independently or together to form a powerful design suite package for digital power supply design and other digital power applications.

One can quickly navigate throughout this user guide by clicking on any contents item to jump to that block description or section. In many parts of the user guide, the hyperlink

Contents-section

can be found which will return the reader back to the chapter contents for further navigation or the hyperlink:

Main Contents

which will return the reader back to the main chapter contents.

Requirements for the Digital Power Designer

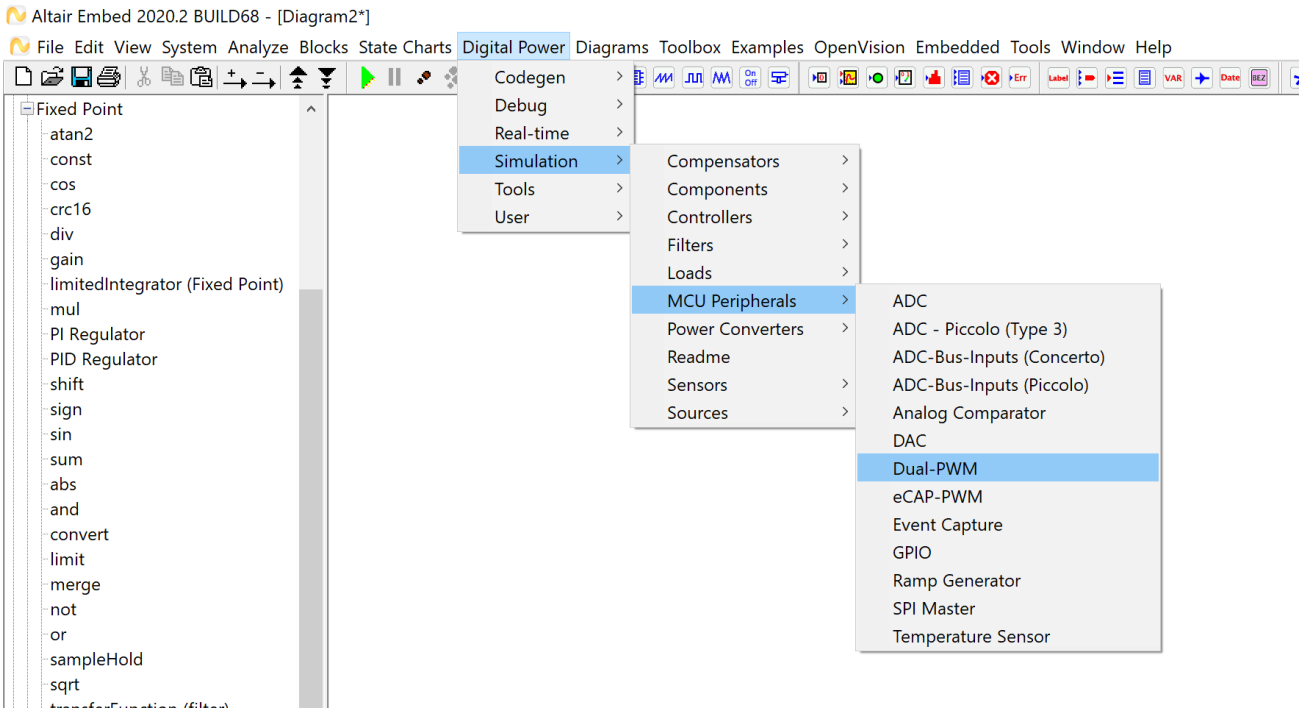
Altair Embed / Digital Power Designer is designed to function within the Embed environment. Therefore, it is important that you install Embed before you install Altair Embed / Digital Power Designer.

The block set runs as an add-on to Embed and therefore it is compatible with the same operating systems as Embed; refer to the Embed SE and Embed manuals for details.

Memory requirements are small and an additional 100MByte of hard disk space, on top of the Embed installation, will be sufficient for installation.

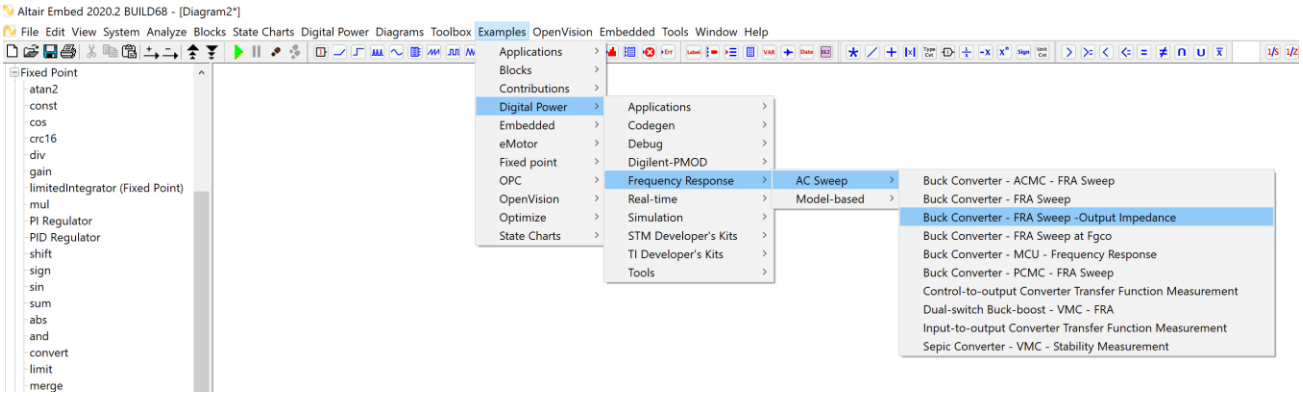
Installing the Digital Power Designer

Refer to the installation guide for installing the Embed / Digital Power Designer on top of an Altair Embed installation. It is recommended to install to the default directory within the Embed folder.



A “Digital Power” menu will be installed within the Altair Embed IDE and consists of high-level digital power application-specific blocks and many examples and tools to quickly come up to speed with the block set and with digital power design techniques.

The examples section will be installed under Examples → Digital Power.



Overview of Digital Power Applications

Digital power is ever more present in power supply design due to its many advantages and the readily available and powerful microcontrollers which these days have many integrated peripherals dedicated to digital power applications at an ever-reducing cost.

Microcontrollers or MCUs, integrate complex PWMs, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), fast comparators and other peripheral hardware integration dedicated to digital power applications. Much of the traditional hardware which was required to support MCUs such as supply voltage monitors, voltage regulators and oscillators have also been integrated within the MCU, decreasing further the cost, printed circuit board footprint and the hardware complexity of a given design.

A very good overview of digital power can be found in the document slup232 - "A Practical Introduction to Digital Power Supply Control" by Laszlo Balogh which can found at:

http://www.ti.com/lit/ml/slup232/slup232.pdf

The main advantage of digital power is the flexibility of the design. As soon as a hardware platform is developed, digital power can allow the implementation of that hardware to many varying applications or application areas. This can speed up the time to market for new products once a base hardware and software has been developed. An MCU can provide the integrated components and processing power necessary for the control loop and it can also provide communications capabilities for interfacing the power supply to the outside world (HMI), power supply monitoring and parallel current sharing communications can also be easily integrated with very little additional hardware. Digital power supplies can be simply integrated into a given system operating other equipment, via standard communication protocols.

Control parameters can be varied during the normal operation of a power supply; something that would be very difficult to implement in analog control. Digital control parameters can be optimized according to the current environmental conditions or due to the aging of analog / power components during the normal life cycle of a power supply. Once set, the parameters in digital control will remain constant and will not vary due to temperature variations or aging of components. Compared with analog control, a much larger range of effective component values is available to the designer by simply choosing numerical values within the software. Custom control algorithms can be flexibly applied using digital control.

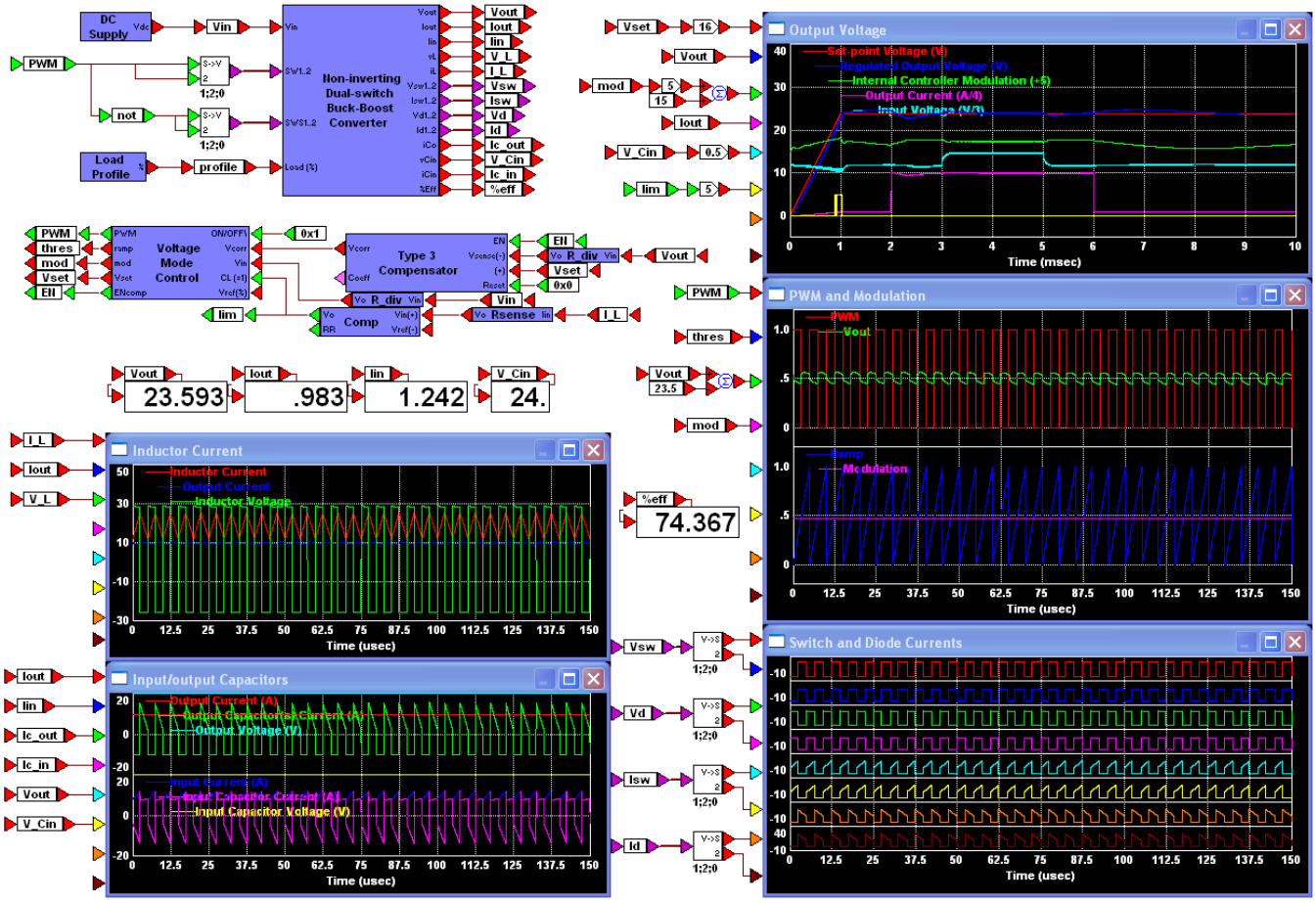
For the analog designer, the main obstacle to digital power applications is the initial complexity of the design and the difficulty of implementing control algorithms which require new techniques which the traditional analog designer is either not accustomed to or does not remember from their university days. The unfamiliarity with digital power design techniques is an issue which needs to be addressed for the continued growth of digital power.

Altair Embed/Digital Power Designer is aimed particularly at assisting the power supply designer with a purely analog background, to overcome this hurdle while at the same time offering many tools and dedicated blocks to aid the designer, either from a digital or analog background, in any type of power supply design.

Overview of the Digital Power Designer

The Altair Embed / Digital Power Designer is aimed to provide the power supply design engineer with a tool to design and develop power supplies and in particular digital power supplies. It is the intention to regularly upgrade this tool with more features and more add-ons to provide a complete power supply design solution.

There are several environments in Embed / Digital Power Designer including simulation, code-generation (Codegen), debugging and tools. The tools assist in the various design stages of designing digital power supplies, generally determining components and parameters by calculation. The simulation environment provides many ready-made blocks in order to quickly perform simulations of digital power supply applications. The code generation environment provides many blocks which can be connected together to form diagrams which can be automatically and effortlessly code-generated, linked and compiled for a MCU thanks to the built-in Embed code generation features. The debugging environment contains blocks to assist with the debugging of diagrams while running in the MCU in hardware together with target-interface diagrams for debugging purposes. The real-time environment includes blocks for faster simulations and real-time applications.



Application areas for Embed / Digital Power Designer include all types of power supply from low power (several Watts) to many Mega Watts . Some application

areas are power supply design, battery chargers and rectifiers, renewable energy, LED lighting, Uninterruptible power supplies (UPS), DC-DC converters, inverters, solar converters etc.

Digital Power Designer in Sections

Altair Embed/Digital Power Designer consists of many sections and several sections of blocks. The main block sections are:

- Codegen
- Debug
- Real Time
- Simulation
- Tools
- User

The codegen (code generation) section consists of blocks with the normal cyan colouring which have been optimized for downloading to an MCU to be used in digital power applications. These blocks can be used for code-generating to create downloadable diagrams and for simulation.

The simulation section consists of a large number of blocks aimed at simulating digital power supplies and power conversion systems. The blocks within this section consist of models of typical hardware components found in power supply design, blocks emulating the software function of digital power design or analog control design and hardware peripherals typically found internally in MCUs designed for digital power applications as well as many typical power converter configurations applied to the many application areas of power supply and power converter design.

The Real-time section consists of blocks coloured in blue which are optimized models for faster simulations and can be used together with the Analyze™ feature of Altair Embed to perform frequency domain analysis in addition to the tools within Embed DPD. The models are also slim-lined and optimised for code-generation and can be used in real-time simulations on appropriate real-time hardware.

The tools section consists of blocks designed to assist the power supply design engineer in the various aspects of digital power supply design including assistance in the conversion from analog to digital power supply control techniques, measurements and frequency domain analysis.

The debug section consists of blocks in the normal cyan colouring which can be code-generated and use in user diagrams for debugging purposes. This section also consists of blocks in a pink colouring which are generally intended to be used in target-interface diagrams, interfacing with diagrams running on hardware containing the code-generable debugging blocks.

The user section provides a repository for user diagrams and blocks which can be easily accessed from the Digital Power menu.

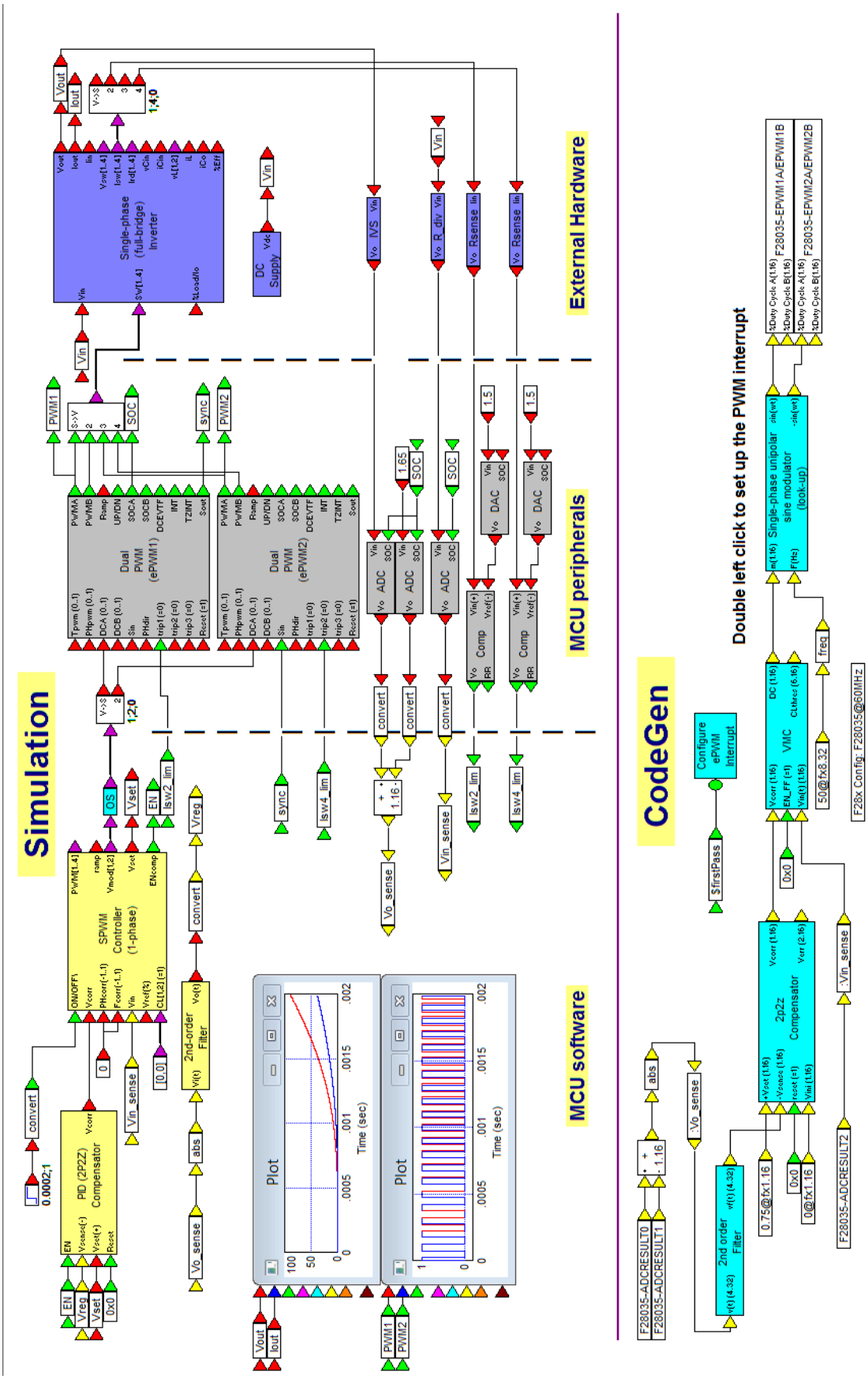
The following figure outlines visually the various sections of the block set with MCU software emulating blocks in yellow, internal MCU peripheral blocks in grey,

external components and hardware emulating blocks in signal blue, code-generable blocks in cyan (which can also be used in simulation) and the tools blocks in orange.

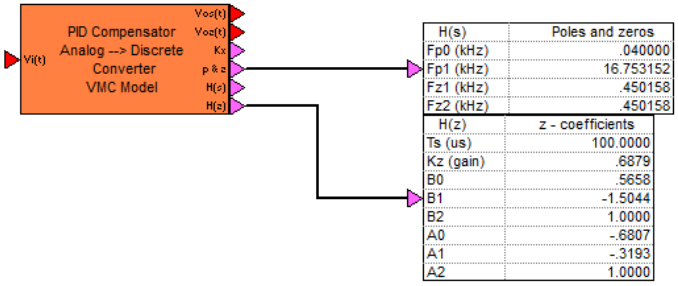
Whereas the cyan code-generable blocks can be used in simulation, they can only be used for digital control simulations with definite and precise functions in order to preserve their optimized code-generable characteristics. The simulation blocks can be used in initial simulations for more flexibility in the initial design by experimenting with various options, trying different control techniques and simulating at a faster rate using initially an analog control loop.

The following chapters outline the many of the blocks included within the block set along with their features and function for each of these five sections.

The various sections of the Digital Power Block Set are outlined in the following diagram:



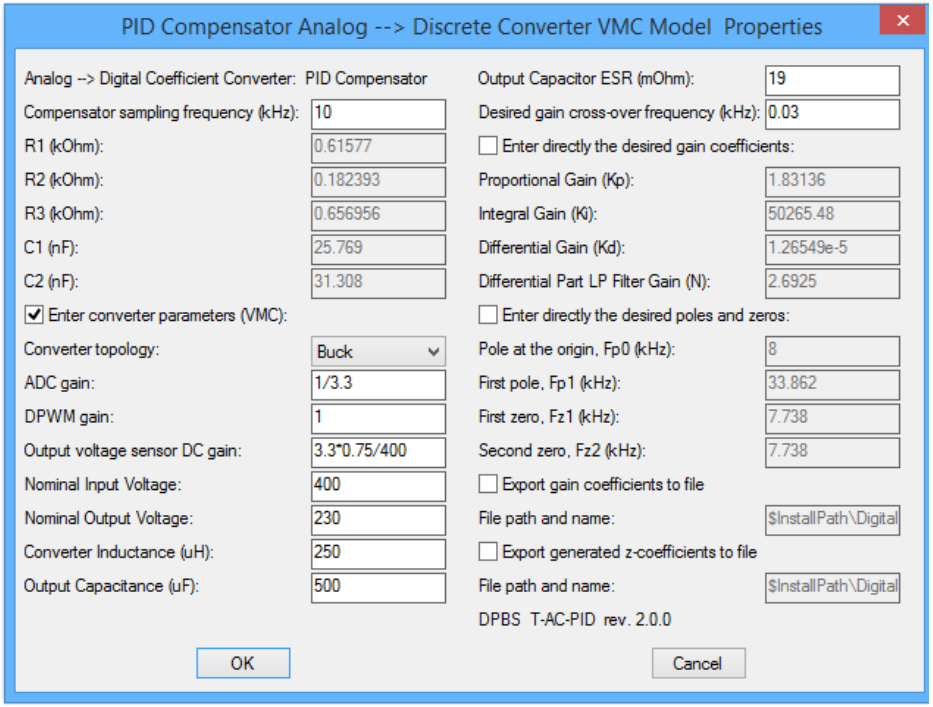
Tools - Compensator Coefficients

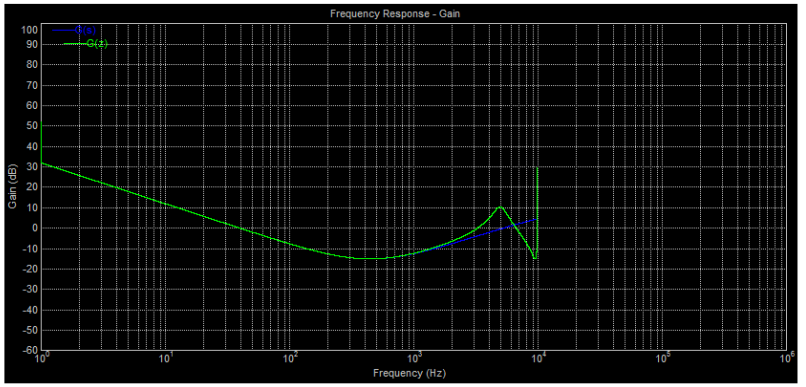


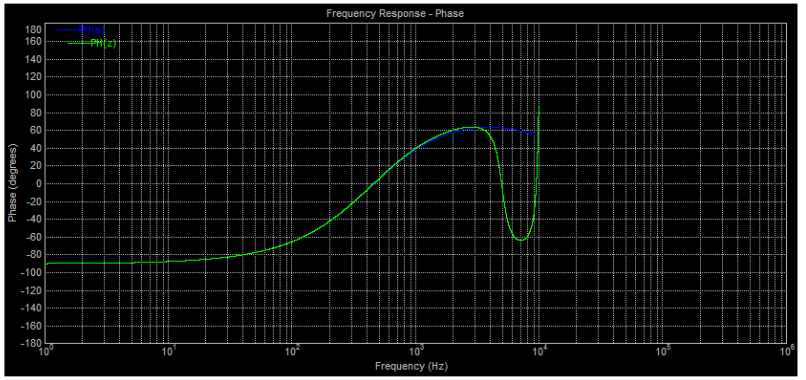
H(s)	Poles and zeros
Fp0 (kHz)	.040000
Fp1 (kHz)	16.753152
Fz1 (kHz)	.450158
Fz2 (kHz)	.450158

H(z)	z - coefficients
Ts (us)	100.0000
Kz (gain)	.6879
B0	.5658
B1	-1.5044
B2	1.0000
A0	-.6807
A1	-.3193
A2	1.0000

PID (2p2z) Compensator

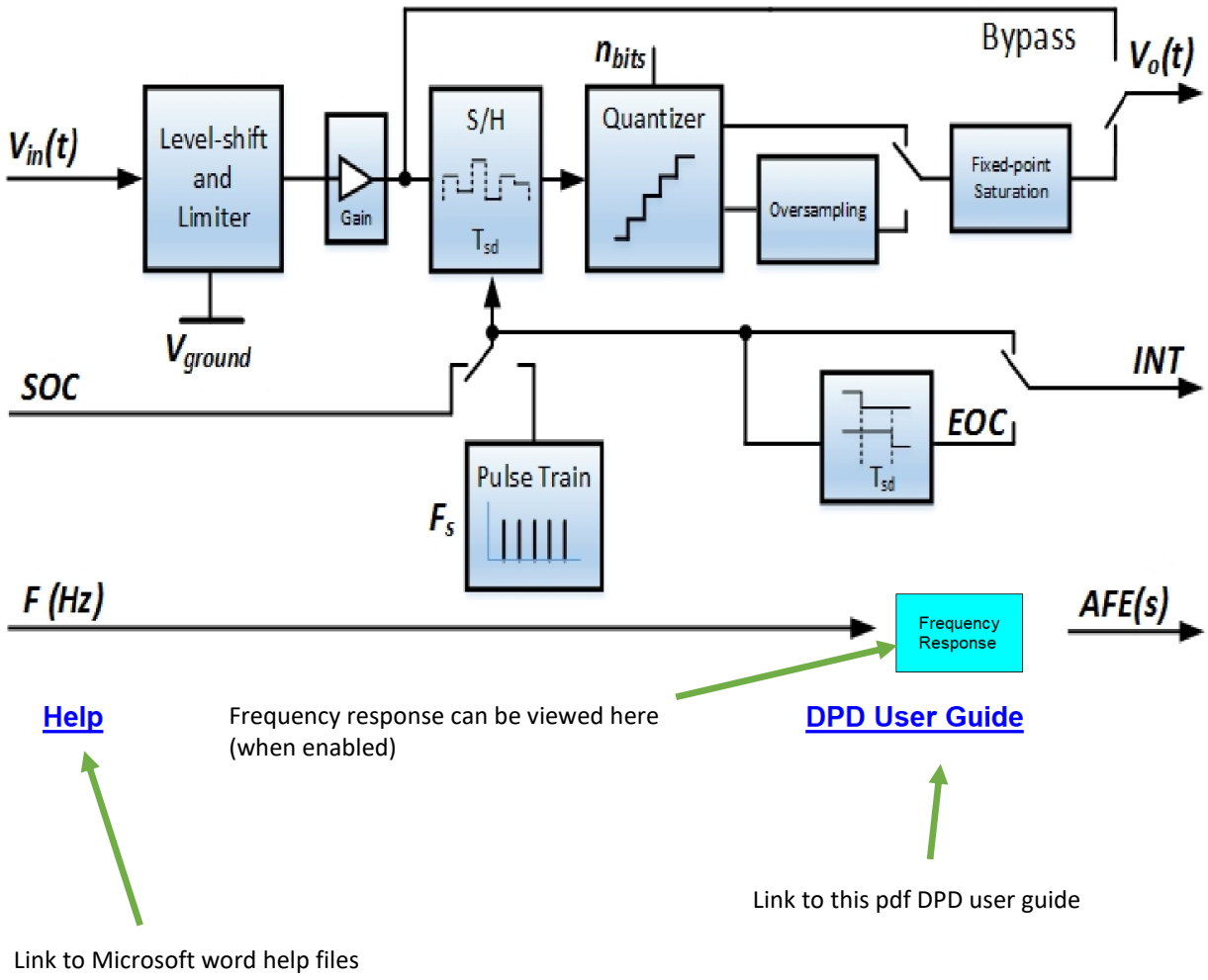






Digital Power Designer Help

Many of the blocks now contain links to Microsoft word-based help files and also a direct link to this DPD user guide. The links are accessible by double right-clicking on the blocks:



What's New in Altair Embed DPD

What's New in version 2022.2

GENERAL:

- Support for complex compensators

CODEGEN:

- No changes.

DEBUG:

- No changes

REAL-TIME

- No changes.

SIMULATION:

- Added support for complex (resonant) poles and zeros in the 2p2z and 3p3z compensators.
- Added a PR (proportional + resonant) compensator

TOOLS:

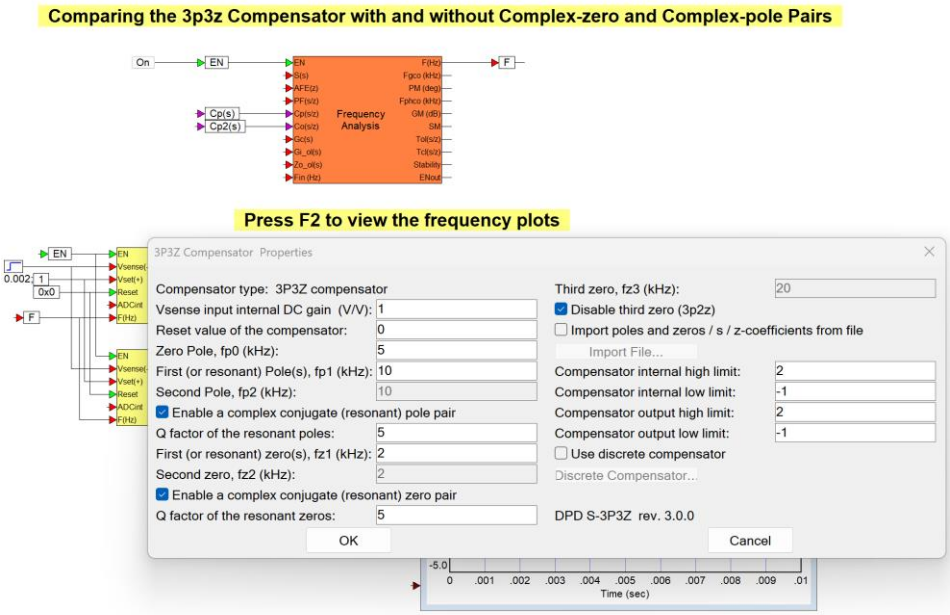
- Added a warning to the PID analog conversion tool in the case of complex zeros.

EXAMPLES:

- Updated the TI BMS examples under Applications.
- Added examples on compensators with complex poles and zeros.

DOCUMENTATION:

- Separated the BMS applications from the User Guide into a separate file and added a Bill of Materials for the battery board.



What's New in version 2022.1

GENERAL:

- General improvements for Altair Embed 2022.1 compatibility in 32-bit and 64-bit versions.

CODEGEN:

- Added code-generable blocks for oversampling.
- Added a cell balancing controller

DEBUG:

- Added code-generable and debug blocks for ADC.

REAL-TIME

- No changes.

SIMULATION:

- Corrected an error in the frequency response of the Resistor divider (voltage sensor) block (Rdiv).
- Corrected the frequency response of the sense resistor (Rsense) block.
- Added a new battery model using look-up tables
- Added a new battery model using polynomial fit equations
- Added a cell balancer model
- Added a wind turbine model
- Added squirrel-cage induction generator (SCIG) models
- Added a current-limited voltage source
- Added a voltage-limited current source
- Corrected the frequency response of the compensators with delay

TOOLS:

- Optimized the frequency response analyzer block (FRA) block and included an option to externally input the frequency for the internal signal generator.
- Optimized the model-based frequency response block and included an option to externally input the frequency to cascade blocks.

EXAMPLES:

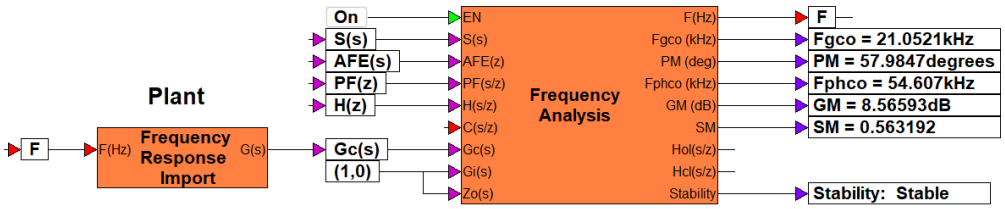
- Updated many examples with the updated blocks and features.
- Additional FRA examples.
- Added compensator design examples
- Added wind turbine examples
- Added SCIG examples
- Added new battery model examples
- Updated and added examples on battery management systems (BMS) including the TI bq76PL455 chip and the Infineon TLE9012 chip.
- Added examples for co-simulation with Altair PSIM® and for the FMU import (64-bit version only).

Compensator Design:

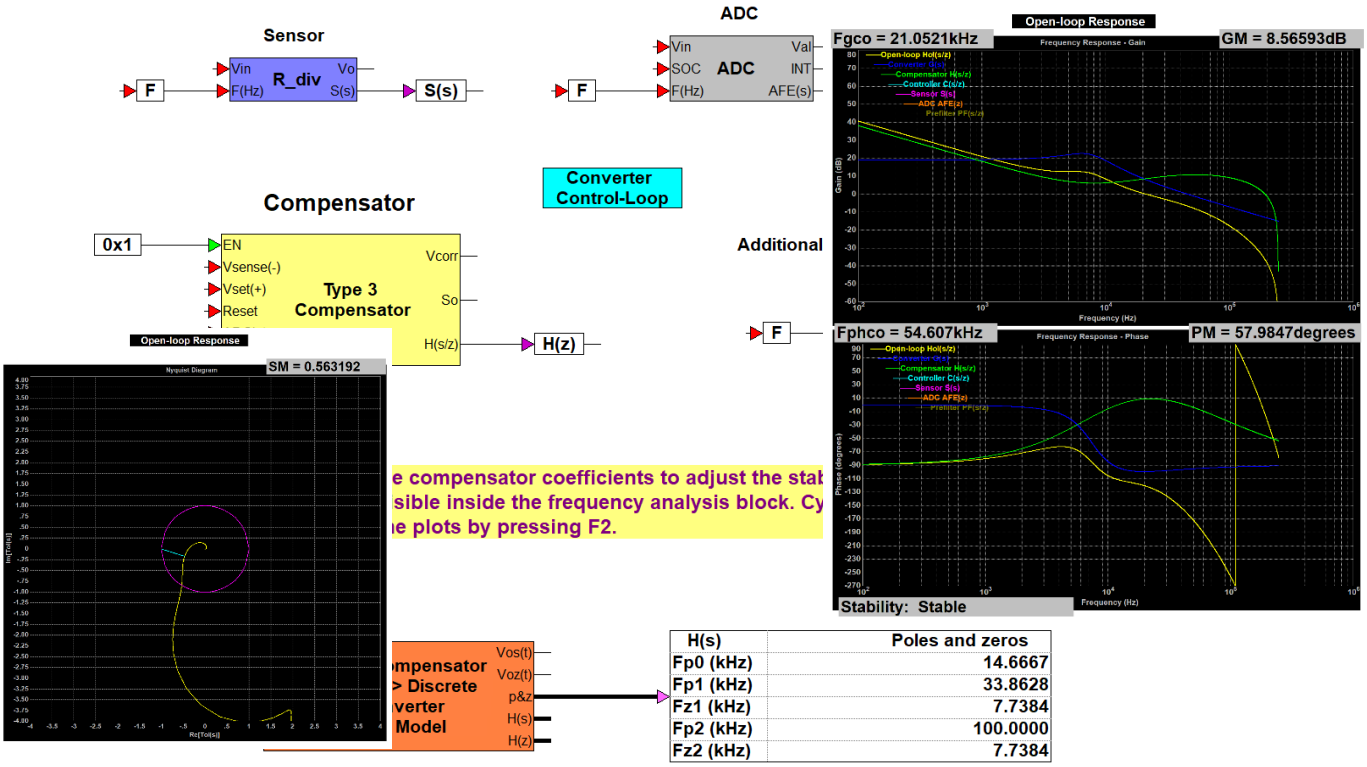
- Updated and added examples for compensator design.

Compensator Design - VMC

Compensator is digital, considers digital delays, ADC sampling delays etc in the loop.



The plant file was created using the diagram at:
Examples --> Digital Power --> Frequency Response --> AC Sweep --> Control-to-Output Converter Transfer Function Measurement

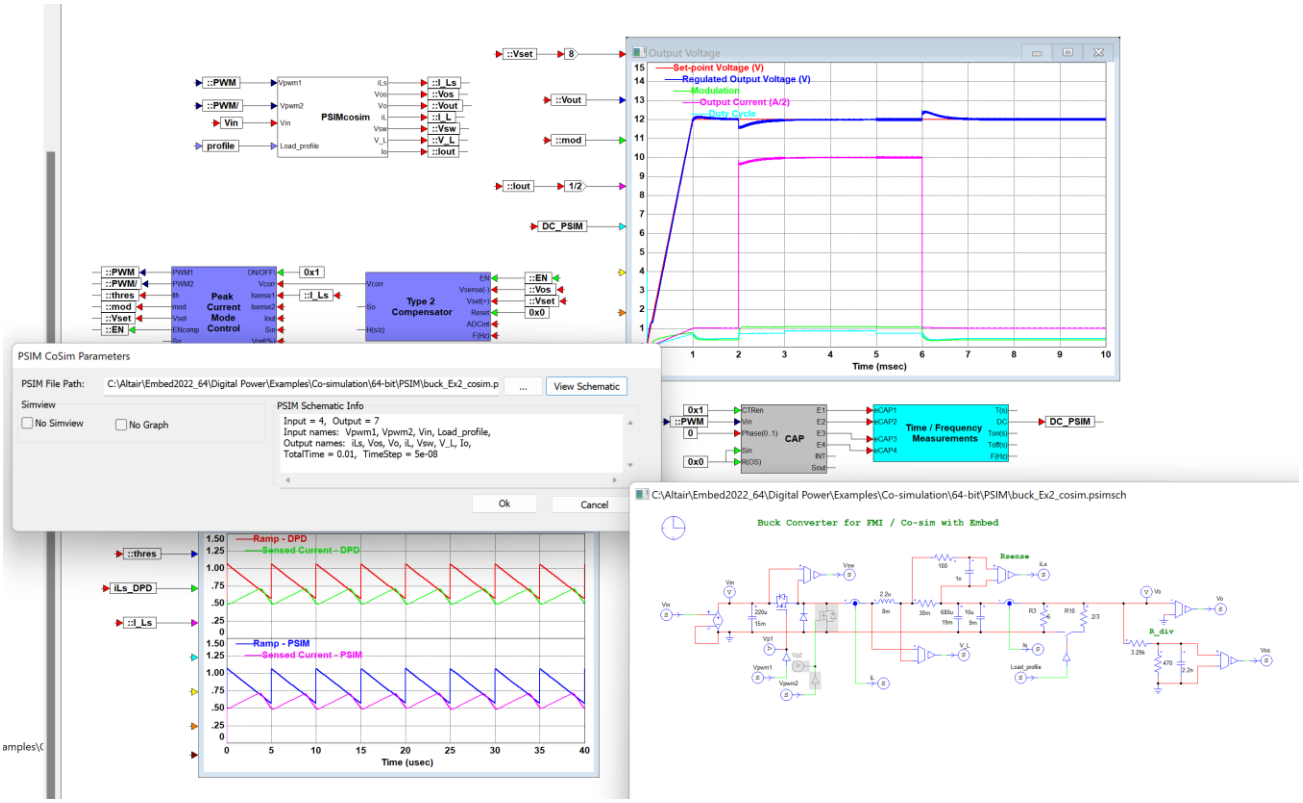


H(s)	Poles and zeros
Fp0 (kHz)	14.6667
Fp1 (kHz)	33.8628
Fz1 (kHz)	7.7384
Fp2 (kHz)	100.0000
Fz2 (kHz)	7.7384

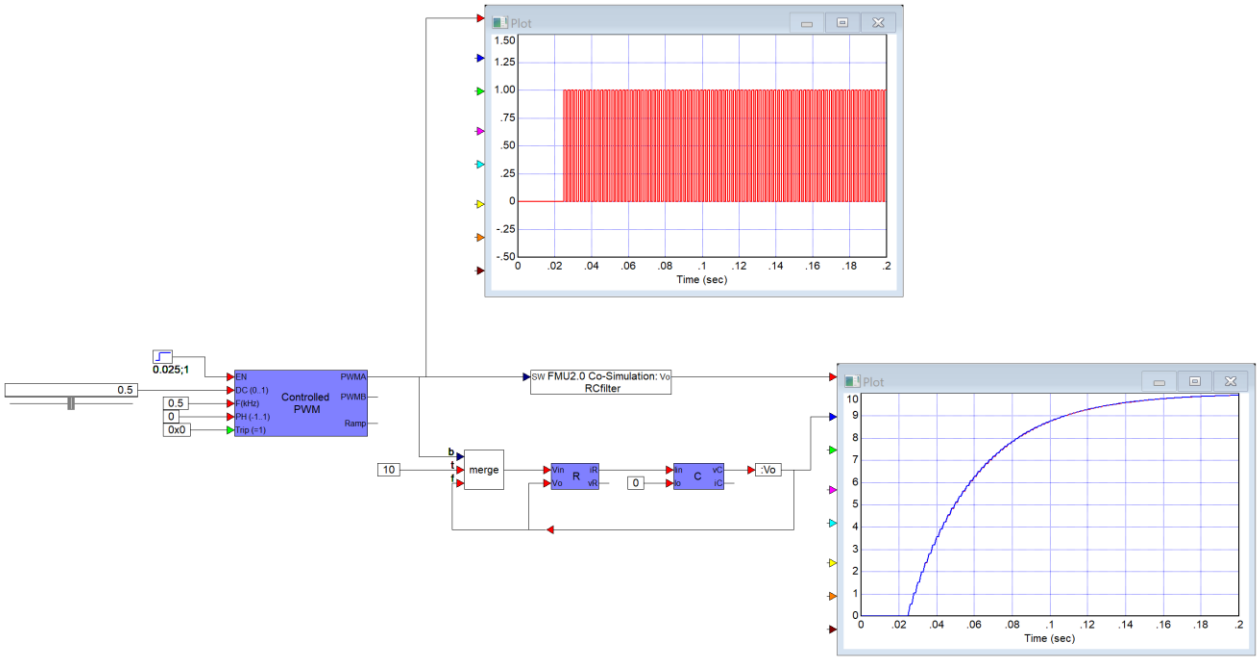
Co-simulation:

- Added examples of co-simulation with Altair PSIM® and using the FMU import (64-bit version only).

Direct co-simulation with PSIM:



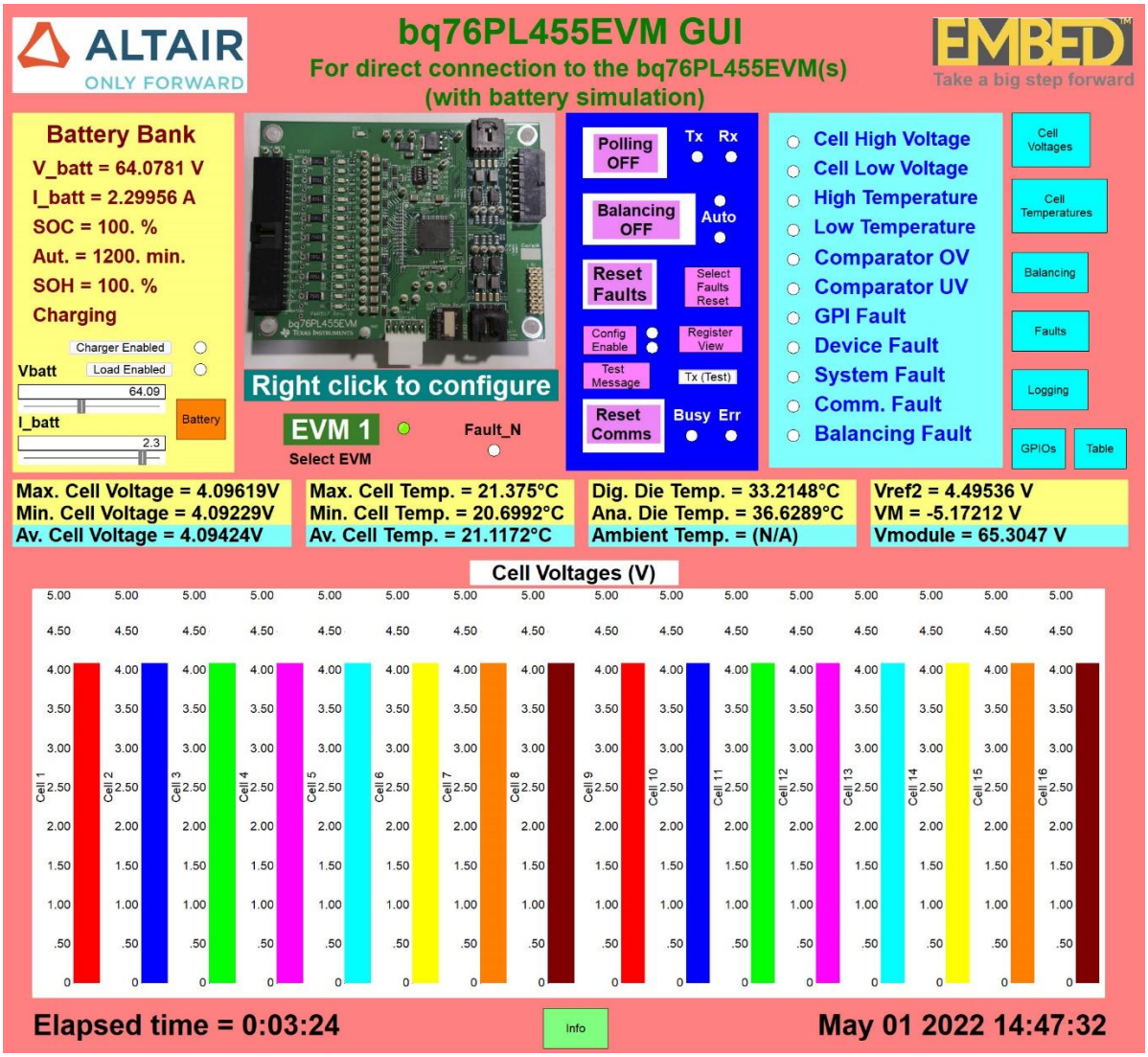
Co-simulation using the generated FMU:



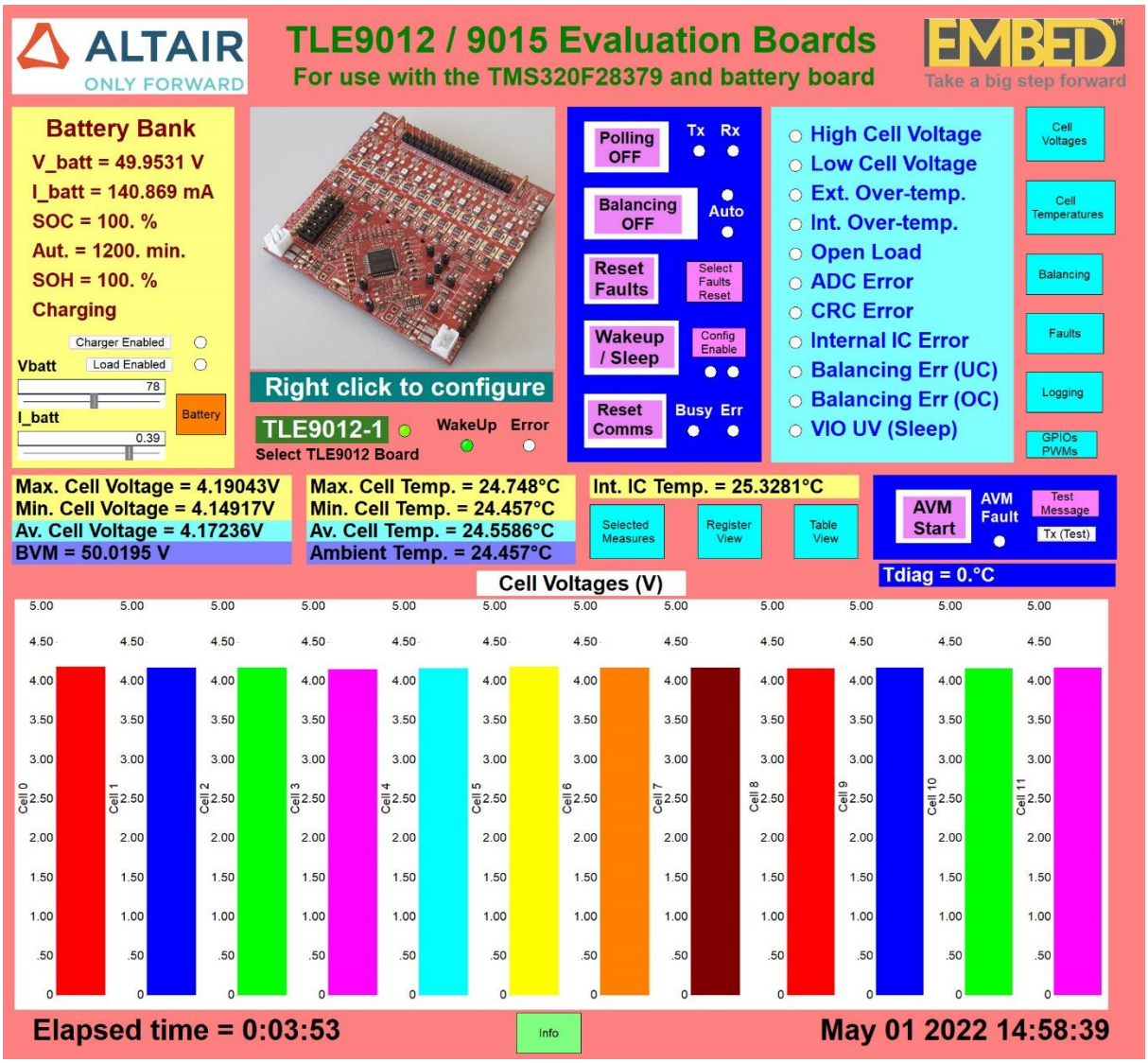
BMS Systems:

- Added a new section of this user guide on “Applications”, specifically for BMS systems.
- Added examples for the TI bq76PL455EVM evaluation module
- Added examples for the Infineon TLE9012 evaluation board.

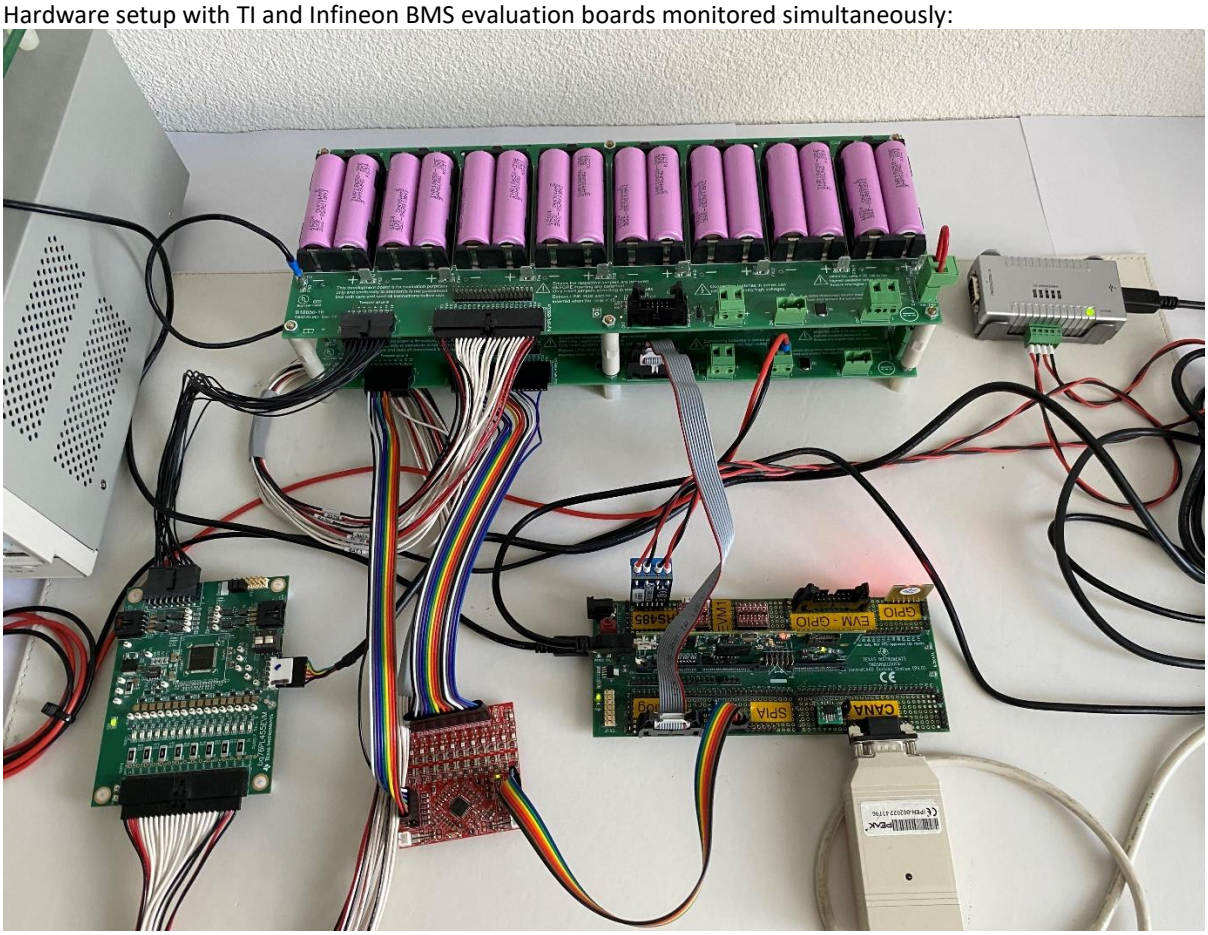
Texas Instruments BMS GUI:



Infineon BMS GUI:



Hardware setup with TI and Infineon BMS evaluation boards monitored simultaneously:



What's New in version 2021

GENERAL:

- General improvements for Altair Embed 2021 compatibility.

CODEGEN:

- Added code-generable blocks for further ePWM configuration.
- Added code-generable blocks for further ADC configuration.
- Added blocks for ADC oversampling.
- Made a correction to the ePWM interrupt config block and added the type 4/5 ePWM interrupt config.

DEBUG:

- Added debug blocks for the C2000 ePWM Type 4/5 and CMPSS.
- Added code-generable blocks for debugging
- Updated the ePWM register blocks in codegen and included blocks for each submodule.
- Added ADC and CMPSS debug registers.

- Corrected bit allocations in the ePWM (Type 1) counter-compare / Action Qualifier and Trip-zone target diagram decoders.

REAL-TIME

- Added more real-time examples.

SIMULATION:

- Corrected an error in the Sinusoidal PWM generator block (single phase).

TOOLS:

- Improved the internal display of the plots for the model-based frequency response and FRA blocks.
- Simulation speed of the model-based frequency response and FRA blocks increased.

EXAMPLES:

- Updated some examples with the updated blocks and features.
- Some of the FRA examples run faster.
- Added examples on real-time.
- Added examples on debugging with the new debug blocks.
- Added examples on debugging of converter controllers.
- General improvements to some of the simulation examples.
- Added examples on BMS systems

What's New in version 2020

GENERAL:

- General improvements for Altair Embed 2020 compatibility.

What's New in version 2019.2

GENERAL:

- General improvements for Altair Embed 2019.2 compatibility.
- Introduced a new dialog for importing and exporting files.
- Included links internally in many blocks to Microsoft Word based help files and to this DPD pdf user guide.
- Added model-based frequency response support to many blocks.
- The delays in digital control diagrams can now be handled using a sampling clock or ADC interrupts to sample and sequence the delays. An estimated calculation delay in digital control for each block can now be selected.
- Upgraded simulation blocks to work concurrently with the embedded sim blocks from the core embed environment.
- Improved support for the F28004x devices.
- Added some examples for STM32.

CODEGEN:

- Added blocks to reconfigure the C2000 ADC and SPI peripherals based upon the output files generated from the new MCU peripheral emulators in the simulation section.
- Added new PWM configuration blocks including HRPWM config, full Dead-band config, compare C/D writes and reads, PWM synchronisation chain config and ADC SOC output selection config.
- Added support for the ADC Post Processing Blocks (PPB) with configuration and writing and reading of the registers.
- Upgraded some of the peripherals config blocks for F28004x support.

DEBUG:

- Added debug blocks for the C2000 ADCs.
- Added more ePWM debug blocks.
- Added debug blocks for the SPI and i2c interfaces.

REAL-TIME

- No changes.

SIMULATION:

- Upgraded all of the compensators with improved internal integrators, with internal integral limits as well as the external limits, improved handling of

delays for discrete compensators, compatibility with the model-based frequency response blocks and internal visualization of the frequency response, improved the coefficient file importing, improved the error reporting and reorganized the dialogs.
- Upgraded all of the controller blocks for compatibility with the model-based frequency response blocks and internal visualization of the frequency response, added the option to use a defined ramp amplitude on those controllers which use an internal ramp, improved handling of delays for discrete controllers, improved the error reporting and reorganized the dialogs.
- Added model-based frequency response capability on many other blocks including sensors and filters.
- Added models for all common thermocouples and RTD temperature sensors under sensors.
- Added some active components in the components section. Some models previously in the sensor section have now been upgraded and place in the components section.
- Added a Piccolo ADC (C2000 Type 3) emulator under MCU peripherals.
- Added a C2000 SPI Master emulator under MCU peripherals.
- Improved the MCU temperature sensor model and based the input on the package power dissipation and the temperature is now also calculated based upon the device and package type.
- Upgraded the generic DAC model for frequency response and general improvements.
- Corrected an error in the ADC generic model.
- Upgraded the ADC, GPIO and Dual PWM blocks to work together with the embedded sim blocks.
- Corrected an error with the Zero Current Transition Controller.
- Included links to help files on many blocks.

TOOLS:

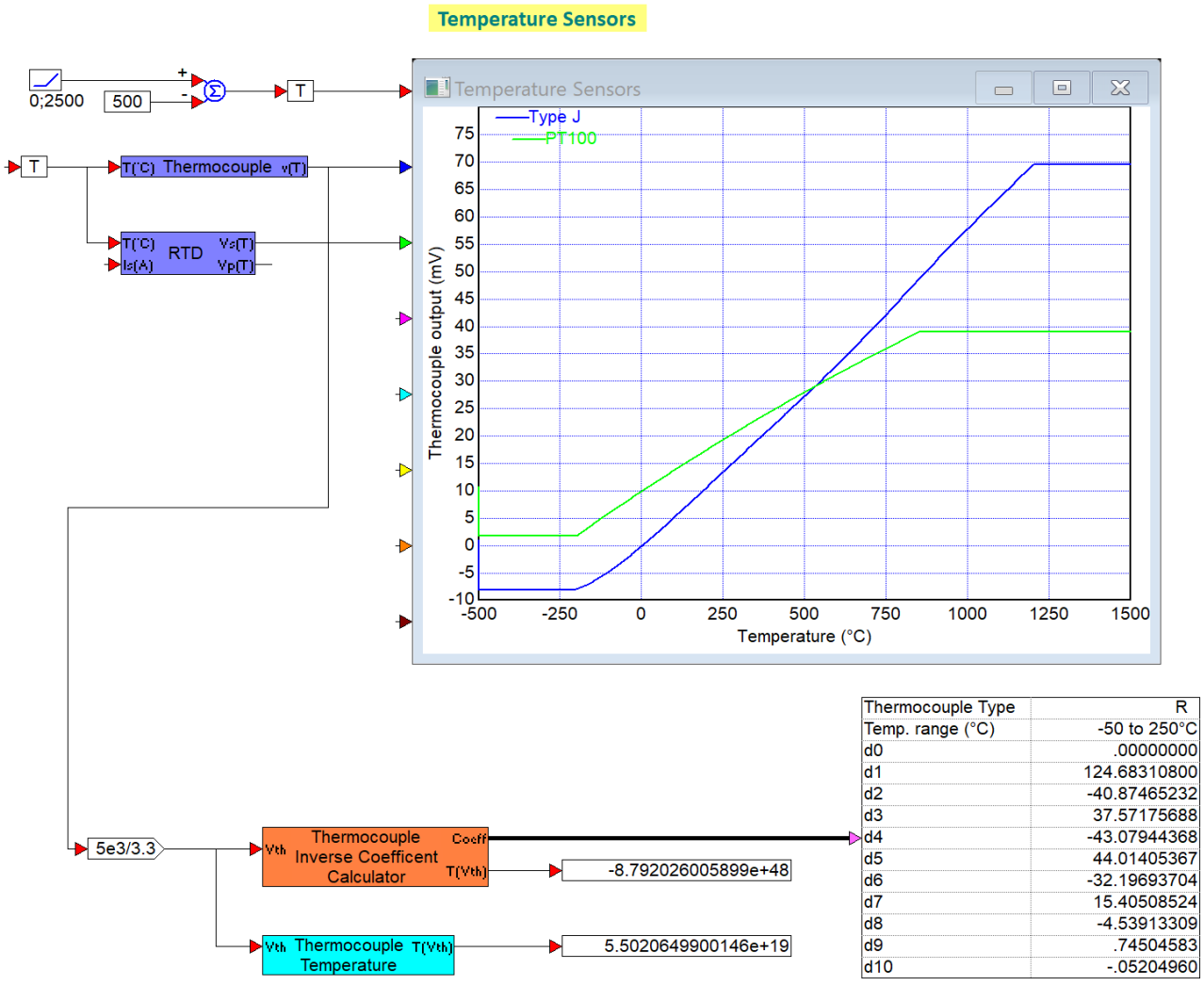
- Added the communications section with a new Synchronous Serial Interpreter (SSI) block which can interpret data from the SPI emulator in the simulation section or from exported files from popular logic analyzers.
- Added a thermocouple inverse coefficients tool.
- Added a block calculating the PWM deadtime for a given configuration.
- Included links to help files on many of the tools blocks.

EXAMPLES:

- Updated all examples with the updated blocks and features.
- Added examples showing the new management of delays in simulations.
- Added examples demonstrating the new blocks.
- Added some examples on STM32.

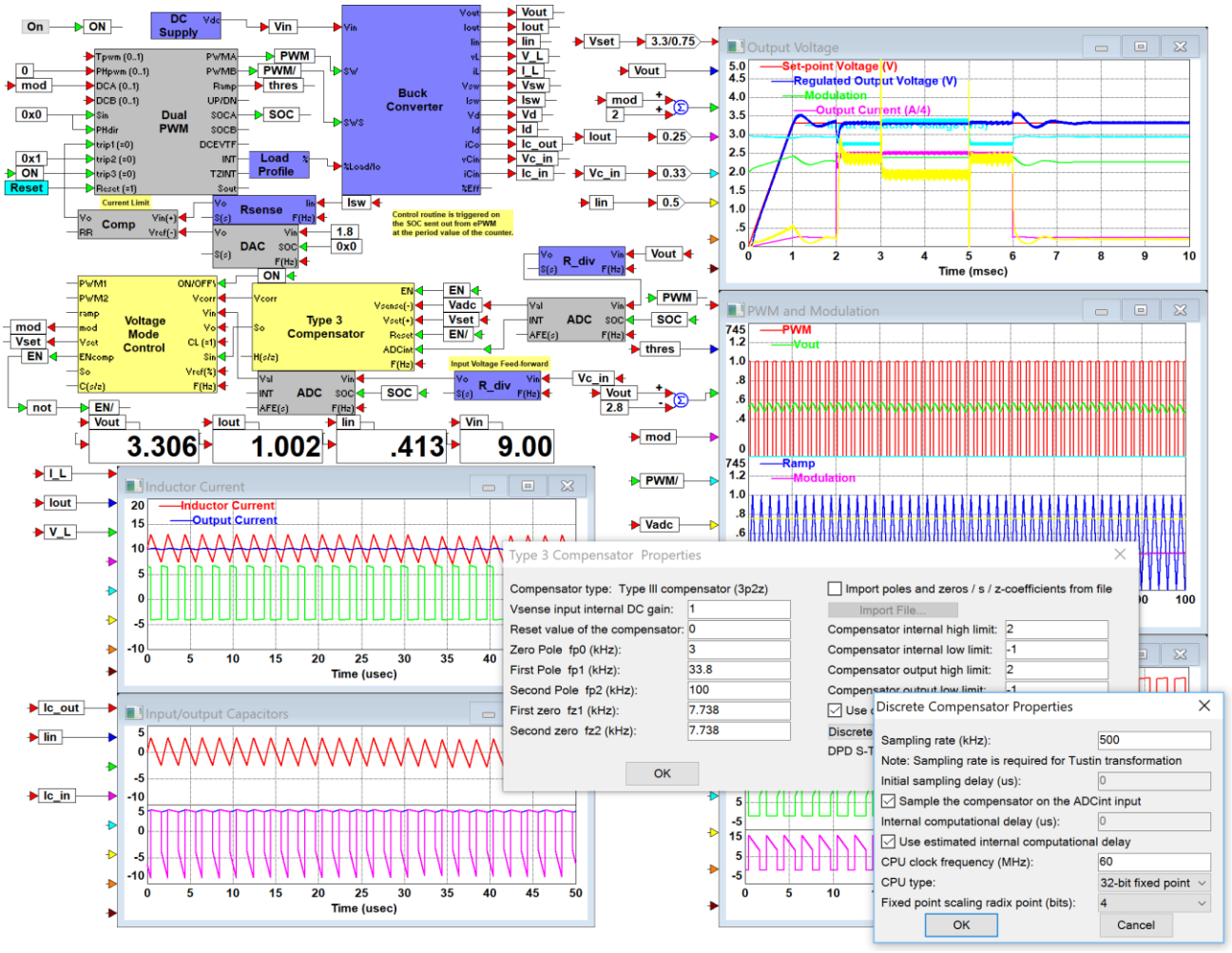
Highlights of New Features in Altair Embed 2019.2

Thermocouples and RTDs:



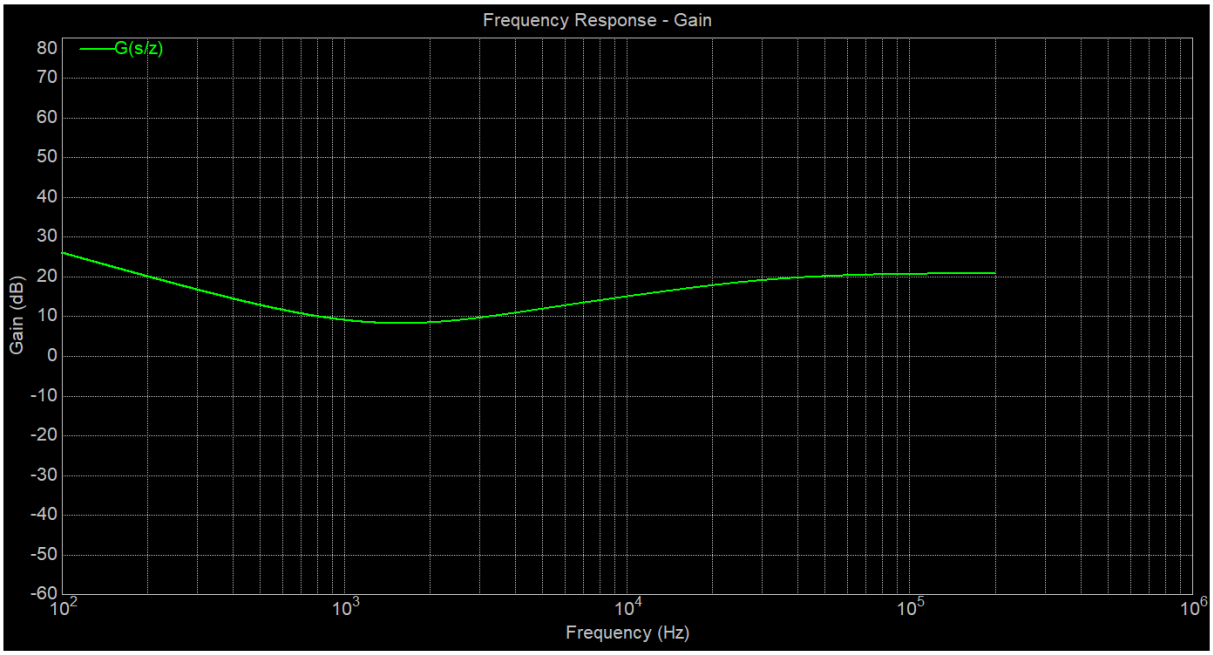
Thermocouple Type	R
Temp. range (°C)	-50 to 250°C
d0	.00000000
d1	124.68310800
d2	-40.87465232
d3	37.57175688
d4	-43.07944368
d5	44.01405367
d6	-32.19693704
d7	15.40508524
d8	-4.53913309
d9	.74504583
d10	-.05204960

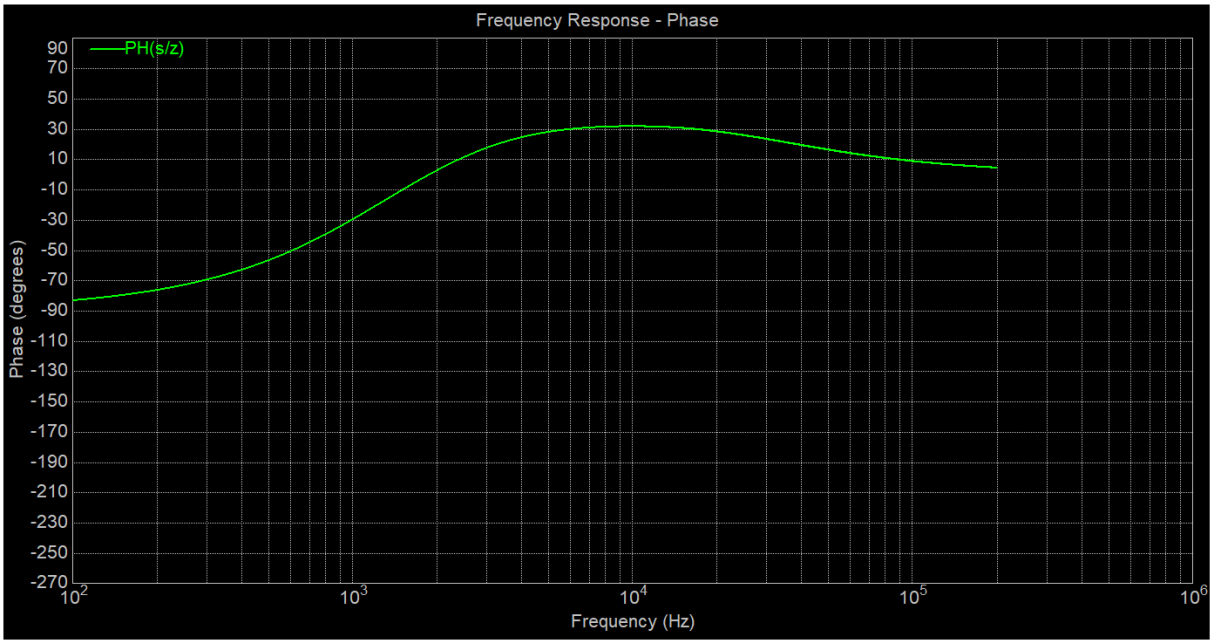
New delay management in simulations:



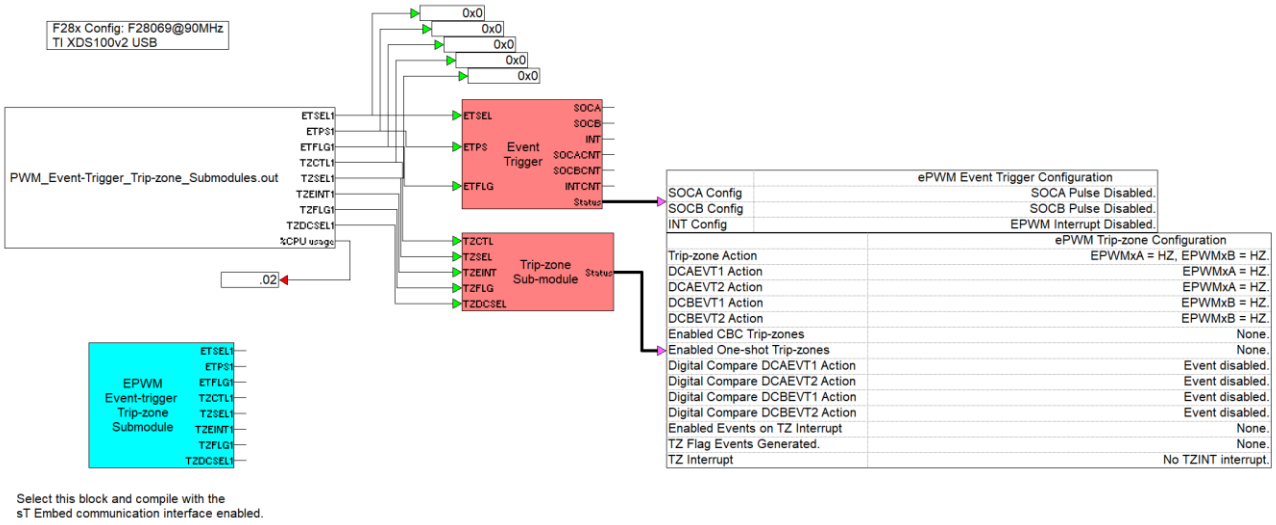
Internal frequency response added to many blocks:

3p3z Compensator

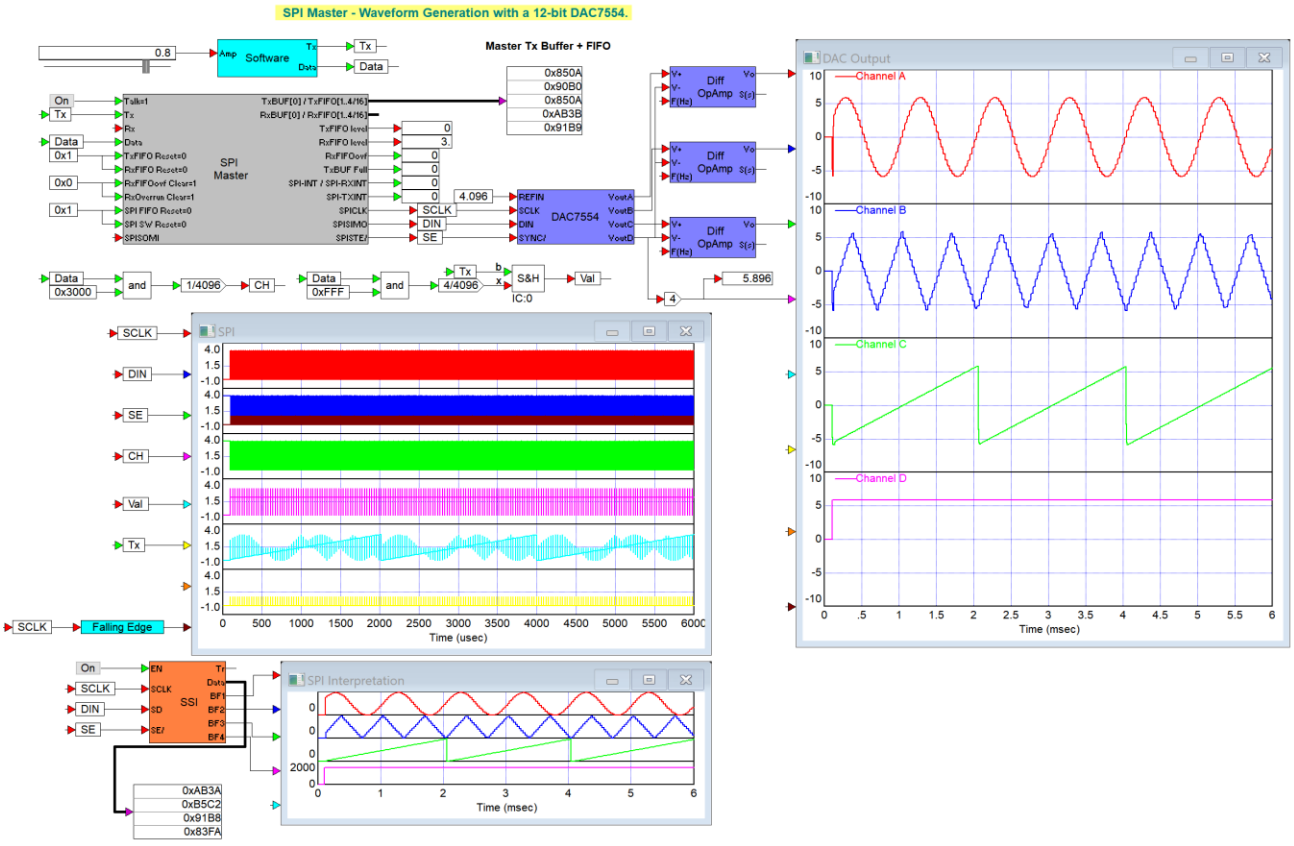




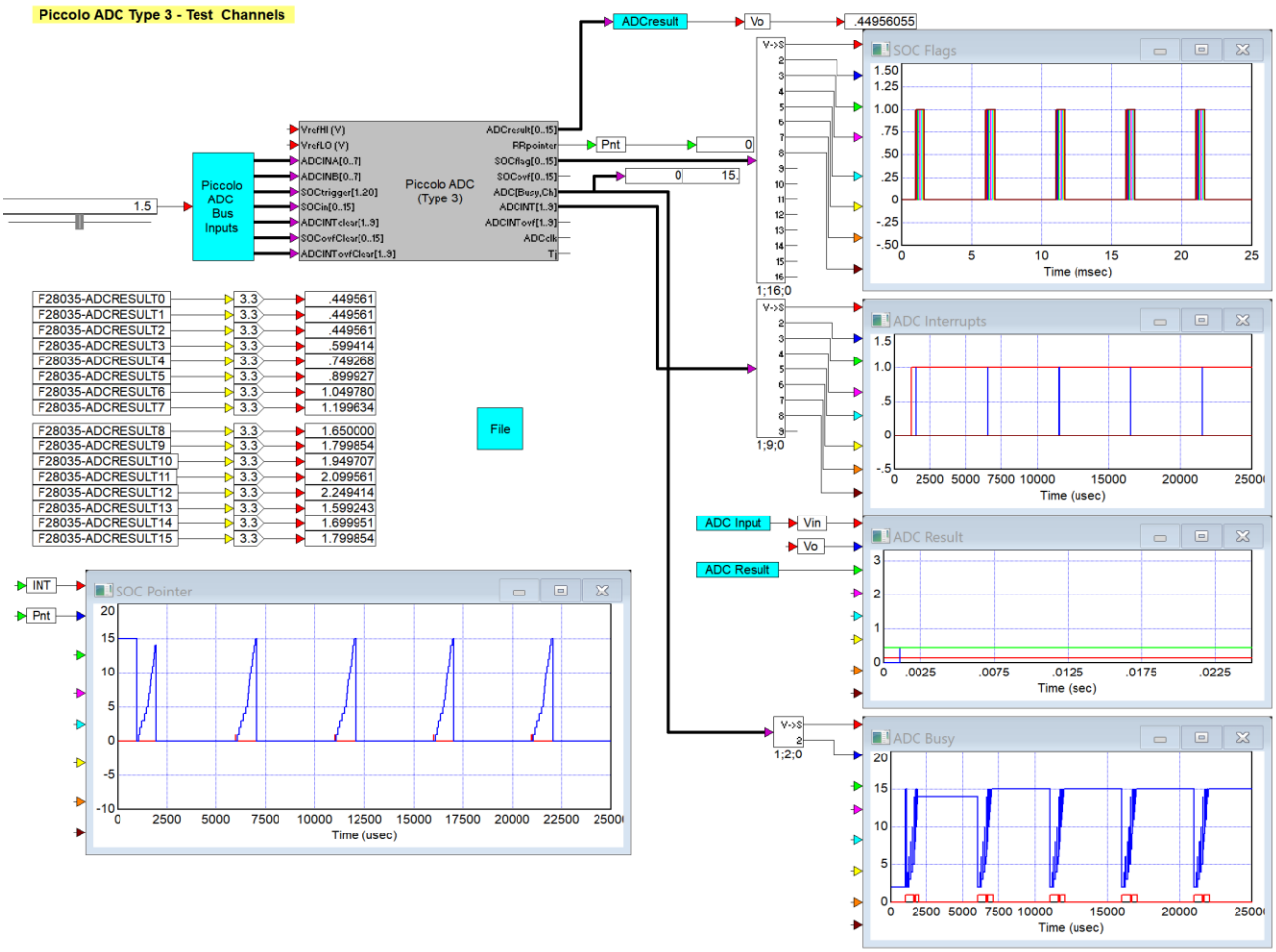
New debug blocks:



SPI Master emulator used as a signal generator in simulation:



TI C2000 piccolo ADC (Type 3) emulator:



What's New in version 2019

GENERAL:

General improvements for Altair Embed 2019 compatibility.
Added the user directory for user diagrams, models and files. Import / export files can now be saved to this directory as a default.
Added the new section on Real-time models.
Added a Components sub-section under Simulation.
Added the Measurements sub-section under Tools.

CODEGEN:

Added the reset integrators with limits under codegen -> extra.
Added the sub-section "Transformations" with various transformations often used in digital power applications.
Updated the ePWM interrupt config block and it is now located under Peripheral Configs and Functional Blocks.

DEBUG:

Expanded the peripheral availability displays for more peripherals and included the F28004x devices.
Added MCU support for the ADC Type 3 registers debug.

REAL-TIME

Added the new Real-time section with optimized average models which can be code-generated for use with real-time simulations on hardware. These models can also be used together with Analyze as another method of frequency response analysis. The models can also be used in normal simulations at larger time steps in order to perform faster simulations without modelling the switching behaviour.

SIMULATION:

Updated the generic ADC block for EOC output, adjusted the bypassing of the block and improved the moving average over-sampling filter and included the internal frequency response of the ADC.
Added a complete new sub-section on components for simulation. Deviations on converter configurations and / or non-standard converters can be simulated with these components along with passive and active circuits.
Added several configurations of converter bridges under simulation -> components -> active.
Added various passive models under simulation -> components -> passive.
Added various comprehensive single phase and 3-phase transformer models according to IEC 60076 / ANSI C57 under simulation -> components -> passive -> transformers.
Added the resonant LLC converter with full-bridge primary and center-tapped secondary.
Added the resonant controller (VMC).
Added the PV model (physical parameters) under sources.
Added the battery model under sources.
Added the DC, AC and 3-phase AC voltage sources with output source impedance.
Re-organized the dialogs of the source blocks for better clarity.

Improved the flexibility of use of the three-phase AC supply.
Corrected an issue with an incorrect phase when slewing the frequency on the AC supplies.
Corrected an error in the various full-bridge models when selecting 3 output capacitor types.

TOOLS:

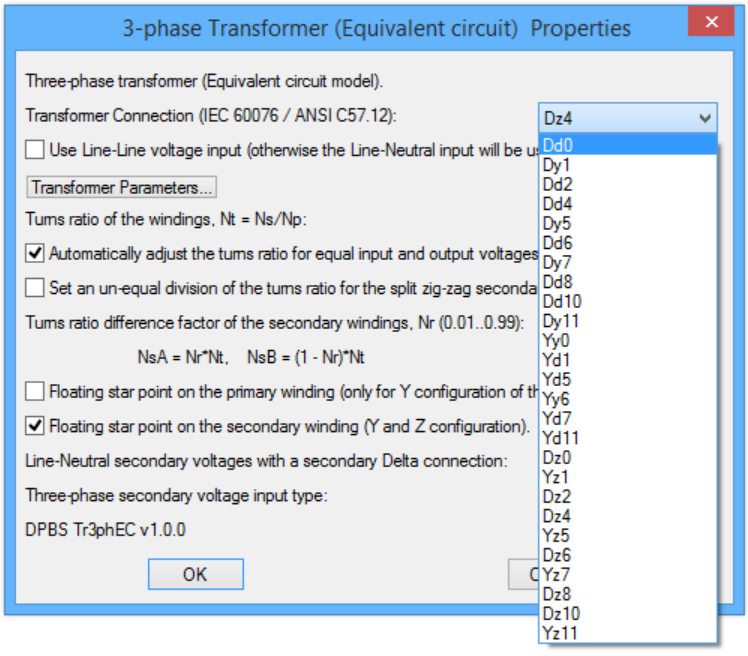
Added the file import block for importing frequency response data.
Updated and released the model-based frequency response block.
Updated and released the FRA block.
Added the Measurements section with various single-phase and 3-phase measurement blocks.
Corrected the link to the correct source file for the analog coefficient converter Type 2 compensator tool.

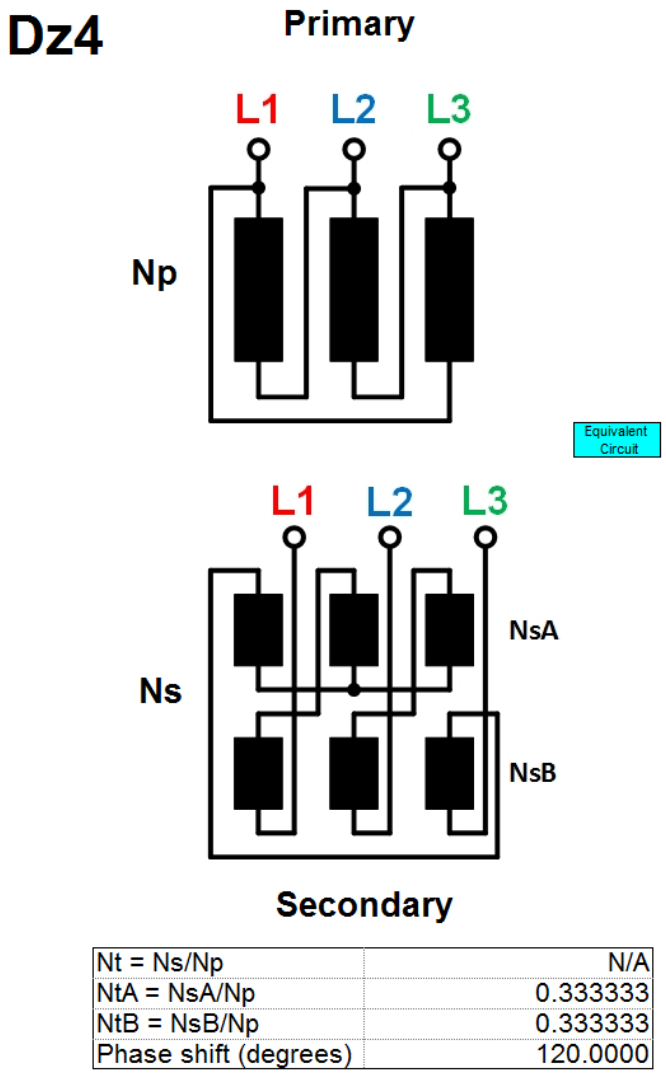
EXAMPLES:

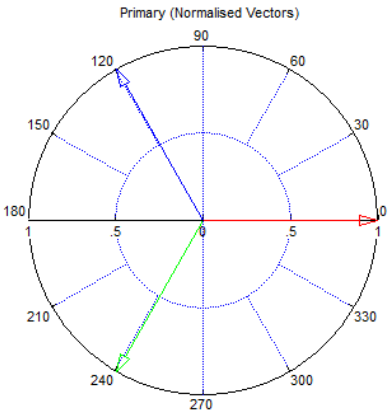
Added new examples under tools on compensator design.
Added a new section of examples under simulation -> components.
Added a new section of examples under simulation -> real-time.
Added simulation examples of the resonant LLC converter, with both analog and digital control and with voltage-mode and current-mode control.
Added new examples on many of the newly added blocks.

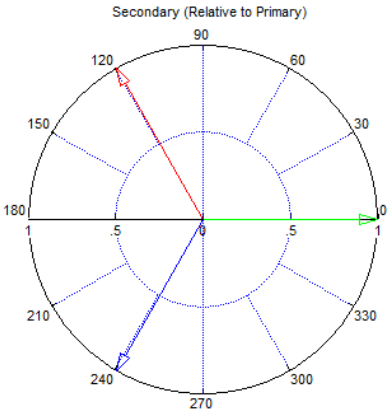
Highlights of New Features in Altair Embed 2019

Three-phase transformer:



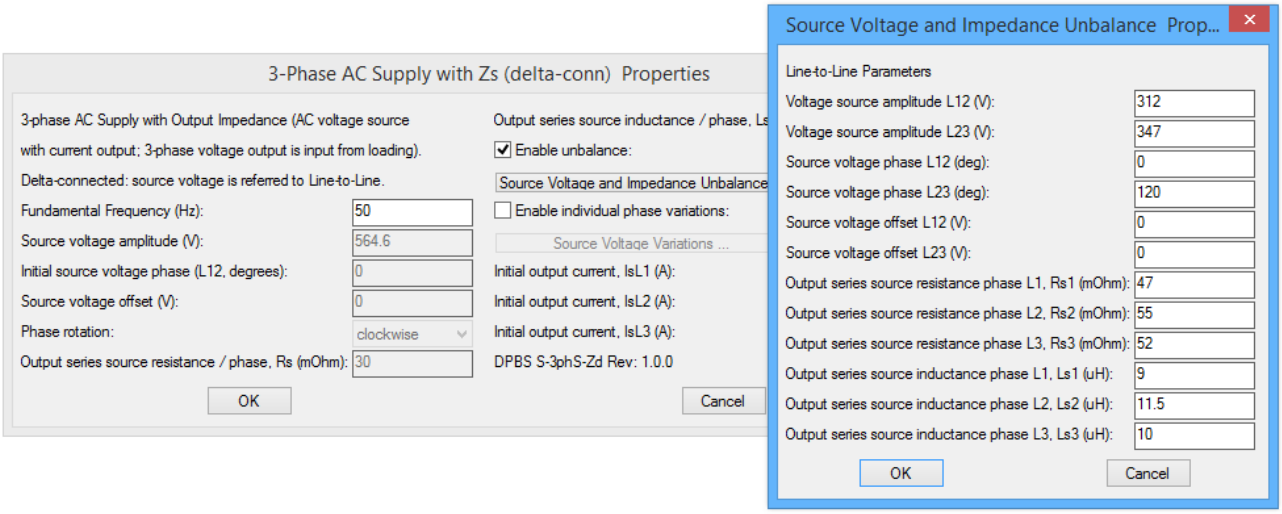


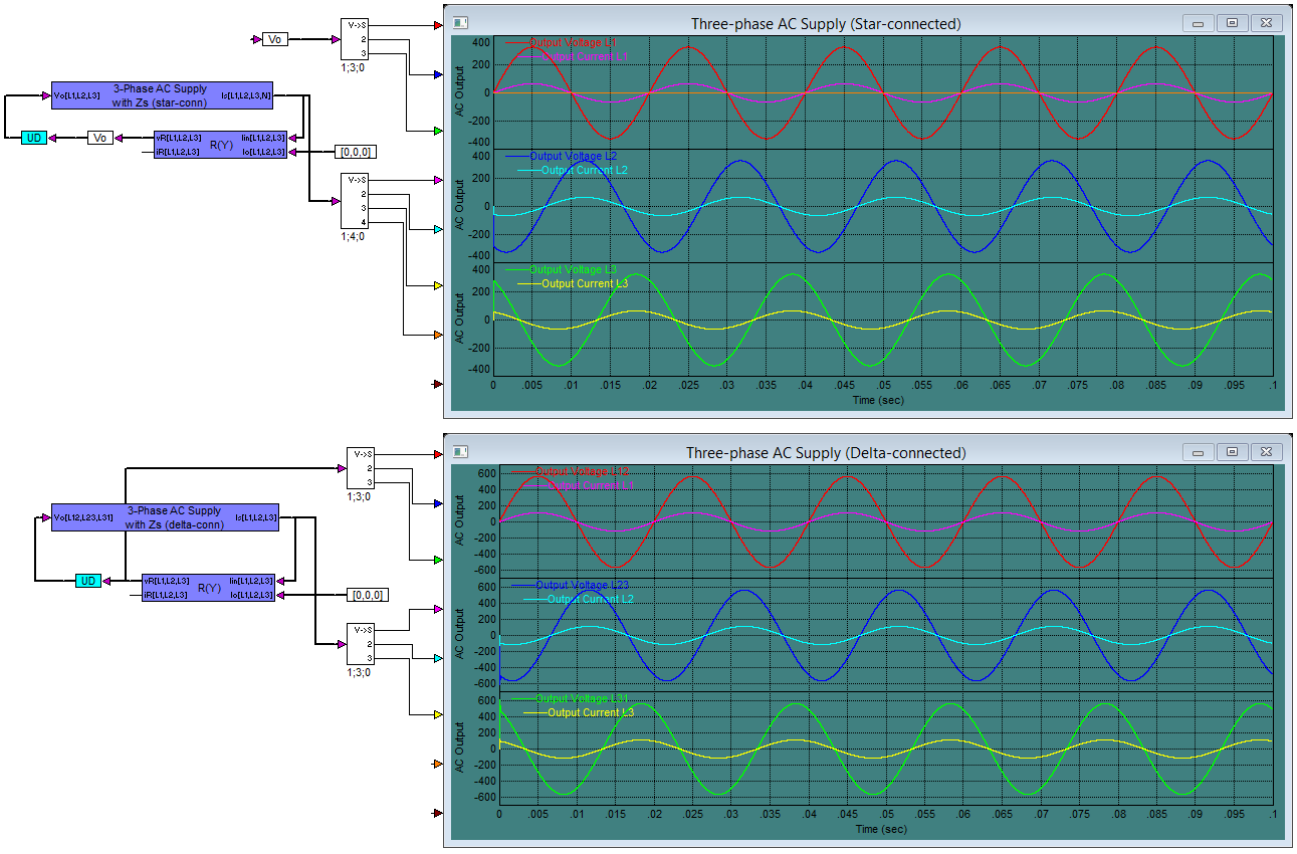




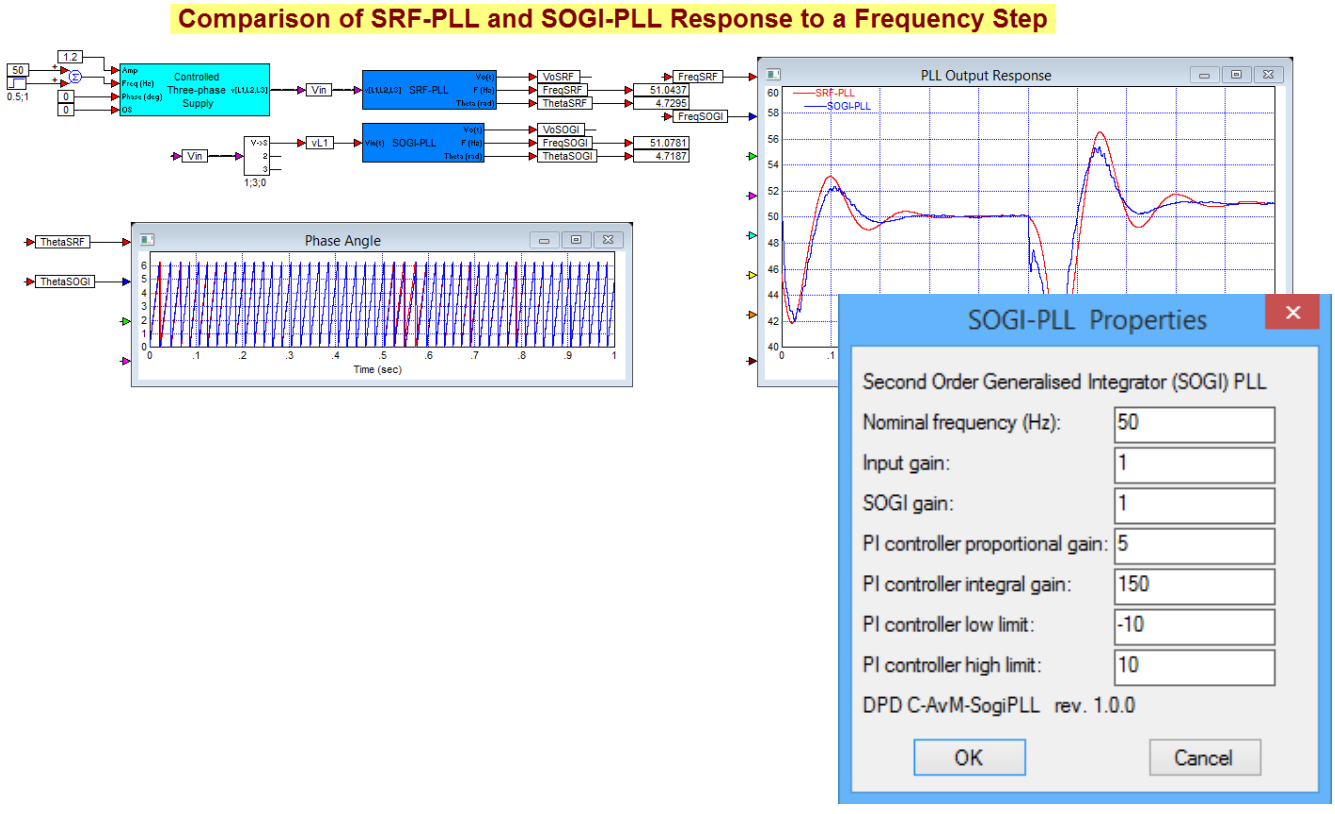
Nt = Ns/Np	N/A
NtA = NsA/Np	0.333333
NtB = NsB/Np	0.333333
Phase shift (degrees)	120.0000

Supplies with source impedance:

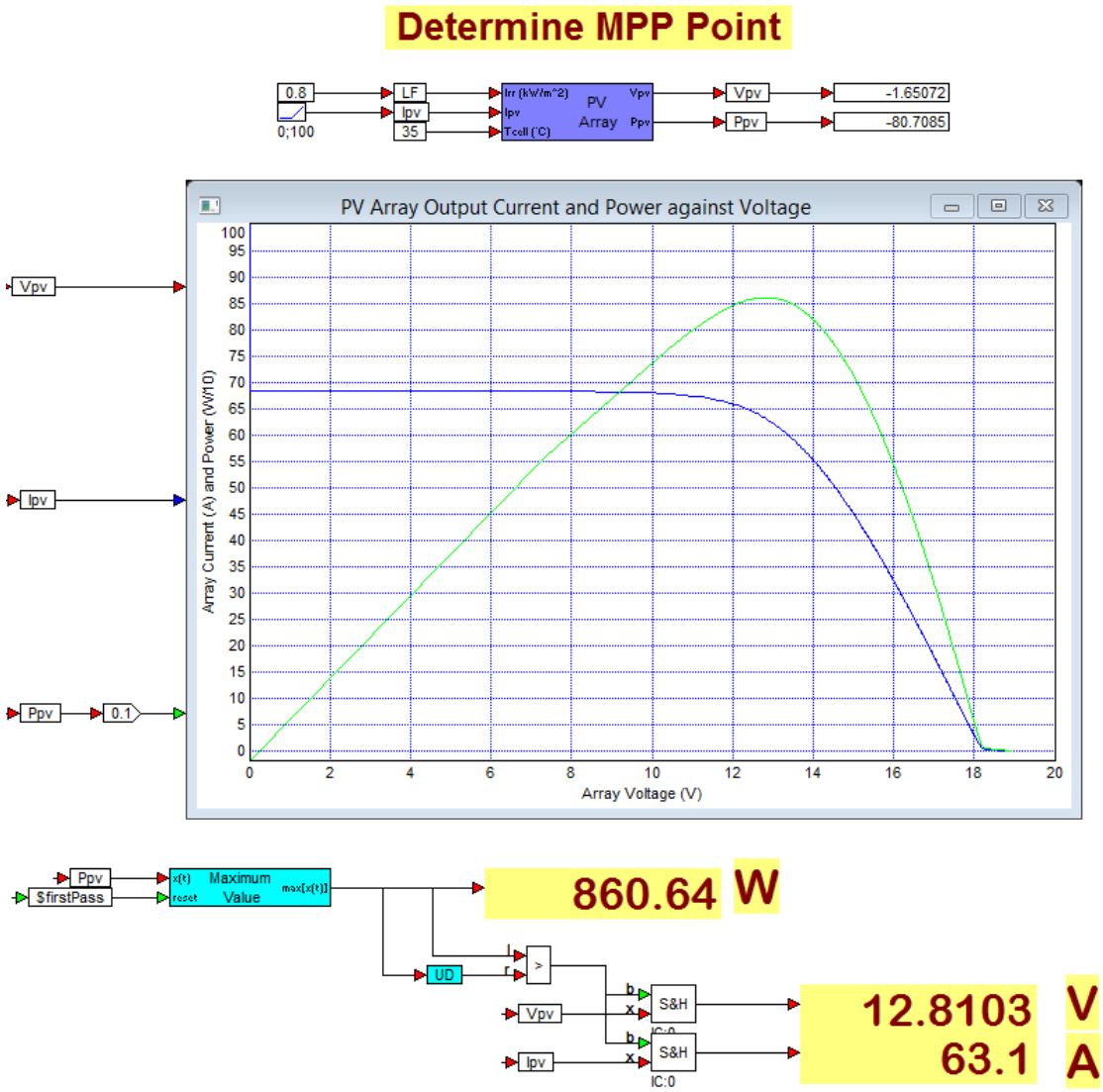




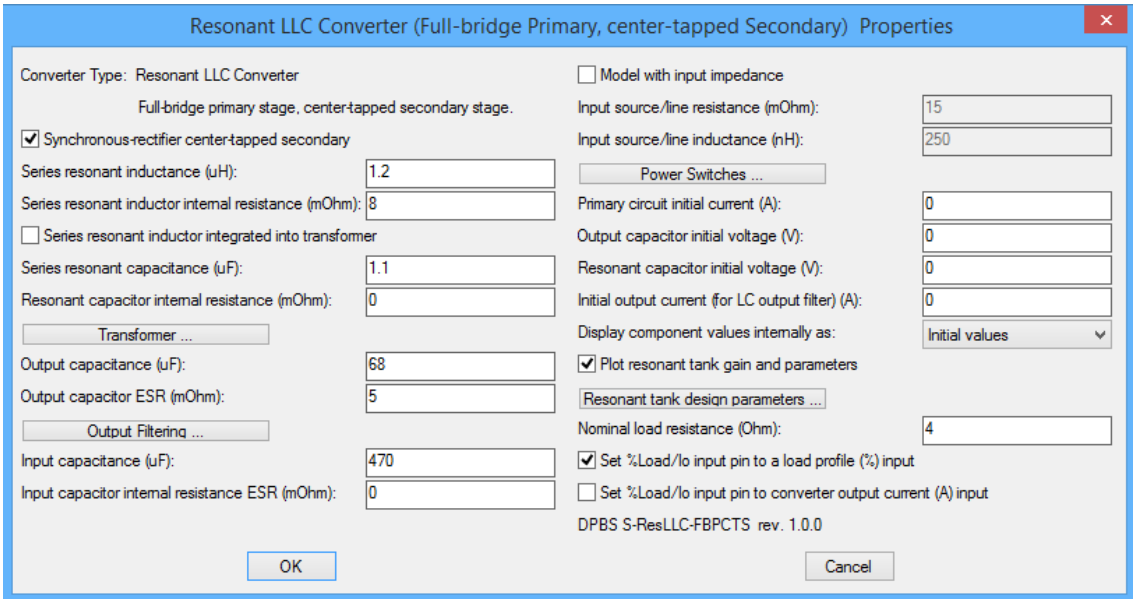
Phase-lock Loops (real-time):

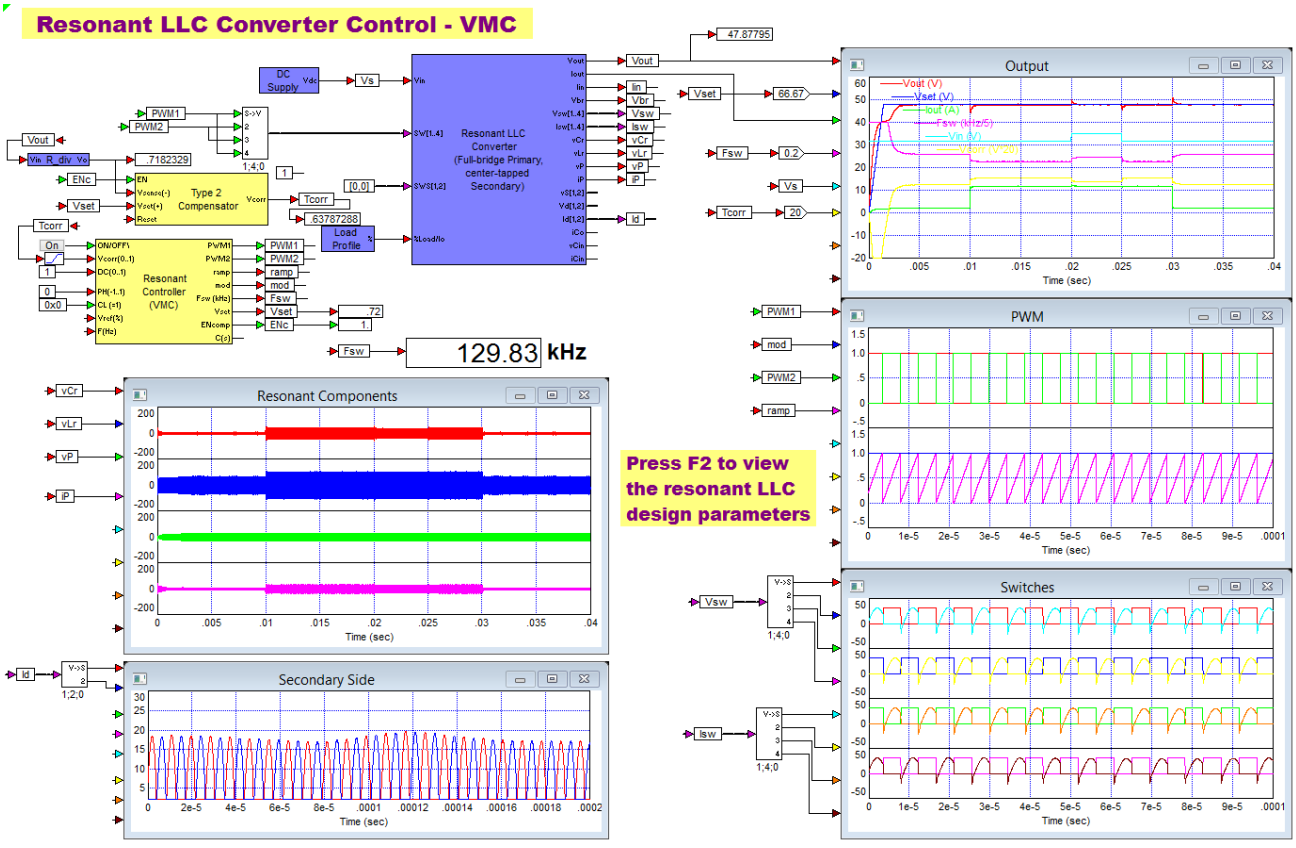


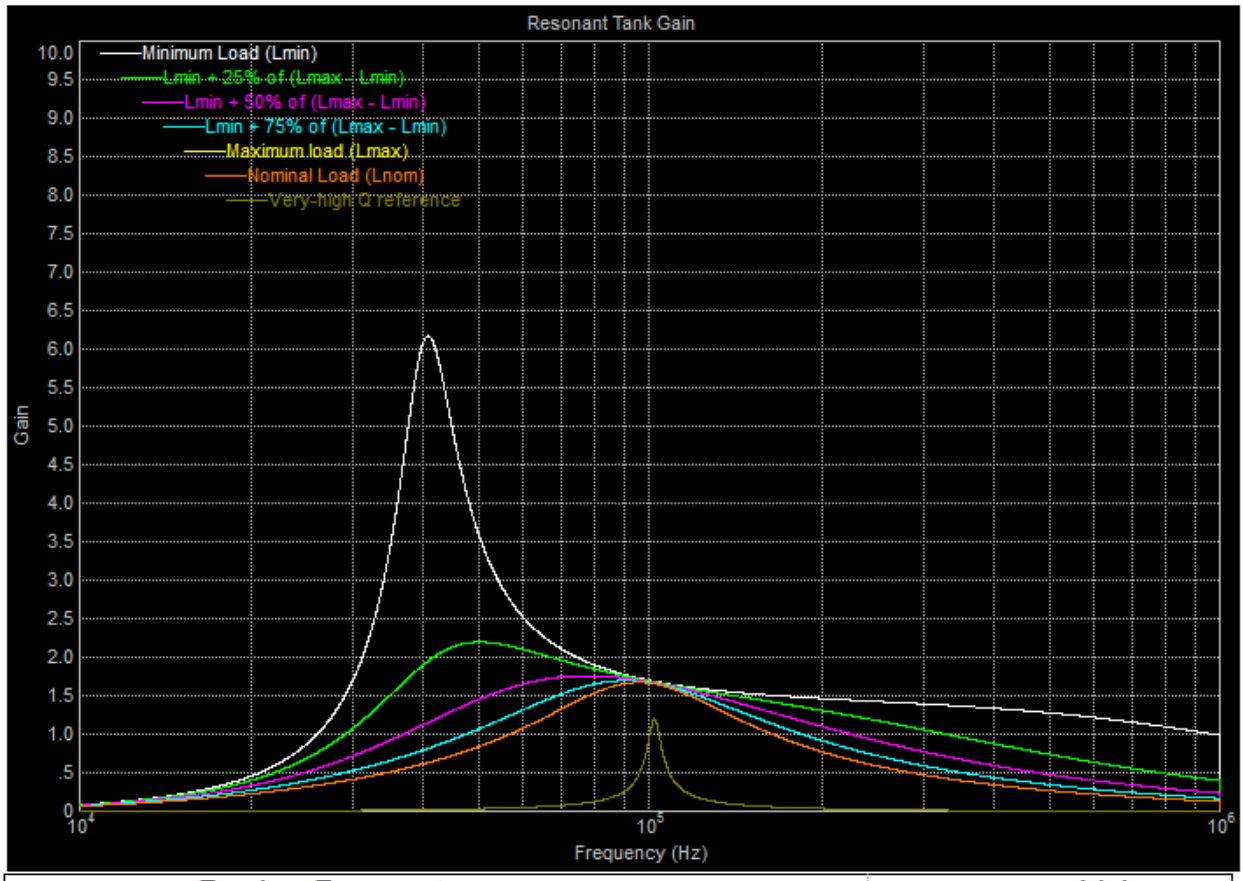
PV Array:


Determine MPP Point
0.8
0;100
LF
Ipv
35
Irr (kW/m^2)
Ipv
Tcell (°C)
PV
Array
Vpv
Ppv
Vpv
Ppv
-1.65072
-80.7085
PV Array Output Current and Power against Voltage
Array Current (A) and Power (W/10)
Array Voltage (V)
Vpv
Ipv
Ppv
0.1
Ppv
$firstPass
x(t)
reset
Maximum
Value
max[x(t)]
860.64
W
UD
>
Vpv
Ipv
S&H
S&H
IC:0
12.8103
V
63.1
A

Resonant LLC converter:







Design Parameter	Value
Resonant frequency, Fr (kHz)	102.3087
Converter Gain at Fr and nom. load	1.6658
Required Fsw at Vin nom. and nom. load, Fnom (kHz)	118.9868
Converter gain at Fnom	1.4995
Min. design Fsw at max. load, Fmin (kHz)	95.9840
Converter gain at Fmin	1.6849
Fsw at Vin max. and min. load, Fmax (kHz)	548.4005
Converter gain at Fmax	1.2620
Rac - reflected to prim. at min. load (Ohm)	11.2190
Rac - reflected to prim. at max. load (Ohm)	1.1219
Quality Factor, Q at min. load	.1261
Quality Factor, Q at max. load	1.2606
m = Lr:Lm	.1833
Characteristic Impedance (Ohm)	1.4142

Chapter 2 - Codegen

Chapter 2 - Codegen 1

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Main Contents

Block Reference – Codegen

The codegen section of the digital power designer block set consists of a series of blocks for digital power applications which can be code-generated and downloaded to a MCU and in particular, the TI C2000 series of MCUs or the STMicro 3 series.

The blocks in this section are therefore optimized for operation on an MCU. The blocks can also be used together with blocks from the simulation section to create simulation diagrams.

Compensators

There are five different digital compensators (and three variants with input pins for the coefficients) in the codegen section of the digital power designer block set. These compensators are given in three forms:

1. 16-bit fixed point
2. 32-bit fixed point
3. FPU (floating point)

Here the 32-bit fixed point blocks are described and the other two forms have identical characteristics except for the internal arithmetic format.



1P1Z Compensator

The 1p1z compensator is a first order compensator which can realize either a type 1 compensator (I-compensator) or a PI compensator in a digital format. The expression for this compensator is given by:

$$\mathbf{H_1(z) = \frac{Y(z)}{X(z)} = K_z \cdot \frac{z + B_0}{z + A_0}}$$

where the coefficients Kz, Bn and An can be derived in the various tools of the digital power designer suite or in the simulation section.

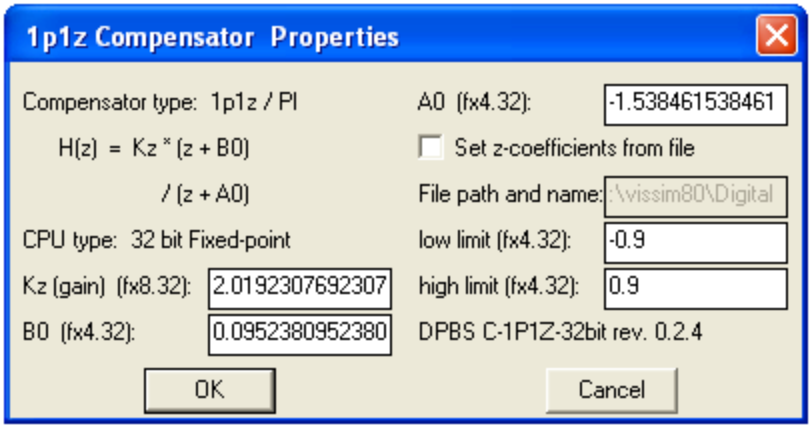
Expressed as a difference equation for implementing in a digital control algorithm this becomes, for the sample k:

$$\mathbf{Y(k) = K_z \cdot \left(X(k) + B_0 \cdot X(k-1)\right) - A_0 \cdot Y(k-1)}$$

Input pins:	**Vset(+)**	The set point voltage (positive input).
	Vsense(-)	The voltage sensing input (negative input to the compensator).
	Reset	A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to the initial value.
	Vini	The initial value of the compensator after a reset.
Output pins:	**Vcorr**	The output of the compensator.
	Verr	The output error signal which is given by: Verr = Vset – Vsense

Dialog properties:

The 1p1z compensator block properties menu is shown in the following box which appears when right-clicking on the block.



Kz (gain):

Enter the DC gain of the compensator.

B0:

Enter the value of the lowest order numerator coefficient.

A0:

Enter the value of the lowest order denominator coefficient.

Set z-coefficients from file:

Check this box to read the z-coefficients from an external file.

File path and name:

Enter the full file name and path if selected.

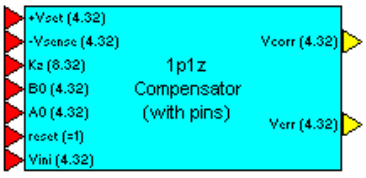
Low limit:

Enter the low-level limit of the compensator.

High limit:

Enter the high-level limit of the compensator.

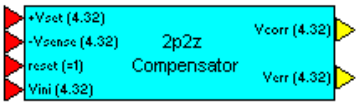
NOTE that these limits are anti-windup limits.



1P1Z Compensator (with pins)

This block is identical to the 1p1z compensator above except that the coefficients can be set using the input pins. In this way, the coefficients become variables and can be updated or changed during a simulation or a MCU routine.

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2P2Z Compensator

The 2p2z compensator is a second order compensator which can realize either a type 2 compensator or a PID compensator in a digital format. This compensator has the discrete transfer function:

$$H_2(z) = \frac{Y(z)}{X(z)} = K_z \cdot \frac{z^2 + B_1 \cdot z + B_0}{z^2 + A_1 \cdot z + A_0}$$

where the coefficients Kz, Bn and An can be derived in the various tools of the digital power designer suite or in the simulation section.

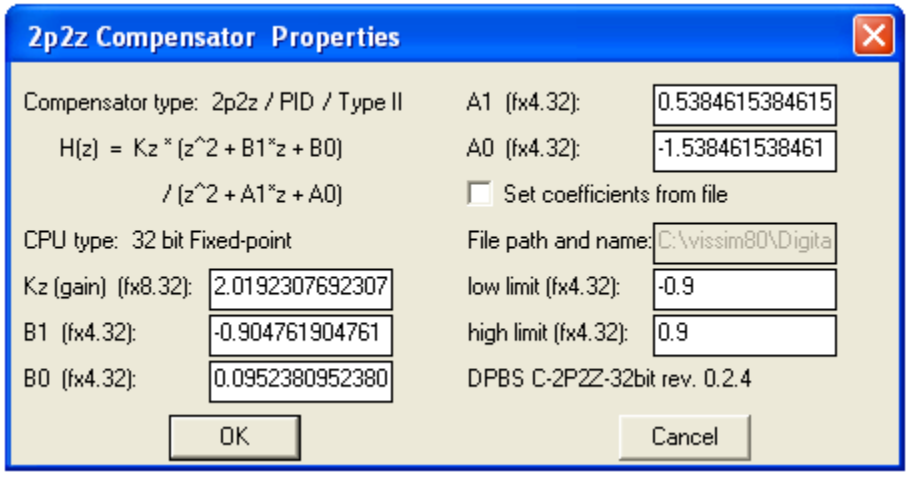
Expressed as a difference equation for implementing in a digital control algorithm this becomes, for the sample k:

$$Y(k) = K_z \cdot \left(X(k) + B_1 \cdot X(k-1) + B_0 \cdot X(k-2)\right) - A_1 \cdot Y(k-1) - A_0 \cdot Y(k-2)$$

Input pins:	**Vset(+)**	The set point voltage (positive input).
	Vsense(-)	The voltage sensing input (negative input to the compensator) .
	Reset	A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to the initial value.
	Vini	The initial value of the compensator after a reset.
Output pins:	**Vcorr**	The output of the compensator.
	Verr	The output error signal which is given by: Verr = Vset – Vsense

Dialog properties:

The 2p2z compensator block properties menu is shown in the following box which appears when right-clicking on the block.



Kz (gain):

Enter the DC gain of the compensator.

B1:

Enter the value of the first order numerator coefficient.

B0:

Enter the value of the lowest order numerator coefficient.

A1:

Enter the value of the first order denominator coefficient.

A0:

Enter the value of the lowest order denominator coefficient.

Set z-coefficients from file:

Check this box to read the z-coefficients from an external file.

File path and name:

Enter the full file name and path if selected.

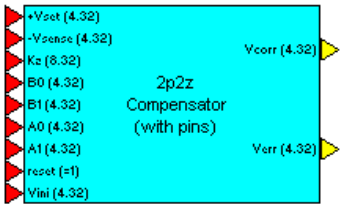
Low limit:

Enter the low-level limit of the compensator.

High limit:

Enter the high-level limit of the compensator.

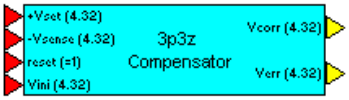
NOTE that these limits are anti-windup limits.



2P2Z Compensator (with pins)

This block is identical to the 2p2z compensator above except that the coefficients can be set using the input pins. In this way, the coefficients become variables and can be updated or changed during a simulation or a MCU routine.

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3P3Z Compensator

The 3p3z compensator is a third order compensator which can realize either a type 3 compensator or a 3p3z compensator in a digital format. This compensator has the transfer function:

$$H_3(z) = \frac{Y(z)}{X(z)} = K_z \cdot \frac{z^3 + B_2 \cdot z^2 + B_1 \cdot z + B_0}{z^3 + A_2 \cdot z^2 + A_1 \cdot z + A_0}$$

where the coefficients Kz, Bn and An can be derived in the various tools of the digital power designer suite or in the simulation section.

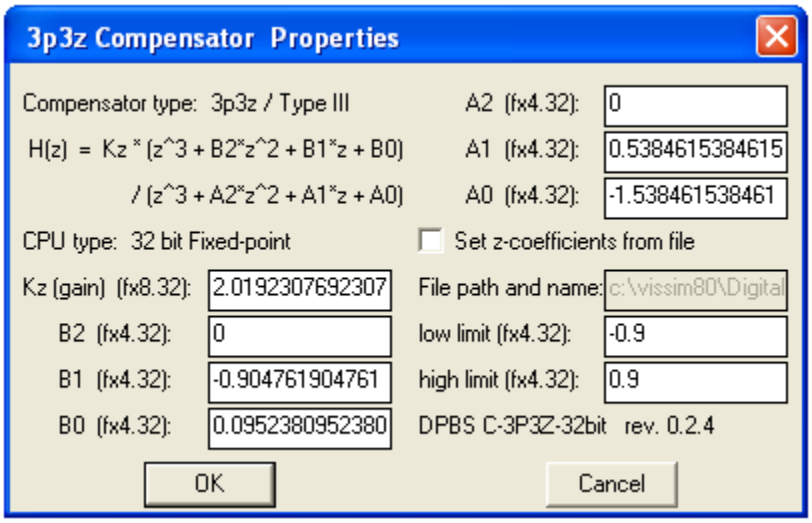
Expressed as a difference equation for implementing in a digital control algorithm this becomes, for the sample k:

$$Y(k) = K_z \cdot \left(X(k) + B_2 \cdot X(k-1) + B_1 \cdot X(k-2) + B_0 \cdot X(k-3)\right) - A_2 \cdot Y(k-1) - A_1 \cdot Y(k-2) - A_0 \cdot Y(k-3)$$

Input pins:	**Vset(+)**	The set point voltage (positive input).
	Vsense(-)	The voltage sensing input (negative input to the compensator) .
	Reset	A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to the initial value.
	Vini	The initial value of the compensator after a reset.
Output pins:	**Vcorr**	The output of the compensator.
	Verr	The output error signal which is given by: Verr = Vset – Vsense

Dialog properties:

The 3p3z compensator block properties menu is shown in the following box which appears when right-clicking on the block.



Kz (gain):

Enter the DC gain of the compensator.

B2:

Enter the value of the second order numerator coefficient.

B1:

Enter the value of the first order numerator coefficient.

B0:

Enter the value of the lowest order numerator coefficient.

A2:

Enter the value of the second order denominator coefficient.

A1:

Enter the value of the first order denominator coefficient.

A0:

Enter the value of the lowest order denominator coefficient.

Set z-coefficients from file:

Check this box to read the z-coefficients from an external file.

File path and name:

Enter the full file name and path if selected.

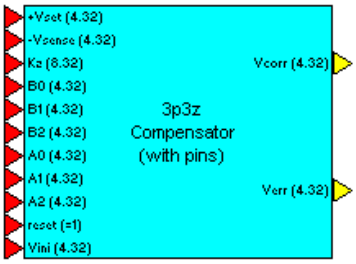
Low limit:

Enter the low-level limit of the compensator.

High limit:

Enter the high-level limit of the compensator.

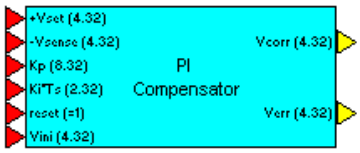
NOTE that these limits are anti-windup limits.



3P3Z Compensator (with pins)

This block is identical to the 3p3z compensator above except that the coefficients can be set using the input pins. In this way, the coefficients become variables and can be updated or changed during a simulation or MCU routine.

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PI compensator

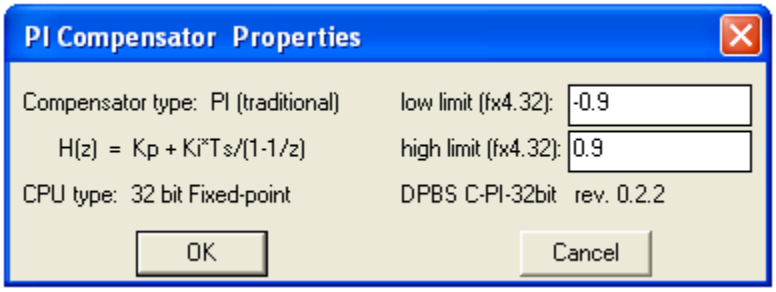
The PI compensator is a proportional + integral gain compensator . It is a first order compensator with one pole at the origin and one zero. This block enables the setting of the coefficients using the familiar proportional and integral gains rather than the poles and zeros. This type of compensator is popular in certain applications (current mode control or auxiliary loops such as paralleling) due to its simplicity (only two parameters need to be set). This compensator has the transfer function:

$$H_{pi}(z) = K_p + K_i \cdot T_s \cdot \left(\frac{z}{z-1} \right)$$

Input pins:	**Vset(+)**	The set point voltage (positive input).
	Vsense(-)	The voltage sensing input (negative input to the compensator) .
	Kp	The value of the proportional gain for the compensator.
	Kp*Ts	The value of the integral gain multiplied by the sampling time.
	Reset	A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to the initial value.
	Vini	The initial value of the compensator after a reset.
Output pins:	**Vcorr**	The output of the compensator.
	Verr	The output error signal which is given by: Verr = Vset – Vsense

Dialog properties:

The PI compensator block properties menu is shown in the following box which appears when right-clicking on the block.



Low limit:

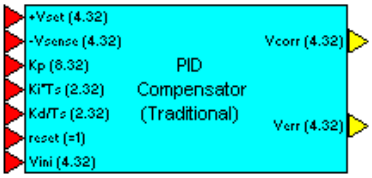
Enter the low-level limit of the compensator.

High limit:

Enter the high-level limit of the compensator.

NOTE that these limits are anti-windup limits.

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PID compensator (traditional)

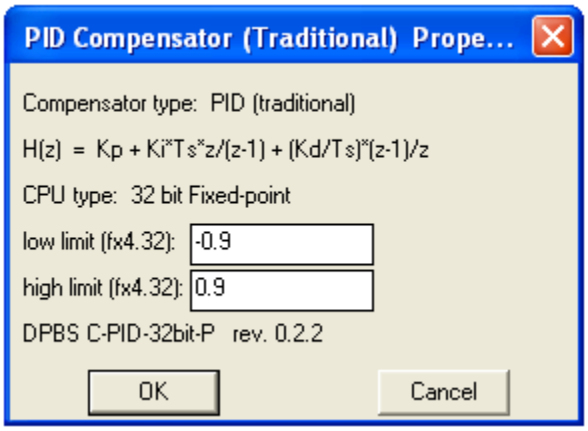
This compensator is a second order compensator allowing the setting of the proportional, integral and differential gains. The differential part of the transfer function is approximated to the difference of the last two samples times the differential gain. This compensator would have effectively two zeros and one pole at the origin. This compensator would more regularly be replaced by the 2p2z PID compensator for digital power applications. This compensator has the transfer function:

$$H_{pid}(z) = K_p + K_i \cdot T_s \cdot \left(\frac{z}{z-1}\right) + \frac{K_d}{T_s} \cdot \left(\frac{z-1}{z}\right)$$

Input pins:	**Vset(+)**	The set point voltage (positive input).
	Vsense(-)	The voltage sensing input (negative input to the compensator) .
	Kp	The value of the proportional gain for the compensator.
	Kp*Ts	The value of the integral gain multiplied by the sampling time.
	Kd/Ts	The value of the differential gain divided by the sampling time.
	Reset	A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to the initial value.
	Vini	The initial value of the compensator after a reset or at start-up.
Output pins:	**Vcorr**	The output of the compensator.
	Verr	The output error signal which is given by: Verr = Vset – Vsense

Dialog properties:

The PID compensator properties menu is shown in the following box which appears when right-clicking on the block.

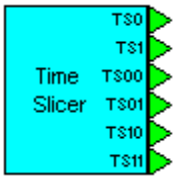


Low limit:	Enter the low-level limit of the compensator.
High limit:	Enter the high-level limit of the compensator.

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Controllers

Controllers are generally used in conjunction with the compensators to perform the major part of digital power control loops for various control techniques. The time slicer is an exception here which is used to control the time frame for the execution of various tasks.

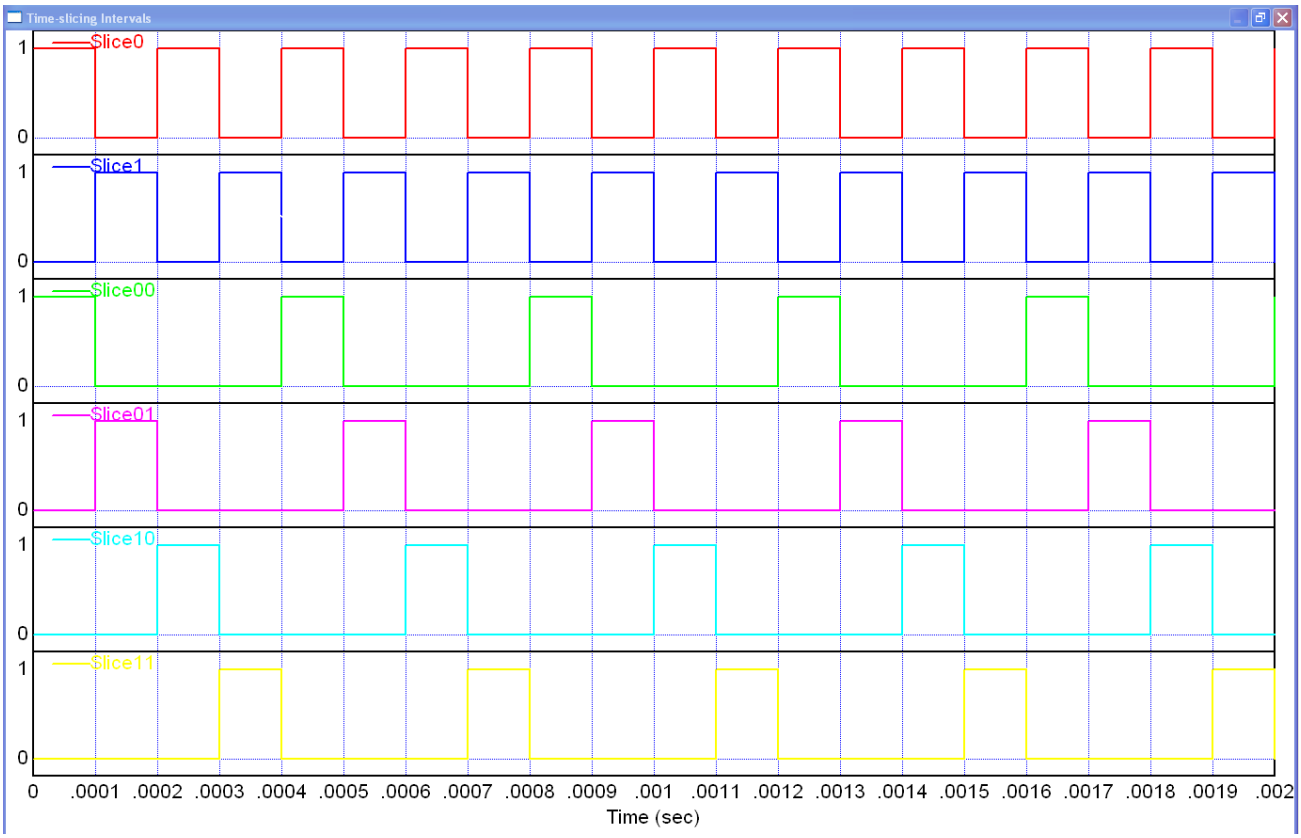


Time slicer

The time slicer controller performs time division multiplexing, first by two and additionally by four.

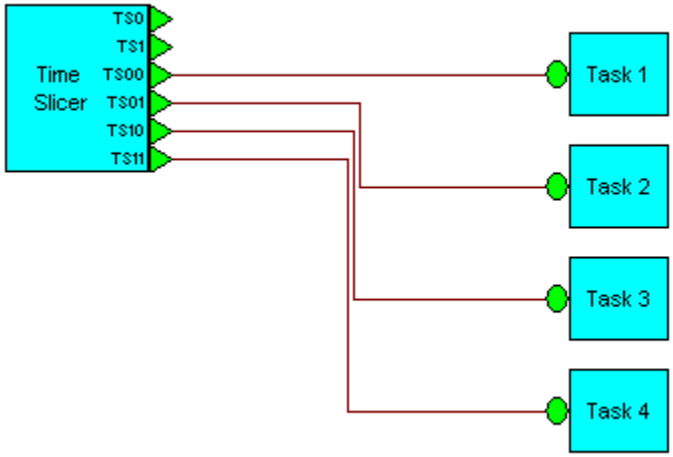
Output pins:	**TS0**	Time divided by 2; first interval.
	TS1	Time divided by 2; second interval.
	TS00	Time divided by 4; first interval.
	TS01	Time divided by 4; second interval.
	TS10	Time divided by 4; third interval.
	TS11	Time divided by 4; fourth interval.

The time intervals are represented in the following graph.



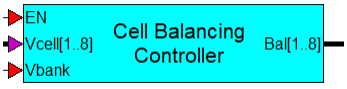
If a task does not need to run at the full ISR rate then its rate can be divided down by an integer number of the ISR rate. If several tasks are to be run at the divided down rate, then simply setting them to the same rate can create problems with CPU usage as the various tasks will be executed during the same ISR time frame, perhaps overloading the CPU with tasks in that frame while during other time frames, the CPU will be relatively free. This situation can be avoided with time slicing so that the task execution is more evenly distributed over time.

The time slicer would be normally connected up in a diagram similar to the following:



Without time-slicing, the tasks, which would then each be chosen to run at a larger local time step in the compound block properties, would all be executed together during the time frame TS00, perhaps burdening too much the CPU during this ISR cycle while the next three ISR cycles have execution time in reserve. With time-slicing, the four tasks (especially if identical in execution time), will be executed with a more even distribution over time and possibly allowing for additional tasks to be included in the routine at the full ISR rate.

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Cell Balancing Controller

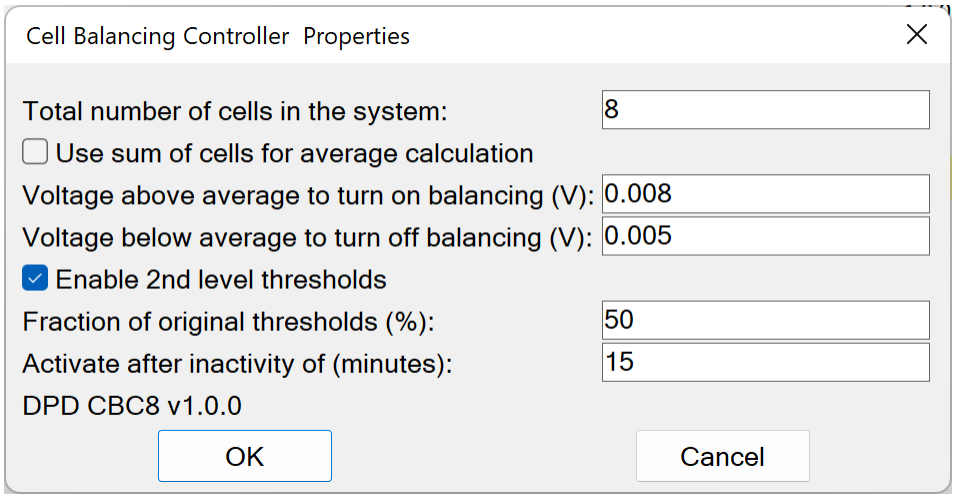
The cell balancing controller can control the switching of the balancing resistors for up to 8 series-connected cells. This controller would normally be used together with the passive cell balance in the simulation section.

More than 8 cells can be balanced by using multiple cell balancing controllers and passive cell balancer blocks in a diagram.

Input pins:	**EN**	Enable input for the balancing controller.
	Vcell[1..8]	Input for the cell voltages of 1 to 8 cells.
	Vbank	Input for the total battery bank voltage of the series-connected cells (V).
Output pins:	**Bal[1..8]**	Output switch for the balancing resistors for 1 to 8 cells.

Dialog properties:

The Cell balancing controller properties menu is shown in the following box which appears when right-clicking on the block.



Total number of cells in the system:

Select the total number of series-connected cells to be balanced (may be more than 8 if multiple controller blocks are used).

Use sum of cells for average calculation:

Select this option if there are 8 cells or less and the average is calculated by the individual cell voltages, otherwise the average is calculated from the total battery voltage.

Voltage above average to turn on balancing (V):

Enter the threshold voltage above the average cell voltage at which the balancing must turn on.

Voltage below average to turn off balancing (V):

Enter the threshold voltage below the average cell voltage at which the balancing turns off.

Enable 2nd level thresholds:

Second level thresholds can be enabled in order to further fine tune the balancing of the cells.

Fraction of original thresholds (%):

The thresholds can be reduced to from 0 to 90% of the original thresholds.

Activate after inactivity of (minutes):

If the balancing becomes inactive for longer than this delay (cell voltages remain within the larger threshold range), the second level thresholds will be activated.



Voltage Mode Controller (VMC)

The voltage mode controller operates together with a compensator to control the output voltage of a digital power converter. In this control mode, the output voltage feedback is compared with a set reference and the output duty cycle is varied according to the input voltage correction signal (from a compensator).

Input pins:

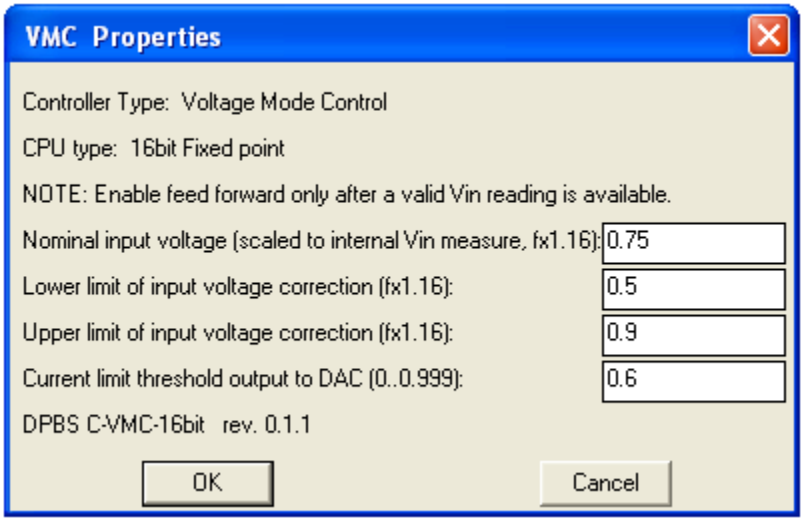
Vcorr The input signal which is normally connected directly from a compensator block.

EN_FF This pin will enable the input voltage feed forward when ≥ 1.

	Vin(t)	The input voltage sensing input for input voltage feed forward compensation.
Output pins:	**DC**	The output of the controller (duty cycle) to be connected to a ePWM block DC input.
	CLthres	The current limit threshold value which can be connected to a DAC input.

Dialog properties:

The VMC properties menu is shown in the following box which appears when right-clicking on the block.



Nominal input voltage:

Enter the value of the nominal input voltage (for input voltage feed-forward) as scaled down and seen by the input of the block at Vin(t).

Lower limit of input voltage correction:

Enter the lower limit of the input voltage correction for input voltage feed-forward.

Upper limit of input voltage correction:

Enter the upper limit of the input voltage correction for input voltage feed-forward.

Current limit threshold output to DAC:

Enter the current limit threshold value (0 to 1 in this case).

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Average Current Mode Controller (ACMC)

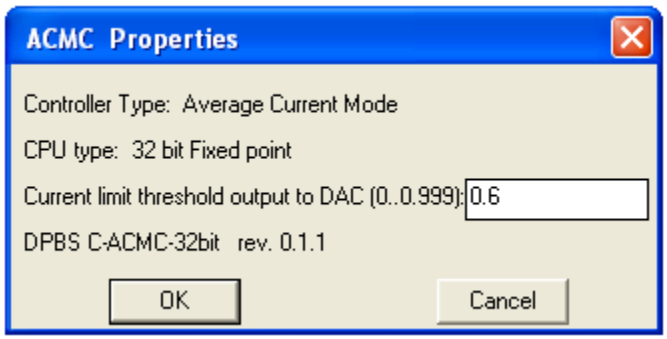
The average current mode controller operates together with a compensator to control the output voltage of a digital power converter using average current mode control.

Input pins:	**Vcorr**	The input signal which is normally connected directly from a compensator block.
	Vref(t)	An input reference signal which is be used to multiply the with the output correction signal.
Output pins:	**DC**	The output of the controller (duty cycle) to be connected to a ePWM block DC input.

CLthres The current limit threshold value which can be connected to a DAC input.

Dialog properties:

The ACMC properties menu is shown in the following dialog which appears when right-clicking on the block.



Current limit threshold output to DAC:

Enter the current limit threshold value (0 to 1 in this case).

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Hysteretic Current Mode Controller (HCMC)

The hysteretic current mode controller operates together with a compensator to control the output voltage of a digital power converter by comparing the inductor current with an upper and lower threshold and maintaining this current within these thresholds.

Input pins: **Vcorr** The input signal which is normally connected directly from a compensator block.

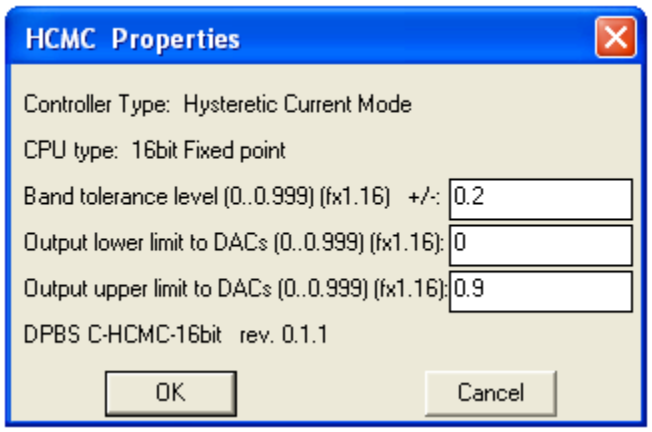
Vref(t) The voltage sensing input (negative input to the compensator) .

Output pins: **DAC_UL** The output upper threshold value to be connected to a DAC block.

DAC_LL The output lower threshold value to be connected to a DAC block.

Dialog properties:

The HCMC properties menu is shown in the following box which appears when right-clicking on the block.



Band tolerance level:

Enter the value of the hysteresis band as a fraction of 1.

Output lower limit to DAC:

Enter the lower limit of the output threshold level.

Output upper limit to DAC:

Enter the upper limit of the output threshold level.



Zero-transition Current Mode Controller (ZCMC)

The zero-transition current mode controller operates together with a compensator to control the output voltage of a digital power converter where the inductor current returns to zero at the end of each cycle.

Input pins: **Vcorr** The input signal which is normally connected directly from a compensator block.

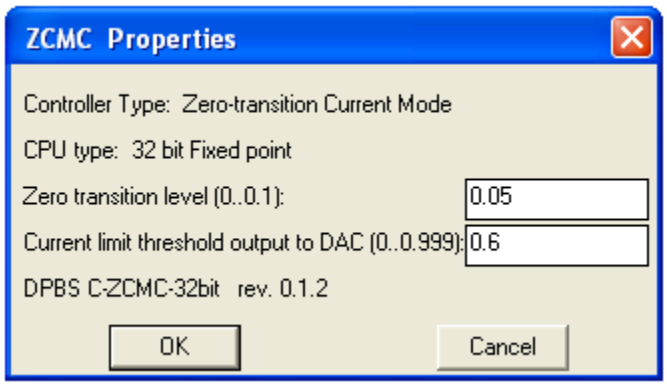
Vref(t) The voltage sensing input (negative input to the compensator) .

Output pins: **DC** The output of the controller (duty cycle) to be connected to a ePWM block DC input.

DAC_zero The zero threshold level (usually slightly above zero), to connect to a DAC block.

Dialog properties:

The ZCMC properties menu is shown in the following box which appears when right-clicking on the block.



Zero transition level:

As the current may not fall exactly to zero, a near zero value can be entered here.

Current limit threshold output to DAC:

Enter the current limit threshold value (0 to 1 in this case).

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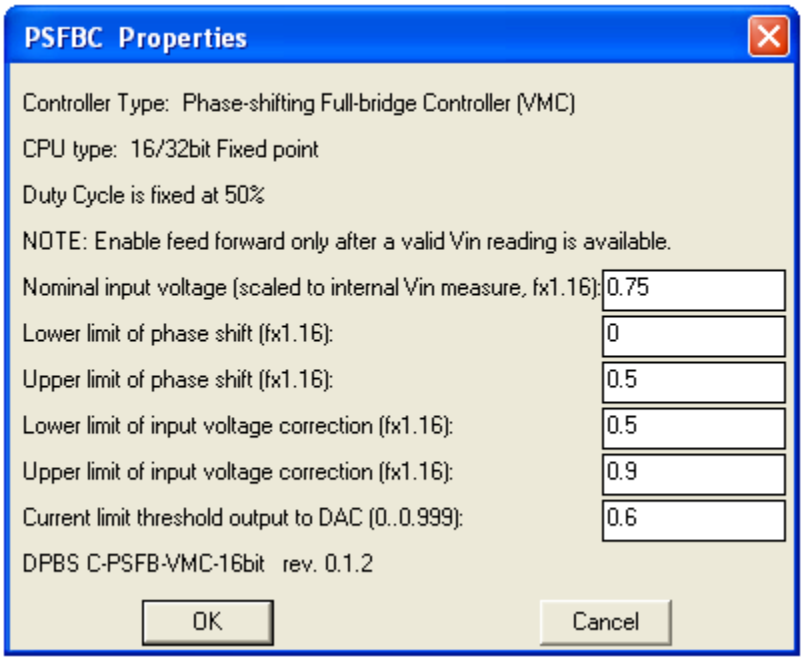
Phase-shifting Full-bridge Voltage Mode Controller (PSFB-VMC)

The phase-shifting full-bridge voltage mode controller operates together with a compensator to control the output voltage of a digital power phase-shifting full-bridge converter.

Input pins:	**Vcorr**	The input signal which is normally connected directly from a compensator block.
	EN_FF	This pin will enable the input voltage feed forward when ≥ 1.
	Vin(t)	The voltage sensing input (negative input to the compensator)
Output pins:	**DC**	This output is simply a fixed 50% duty cycle output which can be connected to two ePWM blocks DC input.
	Phase	The output of the controller which can be connected to one of the two ePWM blocks to control the relative phase between the PWMs.
	CLthres	The current limit threshold value which can be connected to a DAC input.

Dialog properties:

The PSFB-VMC properties menu is shown in the following box which appears when right-clicking on the block



Nominal input voltage:

Enter the value of the nominal input voltage (for input voltage feed-forward) as scaled down and seen by the input of the block at Vin(t).

Lower limit of phase shift:

Enter the lower limit of the phase value for phase-shifting control.

Upper limit of phase shift:

Enter the upper limit of the phase value for phase-shifting control.

Lower limit of input voltage correction:

Enter the lower limit of the input voltage correction for input voltage feed-forward.

Upper limit of input voltage correction:

Enter the upper limit of the input voltage correction for input voltage feed-forward.

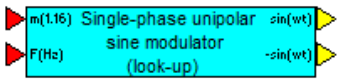
Current limit threshold output to DAC

Enter the current limit threshold value (0 to 1 in this case).

Contents - Codegen

PWM Modulators

This section contains blocks for generating the modulators for SPWM.

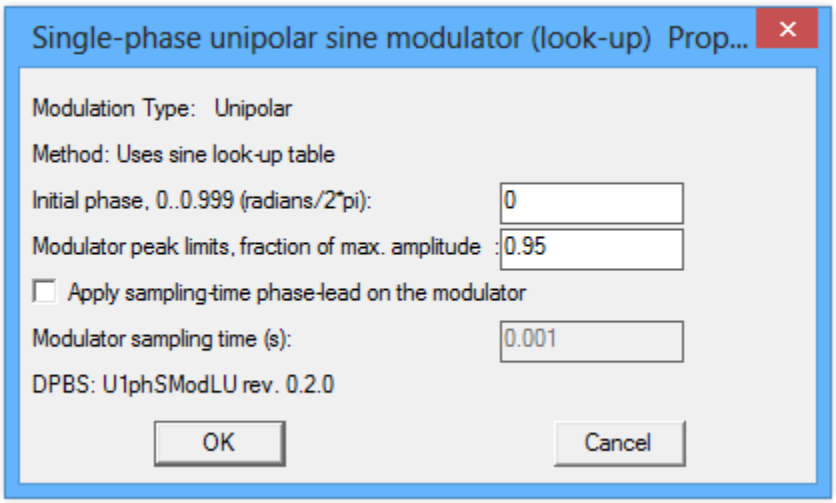


Single-phase Unipolar Sine Modulator

There are several sine-wave modulator blocks in this section and we will describe only one since they are all similar. For a description on the differences between the PWM strategies, see the single-phase SPWM block in the simulation section.

Dialog properties:

The ePWM Interrupt block properties menu is shown in the following box which appears when right-clicking on the block.



Initial phase:

Enter the initial phase of the modulator in radians/2π (0..1).

Modulator peak limits:

Enter a value to limit the peak value of the modulator (0..1).

Apply sampling-time phase-lead on the modulator:

Check this box if the sampling of the modulator waveform is to be compensated with a half-sampling time phase-lead.

Modulator sampling time:

Enter the modulator sampling time in seconds.

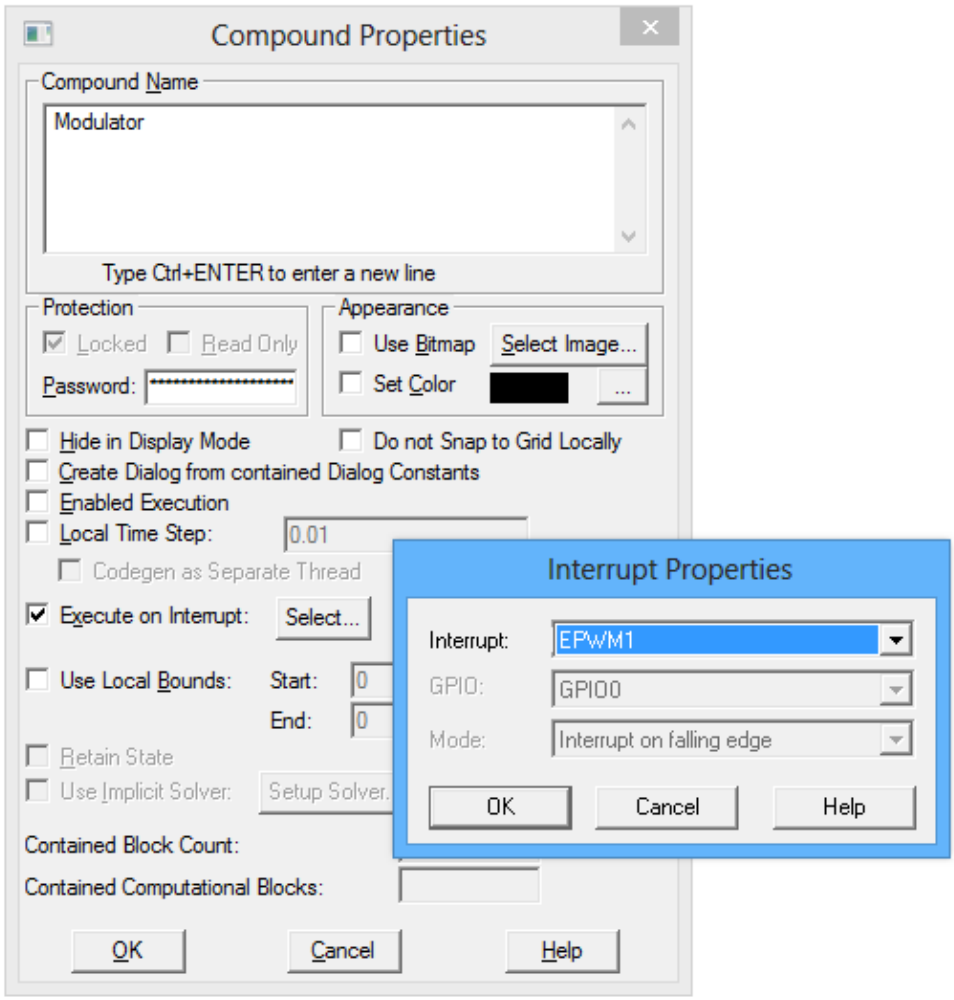
By double-left clicking on this block, one can visualize the following where the modulator blocks can be configured for an interrupt if necessary.

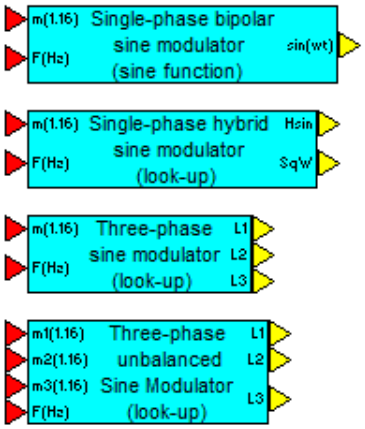
To set the sampling of the modulator synchronous with the carrier:
CTL + right click on this block and tick the checkbox "Execute on Interrupt".
Select the appropriate ePWM module interrupt.



The ePWM interrupt must be set-up as required on the first-pass using the ePWM interrupt block.

Using CTRL + right click, the appropriate ePWM interrupt can be selected as follows:





Other Sine Modulators

There are several sine-wave modulator blocks in this section which include modulators for:

1. Bipolar modulation
2. Unipolar modulation
3. Hybrid modulation
4. Distributed hybrid modulation
5. Three-phase modulation
6. Unbalanced three-phase modulation.

For a description on the differences between the PWM strategies, see the single-phase and three-phase SPWM block descriptions in the simulation section.

Filters



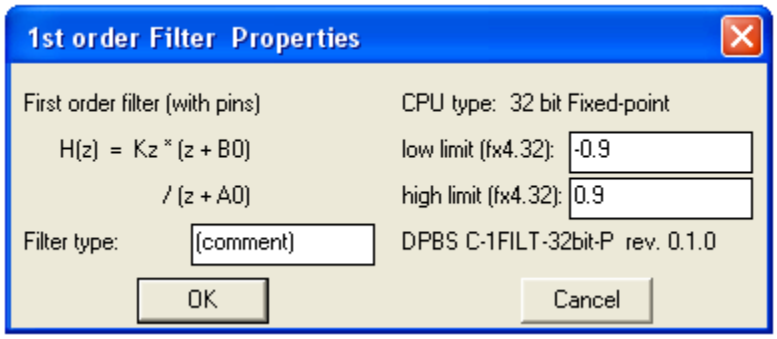
First order filter (with pins)

The first order filter block implements a general first order filter. The type of filter can be set by directly adjusting the coefficients.

Input Pins:	**v(t)**	Input signal.
	Kz	First order filter gain.
	B0	Lowest order numerator coefficient.
	A0	Lowest order denominator coefficient
Output Pins:	**vf(t)**	Filtered output signal

Dialog properties:

The first order filter block properties menu is shown in the following box which appears when right-clicking on the block.



Filter type:

Enter text here to describe the type of filter based upon the coefficients used.

Low limit:

Enter the output low limit of the filter.

High limit:

Enter the output high limit of the filter.



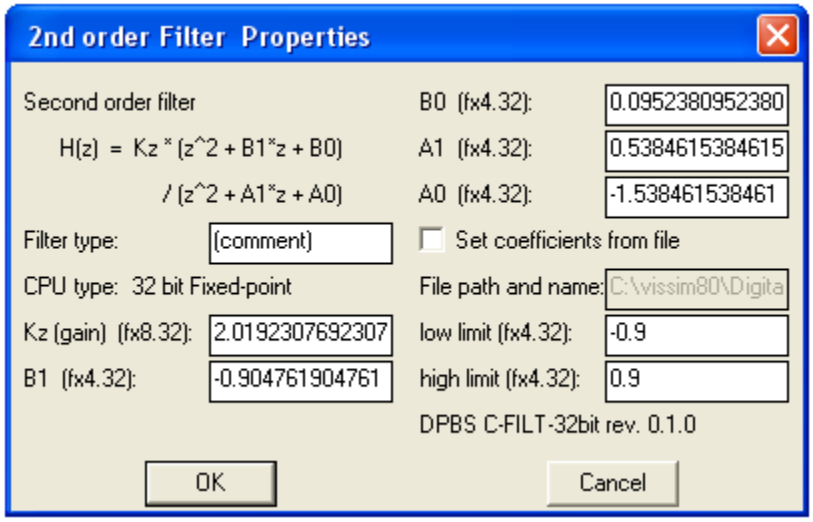
Second order filter

The second order filter block implements a second order discrete filter. The type of filter can be set by directly adjusting the coefficients. Higher order filters can be constructed by connecting together first and second order filter blocks. For designing filters, one can use the transfer function block in the Embed standard block set or analog filters can be converted into digital filters by using the various tools in the tools section of the digital power block set.

Input Pins:	**v(t)**	Input signal.
Output Pins:	**vf(t)**	Filtered output signal.

Dialog properties:

The second order filter block properties menu is shown in the following box which appears when right-clicking on the block.



Filter type:

The choices here are:

Kz (gain):

Enter the DC gain of the compensator.

B1:

Enter the value of the first order numerator coefficient.

B0:

Enter the value of the lowest order numerator coefficient.

A1:

Enter the value of the first order denominator coefficient.

A0:

Enter the value of the lowest order denominator coefficient.

Set coefficients from file:

Check this box to read the coefficients from an external file.

File path and name:

Enter the complete file name and path for the location of the file.

Low limit:

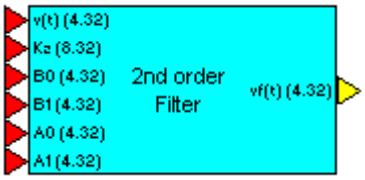
Enter the output low limit of the filter.

High limit:

Enter the output high limit of the filter.

Contents - Codegen

Second order filter (with pins)



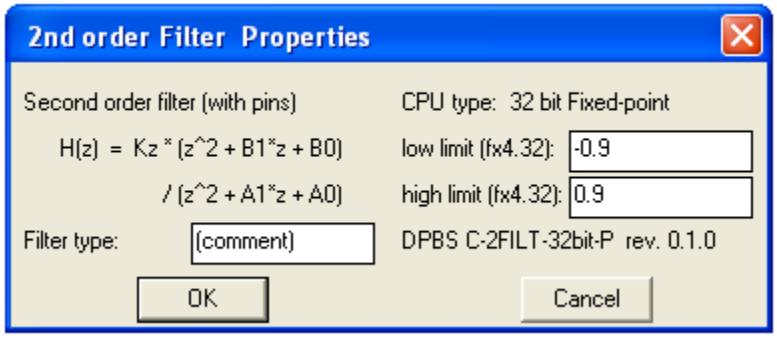
This filter block is identical to the second order filter except that the coefficients can be set with input pins.

Input Pins: **v(t)** Input signal.

Output Pins: **vf(t)** Filtered output signal.

Dialog properties:

The second order filter block properties menu is shown in the following box which appears when right-clicking on the block.



Filter type:

Enter text here to describe the type of filter based upon the coefficients used.

Low limit:

Enter the output low limit of the filter.

High limit:

Enter the output high limit of the filter.

[Contents - Codegen]

Moving average filter



The moving average filter as realized here updates at every time step by sampling the current input and passing the past samples through the filter similar to a FIFO. If the samples are all equal then it is a simple average of the most recent samples.

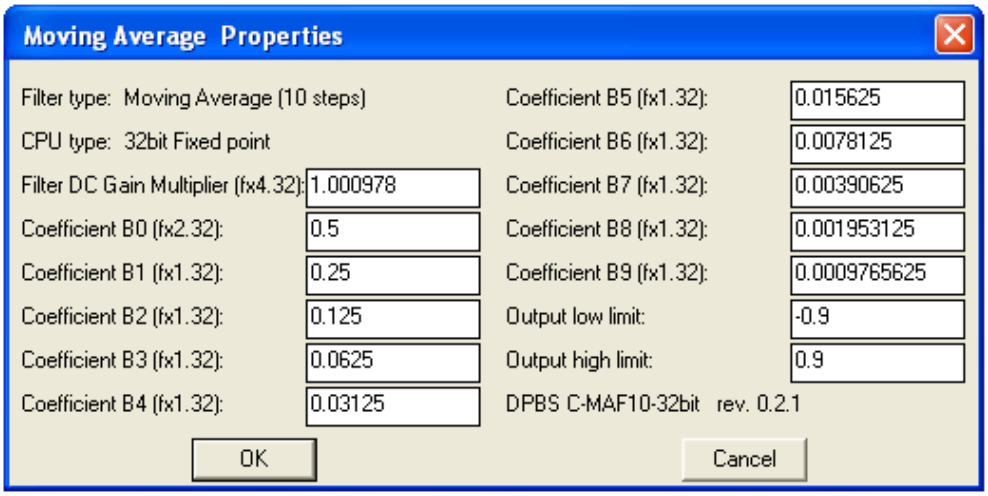
The moving average filter from the simulation section of the digital power block set can be used to generate the coefficients for simple, linear and exponential types of moving average.

Input Pins: **v(t)** Input signal.

Output Pins: **vf(t)** Filtered output signal.

Dialog properties:

The moving average filter block properties menu is shown in the following box which appears when right-clicking on the block.



Filter type:

There are two Moving Average Filter blocks in the block set with filter orders of either 4 or 10 step.

Filter DC Gain Multiplier:

Enter the required DC gain multiplier of the filter. Note that this is not the DC gain of the filter but rather a multiplier to adapt the DC gain.

Coefficient B0:

Enter the multiplier for the current sample.

Coefficient B1:

Enter the multiplier for the past sample.

Coefficient B2:

Enter the multiplier for the z^{-2} sample.

-
-
-

Coefficient B9:

Enter the multiplier for the oldest sample (z^{-9} in this case).

Output low limit:

The output can be limited to this minimum value.

Output high limit:

The output can be limited to this maximum value.

Contents - Codegen



Moving median filter

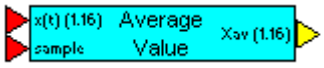
The moving median filter takes the median value of an input sample. In this particular realization, 4 samples are used so that the minimum and maximum values are ignored, leaving the two median values which are then averaged to form the output value. Similar blocks can be found in the Embed main block set under:

blocks → matrix operation → meanSmooth and medianSmooth.

Input Pins:	**In**	Input signal.
Output Pins:	**Out**	Filtered output signal.

[Contents - Codegen]

Measurements



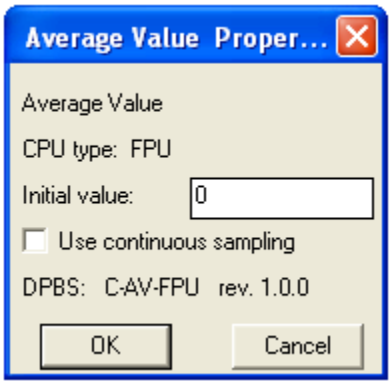
Average Value

This block determines the average value of the input signal between samples. The output value is updated at each sample.

Input Pins:	**x(t)**	Input signal.
	Sample	Connect to a pulse-train block or logic that will produce the required sampling instant(s).
Output Pins:	**Xav(t)**	Average value of the input signal between the last two samples.

Dialog properties:

The average value block properties menu is shown in the following box which appears when right-clicking on the block



Initial value:

Enter the initial value or start value of the averaged output signal.

Use continuous sampling:

If this check box is selected, the block will ignore the sampling instant at the input pin and continuously sample the input value and continuously update the output value.

[Contents - Codegen]



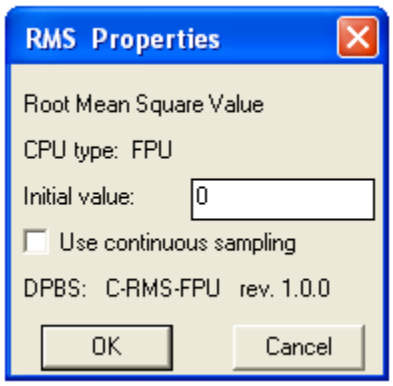
RMS Value

This block calculates the root-mean-square (rms) value of the input signal between the last two sampling instants.

Input Pins:	**x(t)**	Input signal.
	sample	Connect to a pulse-train block or logic that will produce the required sampling instant(s).
Output Pins:	**Xrms(t)**	Rms value of the input signal between the last two samples.

Dialog properties:

The rms value block properties menu is shown in the following box which appears when right-clicking on the block



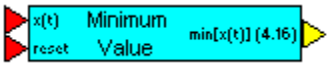
Initial value:

Enter the initial value or start value of the averaged output signal.

Use continuous sampling:

If this check box is selected, the block will ignore the sampling instant at the input pin and continuously sample the input value and continuously update the output value.

Contents - Codegen



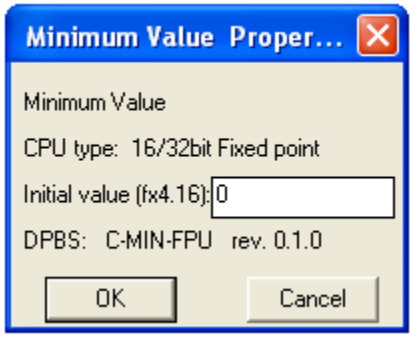
Minimum Value

The minimum value block determines the minimum value of the input signal x(t) until the next reset.

Input Pins:	**x(t)**	Input signal.
	reset	When this input ≥ 1, the current minimum value will be reset and this block will continue sampling the input signal to find a new minimum.
Output Pins:	**min[x(t)]**	The minimum value of x(t) after the last reset.

Dialog properties:

The minimum value block properties menu is shown in the following box which appears when right-clicking on the block



Initial value:

Enter the desired initial value for the minimum value determination.



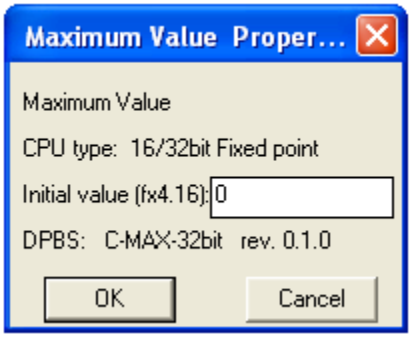
Maximum Value

The maximum value block determines the maximum value of the input signal x(t) until the next reset.

Input Pins:	**x(t)**	Input signal.
	reset	When this input ≥ 1, the current maximum value will be reset and this block will continue sampling the input signal to find a new maximum.
Output Pins:	**max[x(t)]**	The maximum value of x(t) after the last reset.

Dialog properties:

The maximum value block properties menu is shown in the following box which appears when right-clicking on the block



Initial value:

Enter the desired initial value for the maximum value determination.

Contents - Codegen



Real Power

This block will calculate the real power, given the time dependent voltage and current input signals by taking the average value of p(t) where p(t) is given by:

$$p(t) = v(t)*i(t)$$

and then:

$$P = \frac{1}{m}\left(\sum_{k=n}^{n+m} p_k(t)\right)$$

Input Pins: **v(t)** Time-varying voltage input.

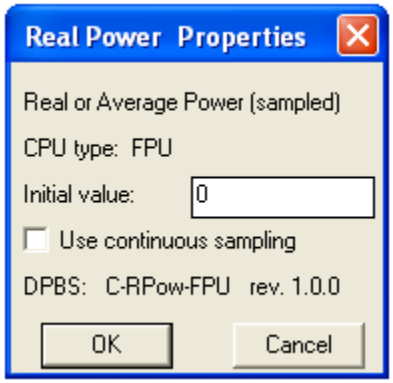
i(t) Time-varying current input.

sample Connect to a pulse-train block or logic that will produce the required sampling instant(s).

Output Pins: **P** The real power output.

Dialog properties:

The real power block properties menu is shown in the following box which appears when right-clicking on the block



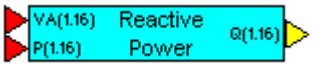
Initial value:

Enter the initial value or start value of the averaged output signal.

Use continuous sampling:

If this check box is selected, the block will ignore the sampling instant at the input pin and continuously sample the input value and continuously update the output value.

Contents - Codegen



Reactive Power

This block will calculate the reactive power, given the apparent power and real power input signals The reactive power is then given by:

$$Q = \sqrt{VA^2 - P^2}$$

Input Pins:	**VA**	Apparent power input.
	P	Real power input.
Output Pins:	**Q**	The reactive power output.



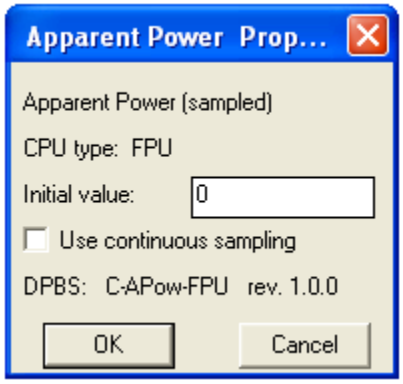
Apparent Power

This block calculates the apparent power based upon the time-varying system voltage and current.

Input Pins:	**v(t)**	Time-varying voltage input.
	i(t)	Time-varying current input.
	sample	Connect to a pulse-train block or logic that will produce the required sampling instant(s).
Output Pins:	**VA**	The apparent power output.

Dialog properties:

The apparent power block properties menu is shown in the following box which appears when right-clicking on the block.

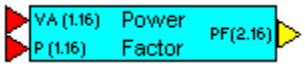


Initial value:

Enter the initial value or start value of the averaged output signal.

Use continuous sampling:

If this check box is selected, the block will ignore the sampling instant at the input pin and continuously sample the input value and continuously update the output value.

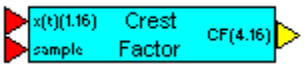


Power Factor

This block calculates the power factor as:

$$PF = \frac{P}{VA}$$

Input Pins:	**VA**	Apparent power input.
	P	Real power input.
Output Pins:	**PF**	The power factor output.



Crest Factor

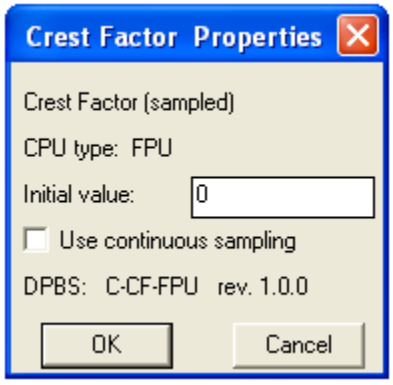
The Crest Factor block measures the crest factor of the input signal. i.e.

$$CF = \frac{\max(x(t))}{Xrms}$$

Input Pins:	**x(t)**	Input signal.
	sample	Connect to a pulse-train block or logic that will produce the required sampling instant(s).
Output Pins:	**CF**	The crest factor of the input signal measured between the last two samples.

Dialog properties:

The crest factor block properties menu is shown in the following box which appears when right-clicking on the block.



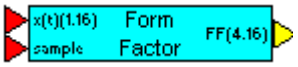
Initial value:

Enter the initial value or start value of the averaged output signal.

Use continuous sampling:

If this check box is selected, the block will ignore the sampling instant at the input pin and continuously sample the input value and continuously update the output value.

Contents - Codegen



Form Factor

The Form Factor block measures the form factor of the input signal. i.e.

$$FF = \frac{\max(x(t))}{Xav}$$

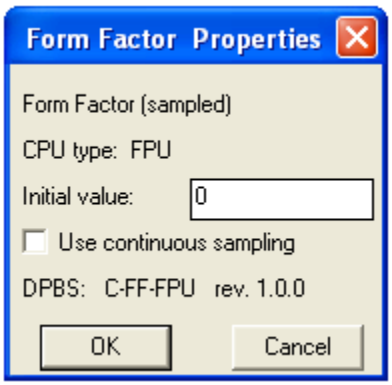
Input Pins: **x(t)** Input signal.

sample Connect to a pulse-train block or logic that will produce the required sampling instant(s).

Output Pins: **FF** The form factor of the input signal measured between the last two samples.

Dialog properties:

The form factor block properties menu is shown in the following box which appears when right-clicking on the block.



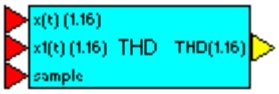
Initial value:

Enter the initial value or start value of the averaged output signal.

Use continuous sampling:

If this check box is selected, the block will ignore the sampling instant at the input pin and continuously sample the input value and continuously update the output value.

Contents - Codegen

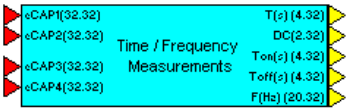


THD

The THD block calculates the THD of a waveform using the following relationship:

$$THD = \frac{\sqrt{x^2(t) - x_1^2(t)}}{x_1(t)}$$

An appropriate filter can be used to determine the fundamental component x1(t) of the measured waveform x(t), however the attenuation of the filter at the given frequency will need to be calculated in order to correct for the true value of the fundamental component.



Time - Frequency

The time-frequency measurement block functions together with an Event Capture block from the simulation section or with an eCAP block from the Embedded menu.

Input Pins: **eCAPx** The captured timer output values of the CAP block (simulation) or eCAP block (under Embedded menu) .

Output Pins: **T(s)** The period of the input signal in seconds, based upon the captured timer values.

DC The duty cycle of the input signal, based upon the captured timer values.

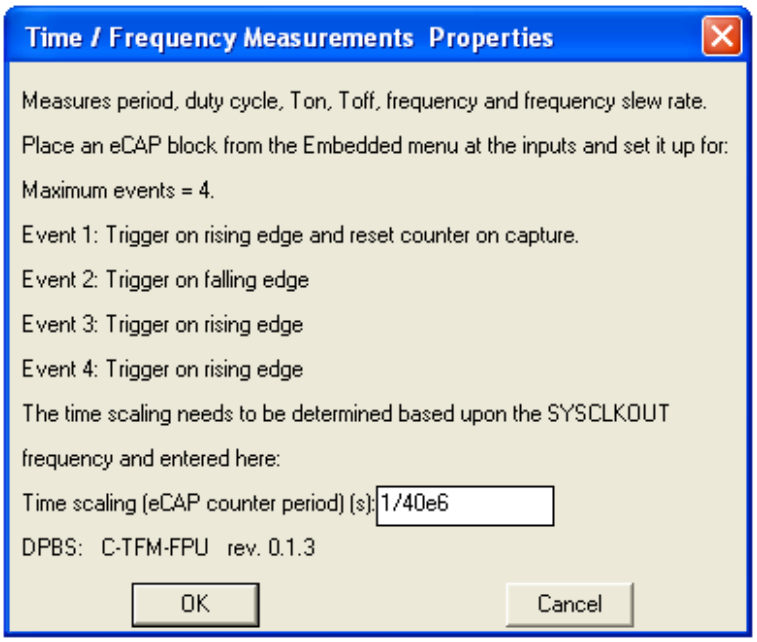
Ton (s) The ON time of the input signal in seconds, based upon the captured timer values.

Toff (s) The OFF time of the input signal in seconds, based upon the captured timer values.

F (Hz) The frequency of the input signal in Hertz, based upon the captured timer values.

Dialog properties:

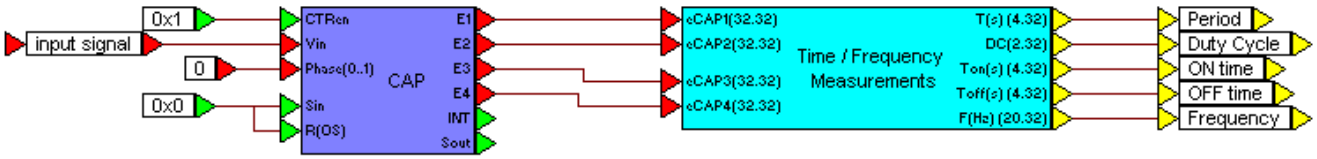
The time-frequency block properties menu is shown in the following box which appears when right-clicking on the block.



Time scaling (eCAP counter period):

Enter the value of the period of the 32-bit counter (1/SYSCLKOUT).

The time-frequency block should be connected as follows in a simulation diagram:



The CAP block must be configured for 4 events as follows:

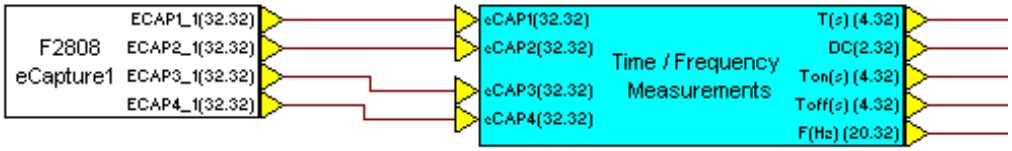
Event 1: Trigger on rising edge and reset the counter on this capture event.

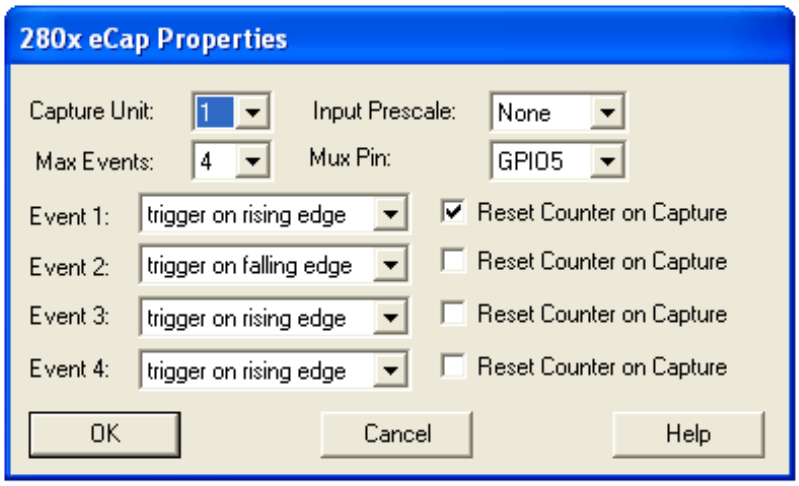
Event 2: Trigger on falling edge.

Event 3: Trigger on rising edge.

Event 4: Trigger on rising edge.

For code generation to a MCU, the time-frequency block should be connected as follows and the eCAP block configured as shown:





The eCAP block must be configured for 4 events identically to the CAP simulation block above.

Contents - Codegen

Background

The background blocks are a series of secondary control blocks which can be configured to run in a background routine, separate from the main Interrupt Service Routine ISR of a digital power control loop.



Soft Start (fixed-point)

Input pins: **Vset** Set point voltage (fx1.16).

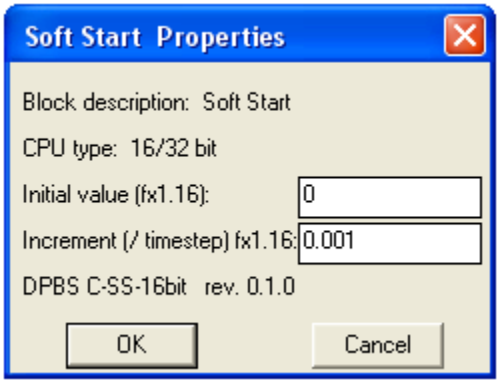
Reset Soft start reset which will set the output back to the initial value. As soon as the reset is released (the value at the pin < 1), the soft start ramp will recommence.

Output pins: **Vout** Vset output voltage including the start start ramp (fx1.16).

SS The value at this pin will be zero when the soft start is active and =1 when the soft start is completed.

Dialog properties:

The soft start block properties menu is shown in the following box which appears when right-clicking on the block.

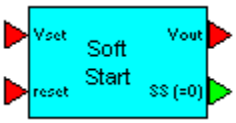


Initial value:

Enter the initial (start) value of the soft start from 0 to 1.

Increment:

Enter the increment value in fx1.16 (from 0 to 0.9999).



Soft start (FPU)

Input pins: **Vset** Set point voltage.

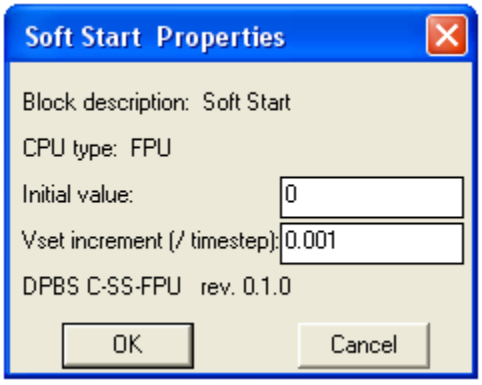
Reset Soft start reset which will set the output back to the initial value. As soon as the reset is released (the value at the pin < 1), the soft start ramp will recommence.

Output pins: **Vout** Vset output voltage including the start start ramp.

	SS	The value at this pin will be zero when the soft start is active and =1 when the soft start is completed.

Dialog properties:

The soft start block properties menu is shown in the following box which appears when right-clicking on the block.



Initial value:

Enter the initial (start) value of the soft start from 0 to 1.

Vset increment:

Enter the increment value from 0 to 1.

Contents - Codegen



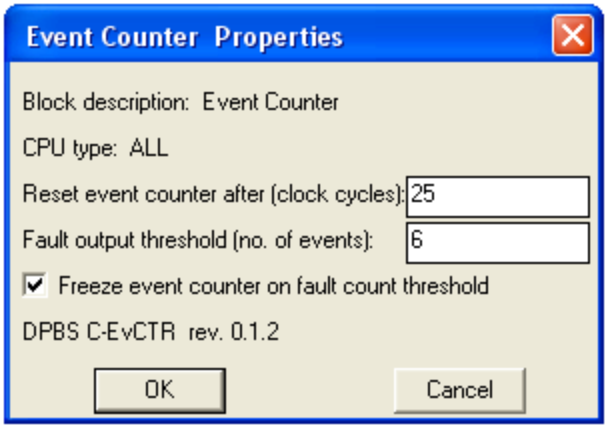
Event Counter

The event counter counts the number of events (rising edge of the input Evt pin) and signals a fault after the specified fault output threshold (number of events). This fault output will be set to 1 until reset by a rising edge at the reset input pin.

Output Pins:	**Evt**	Input event
	CLK	Input clock for timing delays.
	Reset	Reset input pin of the internal event counter.
Output Pins:	**No.**	Number of events
	Fault	Fault output.

Dialog properties:

The event counter properties menu is shown in the following box which appears when right-clicking on the block.



Reset counter after (clock cycles):

Enter the delay time, after which the event counter will be reset to zero. If the fault threshold occurs before this delay time, the event counter will not be reset and the fault output will be set to 1 until reset at the reset input pin.

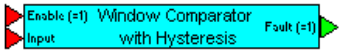
Fault output threshold (no. of events):

Enter the desired number of events which must occur to create a fault output signal.

Freeze event counter on fault count threshold:

If this box is checked the counter will also be frozen on a fault threshold, otherwise it will count continuously.

[Contents - Codegen]



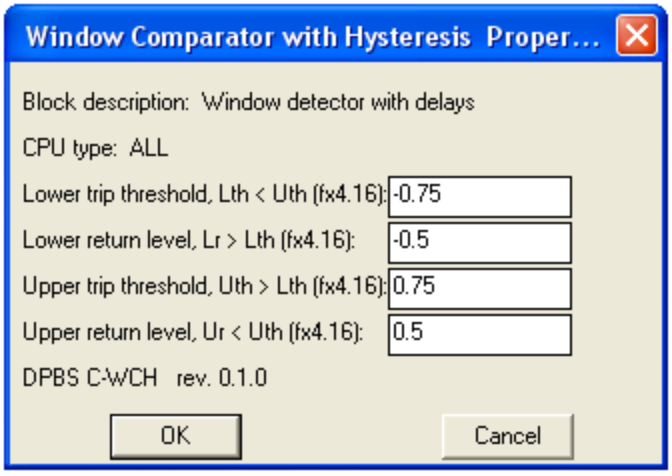
Window Comparator with Hysteresis

The window comparator is a two-level comparator without delay with hysteresis for the return thresholds.

Input Pins:	**Enable**	An enable input (= 1) to enable the comparator.
	Input	The input signal to be monitored.
Output Pins:	**Fault**	The fault output (Fault = 1).

Dialog properties:

The window comparator block properties menu is shown in the following box which appears when right-clicking on the block.



Lower trip threshold:

Enter the desired value of the lower trip level.

Lower return threshold:

Enter the value at which the comparator will return to its normal state after a low level trip (hysteresis value - this value must be greater than the lower trip threshold).

Upper trip threshold:

Enter the desired value of the upper trip level.

Upper return threshold:

Enter the value at which the comparator will return to its normal state after a upper level trip (hysteresis value - this value must be less than the upper trip threshold).



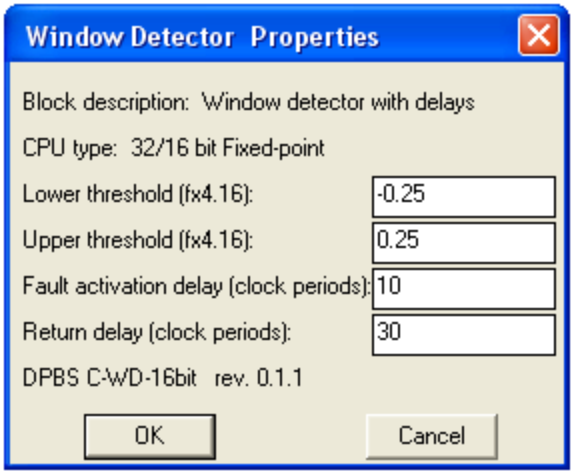
Window detector

This window detector is a window comparator with trip and return delays.

Input Pins:	**Enable**	An enable input (= 1).
	Clock	A clock input which will determine the internal delay times.
	Input	The input signal to be monitored.
	Reset	This pin will reset the window detector after a fault, resetting the delay times to zero.
Output Pins:	**Fault**	The fault condition (Fault = 1).

Dialog properties:

The window detector block properties menu is shown in the following box which appears when right-clicking on the block.



Lower trip threshold:

Enter the desired value of the lower trip level.

Upper threshold:

Enter the desired value of the upper trip level.

Fault activation delay (clock periods):

Enter the delay time of the fault activation. For a fault to be activated (output = 1), the input level must remain outside the trip levels for the duration of this delay.

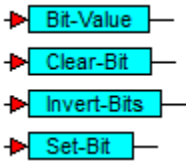
Return delay (clock periods):

Enter the return delay time at which the output will return to normal (= 0). The input level must remain within the two trip levels for the duration of this delay.

Contents - Codegen

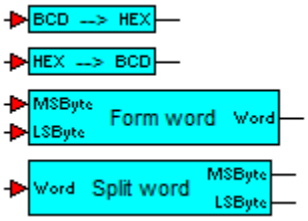
Logic

The logic blocks are a series of blocks to use in normal algorithms used in digital power routines. They are readily-usable blocks which would mostly be used in sections of the diagram separate from the main Interrupt Service Routine ISR of a digital power control loop.



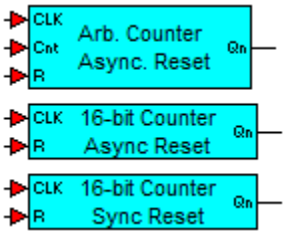
Bit-wise

Blocks which perform bit-wise operations on a selected bit in a nibble, byte, word or long.



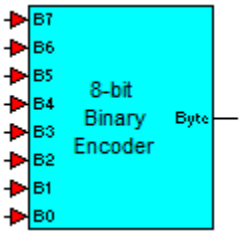
Converters

Blocks which perform conversions on bytes or words.



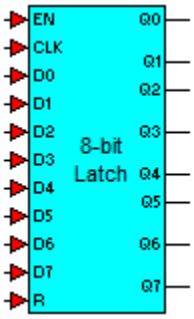
Counters

Different types of counters.



Encoders - Decoders

Many encoders and decoders which are often required in routines.



Latches, Flip-flops

Latches and flip-flops.

Transformations

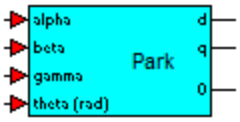
The transformations blocks perform transformations generally required in digital power applications and within the DPD block set.



Clarke

Input Pins: **L1,L2,L3** Three phase input.

Output Pins: **alpha, beta, gamma** Stationary axis frame coordinates.



Park

Input Pins: **L1,L2,L3** Three phase input.

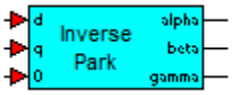
Output Pins: **d, q, 0** The direct-quadrature-zero axis frame coordinates.



Inverse Clarke

Input Pins: **alpha, beta, gamma** Stationary axis frame coordinates.

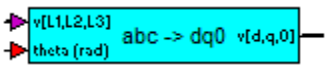
Output Pins: **L1,L2,L3** Three phase output.



Inverse Park

Input Pins: **d, q, 0** The direct-quadrature-zero axis frame coordinates.

Output Pins: **L1,L2,L3** Three phase output.

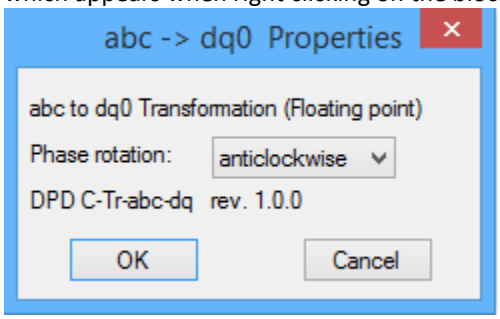


abc to dq0

Input Pins:	v[**L1,L2,L3**]	Three phase input.
	theta	The electrical angle in radians.
Output Pins:	v[**d,q,0**]	The direct-quadrature-zero axis frame coordinates.

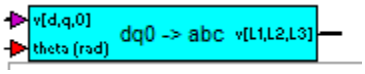
Dialog properties:

The abc to dq0 transformation block properties menu is shown in the following box which appears when right clicking on the block.



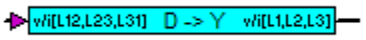
Phase rotation:

Select the phase rotation of the input voltage as clockwise or anticlockwise.



dq0 to abc

Input Pins:	v[**d,q,0**]	The direct-quadrature-zero axis frame coordinates.
	theta	The electrical angle in radians.
Output Pins:	v[**L1,L2,L3**]	Three phase input.

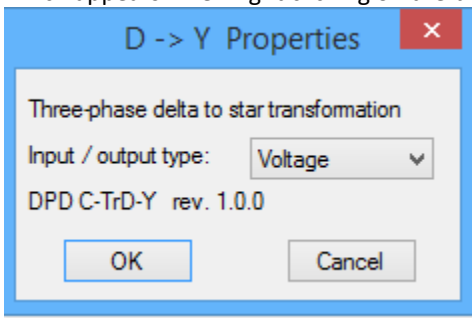


D -Y

Input Pins:	v[**L1,L2,L3**]	Three phase input (delta).
Output Pins:	v[**L1,L2,L3**]	Three phase input (star).

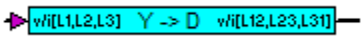
Dialog properties:

The D to Y transformation block properties menu is shown in the following box which appears when right clicking on the block.



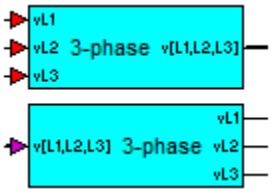
Input / output type:

Select for either voltage or current input / output.



Y - D

Input Pins:	v[**L1,L2,L3**]	Three phase input (star).
Output Pins:	v[**L1,L2,L3**]	Three phase input (delta).

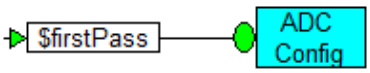


3-phase combine and separate

Basic blocks to transform the vector form of the 3 phases to the 3 phase form and back.

Peripheral Configs and Functional Blocks

This section consists of blocks for directly coding various peripheral functions.

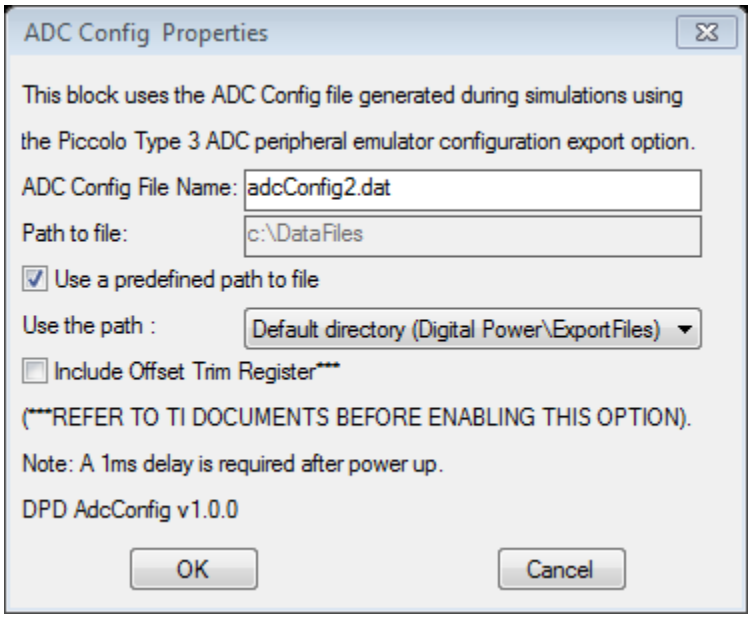


ADC Config (Type 3)

This block can be used with an import file containing the register values for the configuration of the ADC. The configuration import file can be generated by the Piccolo ADC emulator block under MCU peripherals in the simulation section of DPD.

Dialog properties:

The ADC config block properties menu is shown in the following box which appears when right-clicking on the block.



ADC Config file name:

Enter the full file name of the import file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

Select this if the file is located in one of the pre-defined paths.

Use the path:

The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

Include offset trim register:

If the offset trim register is to be written to, then select this option.
Note that this register should NOT be modified unless specifically indicated by Texas Instruments Errata documents. Refer to the appropriate TI documentation before attempting to modify this register.

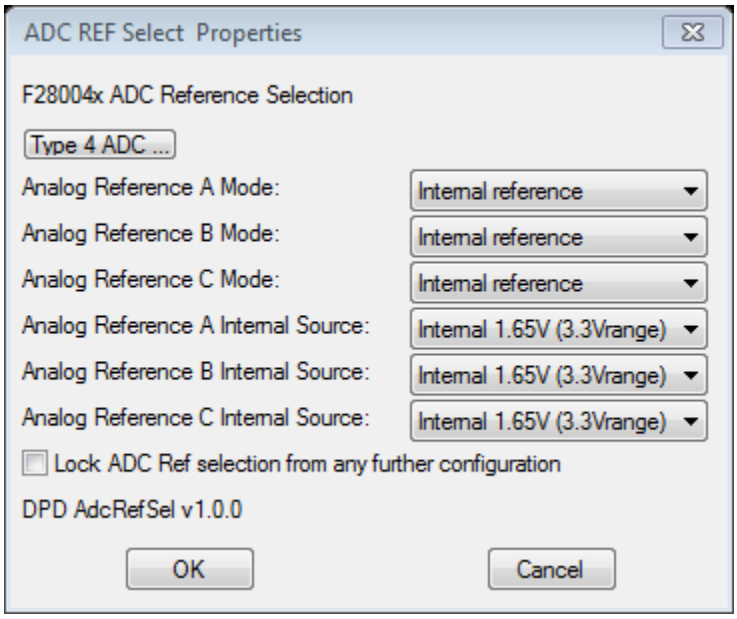


ADC Ref Select (Type 5 ADC: F28004x)

This block can be used to set up the references for the TI C2000 Type 5 ADC (F28004x devices). The F28004x has three internal Type 5 ADCs. Each ADC can have its reference voltage set independently.

Dialog properties:

The ADC Ref Select block properties menu is shown in the following box which appears when right-clicking on the block.



Analog reference A, B and C mode:

Either an internal or an external reference can be selected here. Each ADC reference can be set individually.

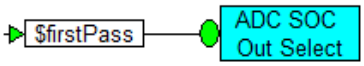
Analog reference A, B and C internal source:

There are two internal references: a 1.65V reference for a 3.3V range of the ADC or a 2.5V reference for a 2.5V range of the ADC.

Lock ADC Ref selection from any further configuration:

Select this if the reference selection is to be locked to prevent any further reconfiguration of the analog reference.

Contents - Codegen

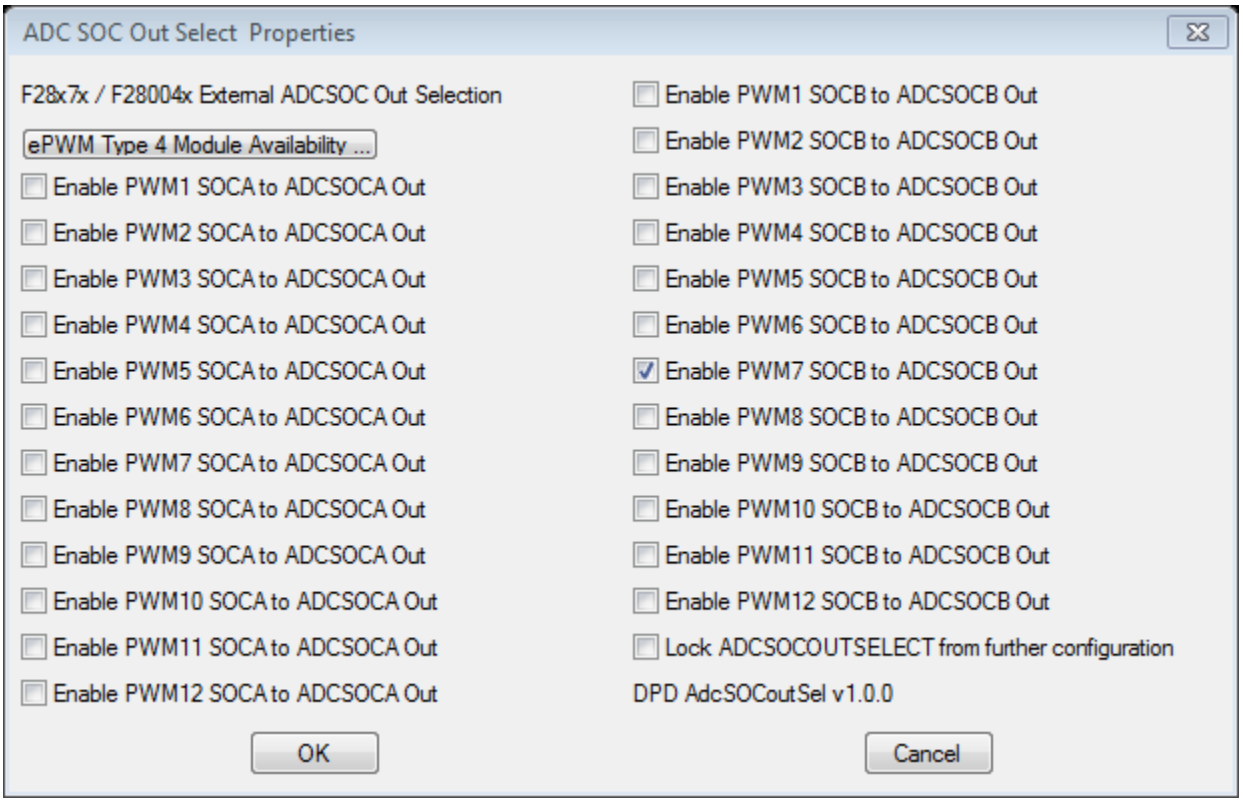


ADC SOC Out Select (Type 4 / 5 ADC)

This block allows the selection of PWM SOCA and SOCB (start of conversion A and B) which can be combined together to form an SOCA and SOCB output respectively.

Dialog properties:

The ADC SOC Out Select block properties menu is shown in the following box which appears when right-clicking on the block.

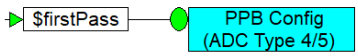


Enable PWMx SOCA to ADCSOCA Out:

Select each PWM module's SOCA which will be combined for an ADCSOCA output.

Enable PWMx SOCB to ADCSOCB Out:

Select each PWM module's SOCB which will be combined for an ADCSOCB output.

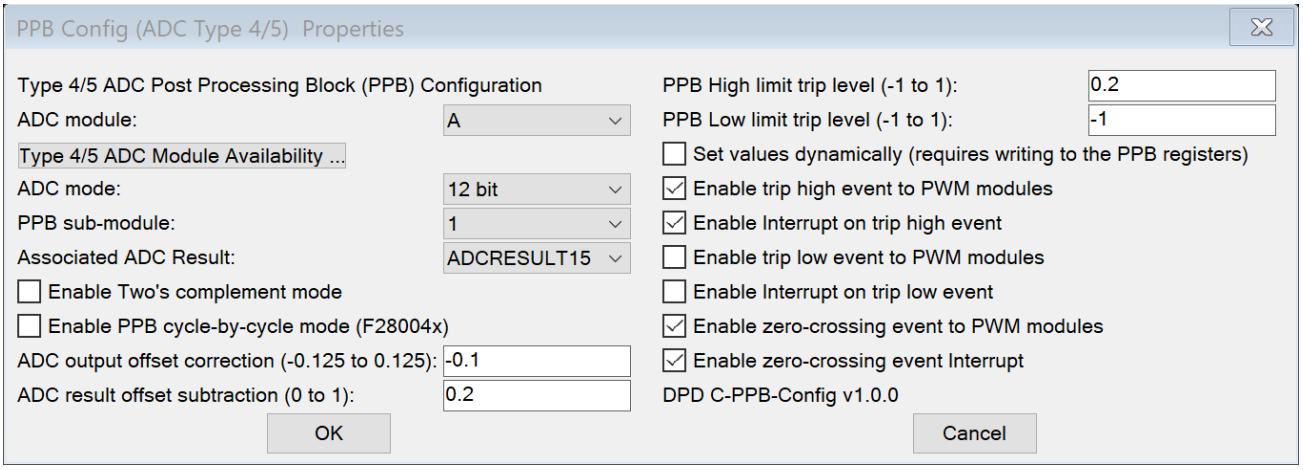


ADC PPB Config (Type 4 / 5 ADC)

This block performs the configuration of the ADC Post Processing Blocks (PPB). The PPB submodule allows subtracting offsets and configuring events directly on ADC results in the hardware so that they do not need to be performed in the control software. The results of the post processing blocks are written into dedicated PPB register which can be read using the ADC PPB Result Read block.

Dialog properties:

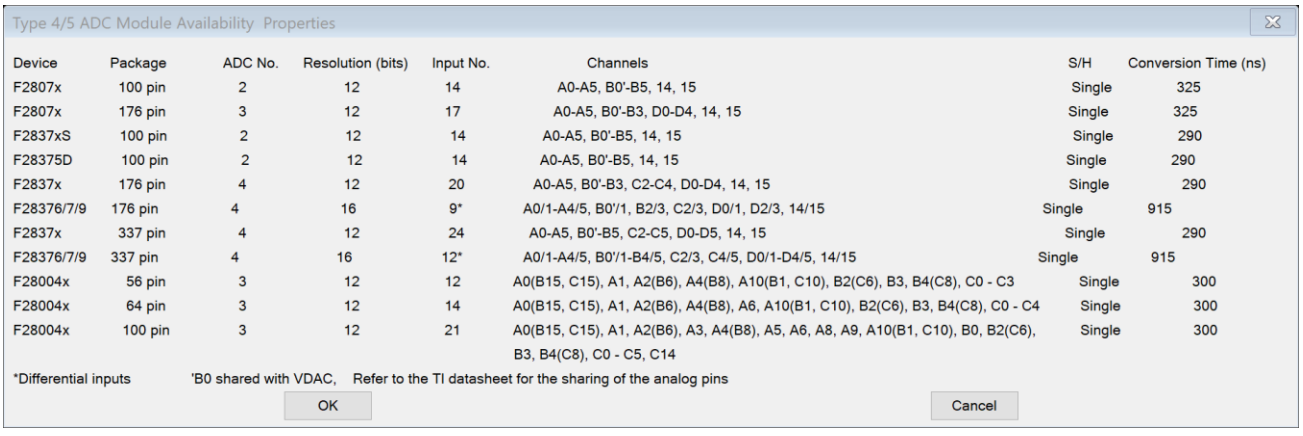
The ADC PPB Config block properties menu is shown in the following box which appears when right-clicking on the block.



ADC Module:

Select each PWM module's SOCA which will be combined for an ADCSOCA output.

Type 4 / 5 ADC module availability:



ADC mode:

Select 12-bit or 16-bit (only F28x7x) mode.

PPB Sub-module:

Select the PPB submodule from 1 to 4 of this ADC module.

Associated ADC Result:

Select the corresponding SOC / EOC /ADCRESULT for this configuration of the ADC PPB submodule.

Enable Two's complement mode:

This option will enable a two's complement conversion in hardware before storing the value in the PPB result register.

If disabled: PPBresult = ADCresult - OffRef

If enabled: PPBresult = OffRef - ADCresult

Enable PPB cycle-by-cycle mode:

When cycle-by-cycle mode (CBC) is enabled, the ADC event status will automatically be cleared when the event condition is no longer present.

ADC output offset correction (-0.125 to 0.125):

This correction factor is usually a one-time correction in order to correct for any hardware offset into the ADC channel. The value is normalised to 1 with respect to the current ADC VREFHI value.

ADC Result Offset Subtraction (0 to 1):

The value here will be subtracted from the ADCRESULT value. This is normally used to remove any offset from the ADC value such as with bipolar input signals. This offset can also be written to dynamically using the ADC PPB Offset Write Block. The value is normalised to 1 with respect to the current ADC VREFHI value.

PPB High Limit Trip Level:

Enter the value of the high trip level on this PPB result. The value is normalised to 1 with respect to the current ADC VREFHI value.

PPB Low limit trip Level:

Enter the value of the low trip level on this PPB result. The value is normalised to 1 with respect to the current ADC VREFHI value.

Set values dynamically:

Select this if the above offsets and trip levels are to be set dynamically in a diagram or not set at all.

Enable trip high event to PWM modules:

Select to enable the trip high event to be directly available to the EPWM modules.

Enable Interrupt on trip high event:

Select to enable an interrupt on the trip high event.

Enable trip low event to PWM modules:

Select to enable the trip low event to be directly available to the EPWM modules.

Enable Interrupt on trip low event:

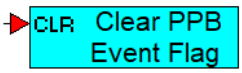
Select to enable an interrupt on the trip low event.

Enable zero-crossing event to PWM modules:

Select to enable the zero-crossing event to be directly available to the EPWM modules.

Enable Interrupt on zero-crossing event:

Select to enable an interrupt on the zero-crossing event.

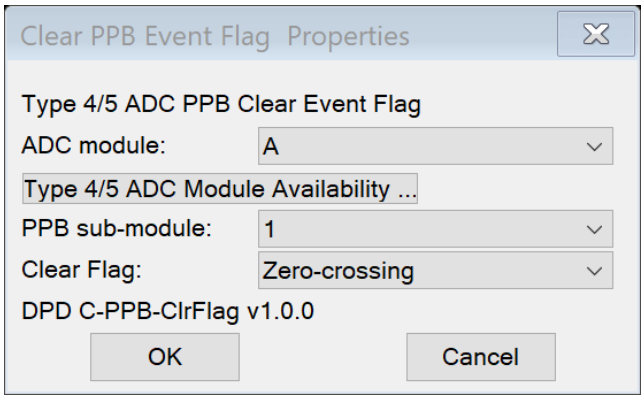


ADC PPB Event Flag Clear (Type 4 / 5 ADC)

This block allows clearing any PPB event flags. The ADC PPB Config block must be placed in the diagram and set for the PPB submodule given here.

Dialog properties:

The ADC PPB Event Flag Clear properties menu is shown in the following box which appears when right-clicking on the block.



ADC Module:

Select the ADC module to which this PPB block corresponds and as has been configured.

Type 4 / 5 ADC module availability:

As shown in the ADC PPB Config block above.

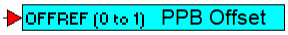
PPB Sub-module:

Select the ADC PPB submodule from 1 to 4.

Clear Flag:

The choices here are:

1. None
2. Trip High
3. Trip Low
4. Trip High and trip Low
5. Zero crossing
6. Zero crossing and Trip High
7. Zero crossing and Trip Low
8. All three Flags.

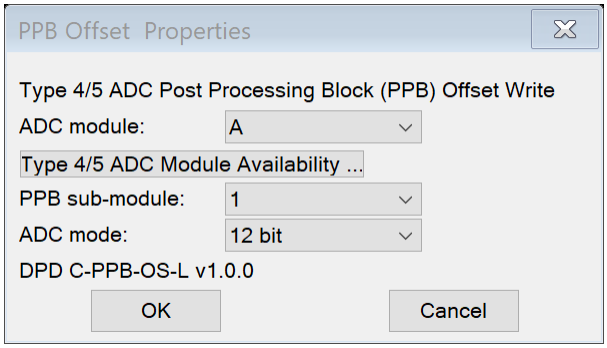


ADC PPB Offset Write (Type 4 / 5 ADC)

This block allows writing to the offset register in the ADC Post Processing blocks in order to add an offset to any ADC inputs. The ADC PPB Config block must be placed in the diagram and set for the PPB submodule given here.

Dialog properties:

The ADC Offset Write block properties menu is shown in the following box which appears when right-clicking on the block.



ADC Module:

Select the ADC module to which this PPB block corresponds and as has been configured.

Type 4 / 5 ADC module availability:

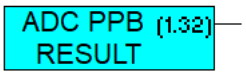
As shown in the ADC PPB Config block above.

PPB Sub-module:

Select the ADC PPB submodule from 1 to 4.

ADC mode:

Select 12-bit or 16-bit (only F28x7x) mode.

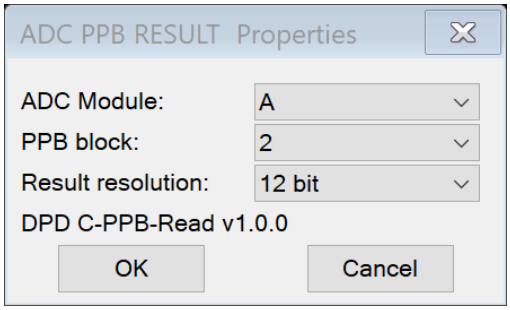


ADC PPB Result Read (Type 4 / 5 ADC)

This block allows reading the ADC Post Processing Block registers. The ADC PPB Config block must be placed in the diagram and set for the PPB submodule given here.

Dialog properties:

The ADC PPB Result Read Block properties menu is shown in the following box which appears when right-clicking on the block.



ADC Module:

Select the ADC module to which this PPB block corresponds and as has been configured.

Type 4 / 5 ADC module availability:

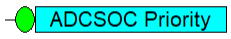
As shown in the ADC PPB Config block above.

PPB Sub-module:

Select the ADC PPB submodule from 1 to 4.

Result resolution:

Select 12-bit or 16-bit (only F28x7x) resolution.

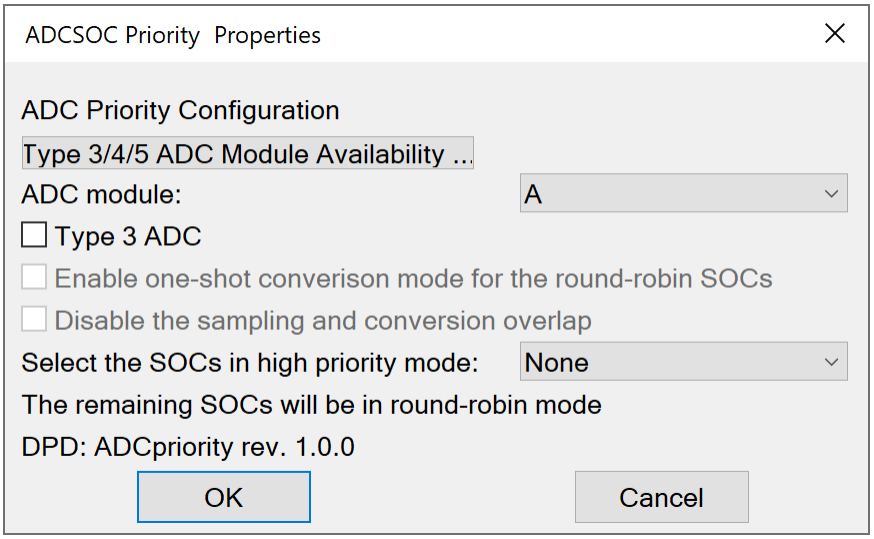


ADC SOC Priority

This block allows the configuration of the ADC sampling/conversion priority. The SOCs that are in round-robin mode and those that are in high-priority mode can be set with this configuration block.

Dialog properties:

The ADC SOC priority Block properties menu is shown in the following box which appears when right-clicking on the block.



ADC Module:

Select the ADC module to which this PPB block corresponds and as has been configured.

Type 3 ADC:

Select this for a type 3 ADC (Piccolo 280x, Concerto).

Enable one-shot conversion mode for the round-robin SOCs:

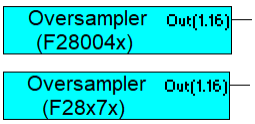
In this mode the conversion will be performed once for each SOC trigger.

Disable the sampling and conversion overlap:

If disabled, there will be no time overlap between the ADC sampling and the ADC conversion. The sampling of the next ADC channel (SOC) will only be performed after the ADC conversion of the previous SOC has been completed.

Select the SOCs in high-priority mode:

Select the SOC in high priority mode starting from the lowest number SOC. These SOCs will be sampled first if simultaneous ADC SOC triggers are received.



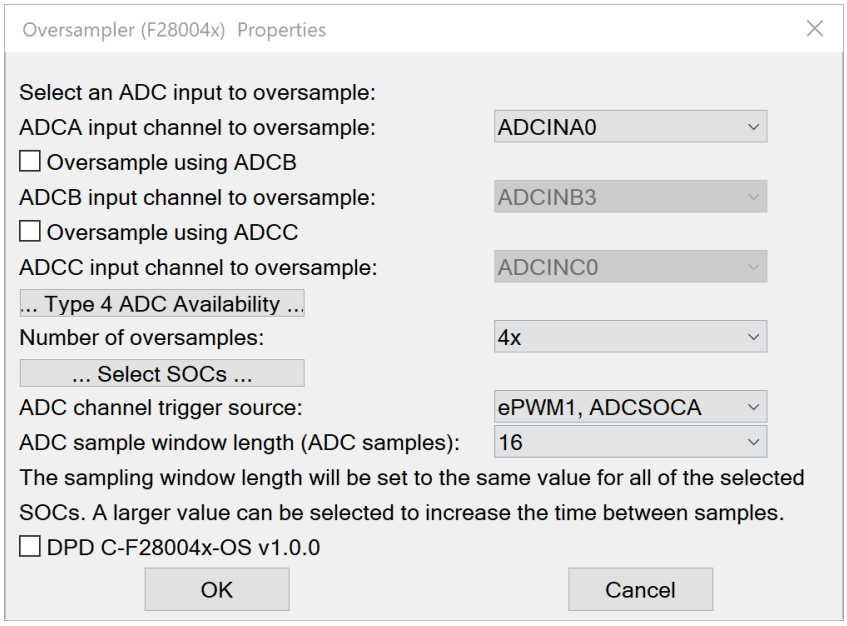
ADC Oversampler

This block allows setting up the ADC in conjunction with the ADC config, in order to oversample an input channel to the ADC sampler. The oversampling technique assigns any available SOCs to the sampling of the desired channel. These SOCs must be available and not used by other channels. This requirement is generally satisfied for the devices with multiple internal ADCs since each ADC has 16 SOCs available.

If another input channels is required to be oversampled, insert a second block into the diagram. If the channels are required to be sampled simultaneously, insert a simultaneous oversampling block (for F280x).

Dialog properties:

The ADC oversampling Blocks properties menu is shown in the following box for the F28004x, which appears when right-clicking on the block.



ADCA input channel to oversample:

Select the ADC input channel to be oversampled (ADCA).

ADCA input channel to oversample:

Or select from ADCB.

Number of oversamples:

Select the number of times to oversample the ADC channel from 2 to 16. Note that there must be sufficient SOCs available and not in use by another channel, in order to perform the number of oversamples.

Select SOCs:

The SOCs must be selected for the number of oversamples. The number of selected SOCs must equal the oversample number.

ADC channel trigger source:

Select the trigger source for the ADC channel to be oversampled. This will override the normal ADC configuration.

ADC sample window length:

Select the sampling window time in ADC samples (will be valid for all SOCs).

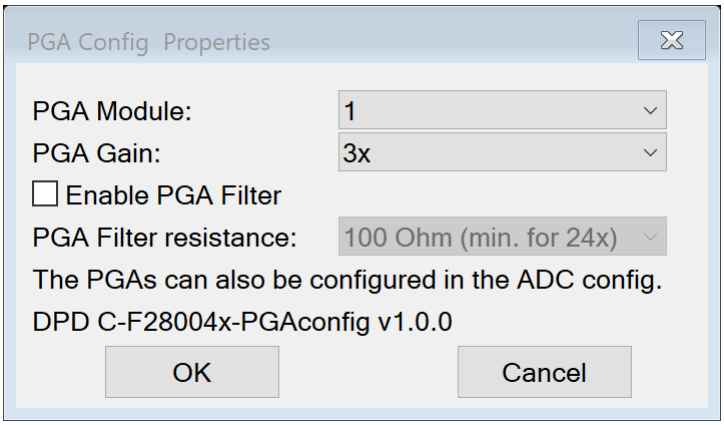


PGA Config

This block allows the configuration of the programmable gain amplifiers (PGA) in the analog front end (AFE) of the C2000.

Dialog properties:

The PGA config Block properties menu is shown in the following box which appears when right-clicking on the block.



PGA Module:

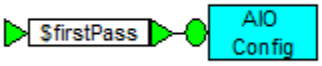
Select the PGA module to configure.

PGA gain:

Select the desired PGA gain of the analog input signal.

PGA filter resistance:

If the filtered PGA output is to be used, select the desired filter resistance.



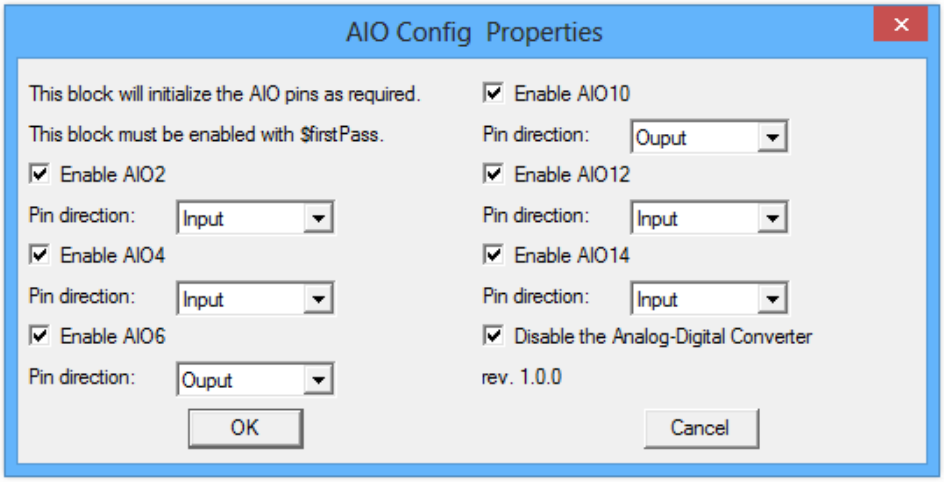
AIO Config (280x)

Where there are analog ADC inputs free and there is a need for more digital I/O, the AIO ports can provide additional inputs or outputs.

This configuration block should be placed in a diagram if the AIO ports are desired to be used. The block can be enabled on the first pass (executed once only at the start of a routine) as is the default case or it may be enabled at any time during a diagram execution to change the port configuration.

Dialog properties:

The AIO config block properties menu is shown in the following box which appears when right-clicking on the block.



Enable AIOx:

Select any of these boxes to enable the appropriate AIO port.

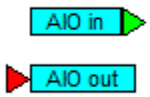
Pin direction:

The pin direction can be selected as input or output.

Disable the Analog-Digital Converter:

If the ADC is not used at all, then it can be disabled by checking this box.

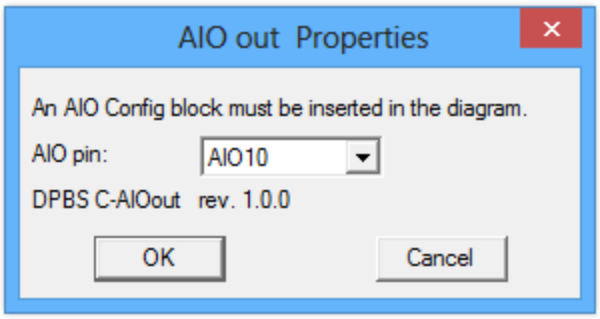
[Contents - Codegen]



AIO in / out

Dialog properties:

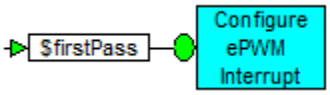
The AIO in / out blocks properties menu is shown in the following box which appears when right-clicking on the block.



AIO pin:

For the piccolo microcontrollers, one can select from the 6 available AIO ports.

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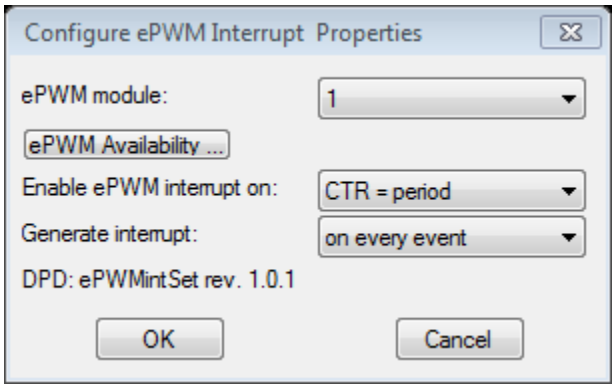
Configure ePWM Interrupt

This block can be used additionally to the normal interrupt setup of a compound block.

This configuration block should be placed in a diagram if an ePWM interrupt is required and the interrupt must be activated on anything other than the default of counter equals zero.

Dialog properties:

The ePWM interrupt block properties menu is shown in the following box which appears when right-clicking on the block.



ePWM unit:

Select the ePWM unit which should generate the desired interrupt.

ePWM Availability:

Shows the ePWM module availability for each device and package type.

Enable ePWM interrupt on:

The choices here are:

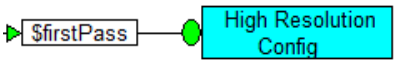
1. No action (reserved) – not a valid choice since the block would not be required in this case.
2. CTR = 0 - Generate an interrupt when the counter reaches zero.

3. CTR = Period – Generate an interrupt when the counter reaches the period value.
4. CTR = 0 or Period - Generate an interrupt when the counter reaches zero value or the period value.
5. CMPA up – Generate an interrupt when the counter equals the DCA input on the up count.
6. CMPA down – Generate an interrupt when the counter equals the DCA input on the down count.
7. CMPB up – Generate an interrupt when the counter equals the DCB input on the up count.
8. CMPB down – Generate an interrupt when the counter equals the DCB input on the down count.

Generate interrupt:

The interrupt can be generated on every event, every second event of every third event with this option.

Also refer to the Single-phase Unipolar Sine Modulator block description for setting up the interrupt.

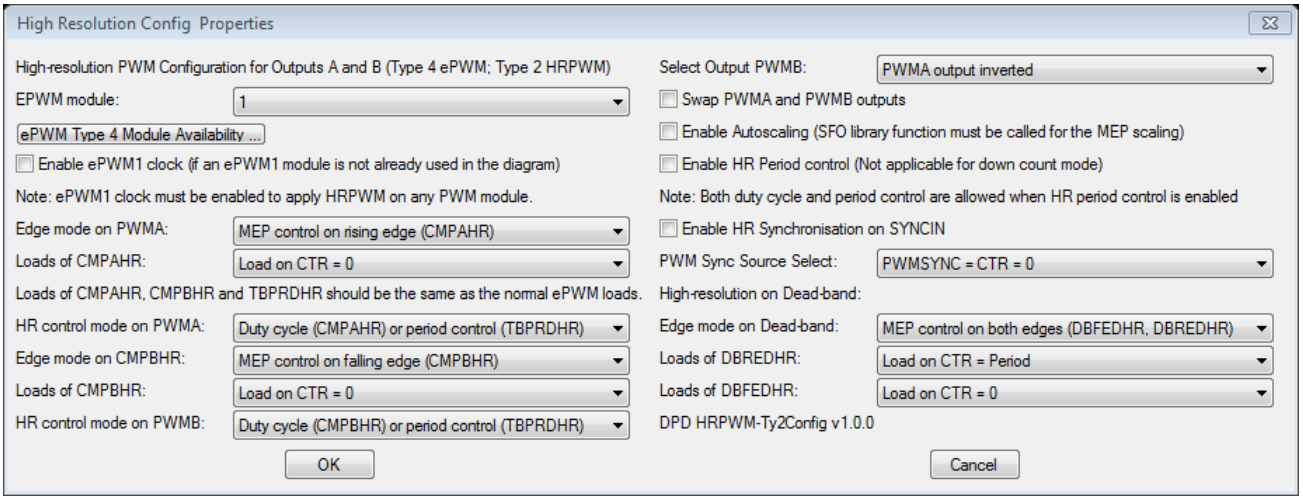


HRPWM Config

This block can be used to completely configure the High-resolution PWM and it should be used in conjunction with the high-resolution option in each PWM module embedded block. The block uses the additional configurations of the Type 4 ePWM.

Dialog properties:

The HRPWM Config block properties menu is shown in the following box which appears when right-clicking on the block.



ePWM module:

Select the ePWM module for the HR configuration.

ePWM Type 4 Availability:

Shows the ePWM module availability for each device and package type.

Enable ePWM1 clock:

All HRPWMs are clocked on the ePWM clock of the ePWM1 module. If this module is not already used within a diagram, then the clock should be enabled here.

Edge mode on PWMA:

The selection here is:

1. High resolution disabled on PWMA
2. MEP control on rising edge (CMPAHR)
3. MEP control on falling edge (CMPAHR)
4. MEP control on rising and falling edge (TBPHSHR or TBPRDHR)

Selections 2 and 3 are for normal duty cycle control using HRPWM, while selection 4 is for variable frequency control with HRPWM.

Loads of CMPAHR:

The selections available here for the moment of loading the CMPAHR register are:

1. Load on counter = 0.
2. Load on counter = Period.
3. Load on counter = 0 or Period.

The register loading configuration here should be set identically to that of the corresponding normal PWM register loading.

HR control mode on PWMA:

The selections available here are:

1. Duty cycle (CMPAHR) or period (TBPRDHR)
2. Phase control (TBPHSHR).

Edge mode on PWMB:

The selection here is:

1. High resolution disabled on PWMB
2. MEP control on rising edge (CMPBHR)
3. MEP control on falling edge (CMPBHR)
4. MEP control on rising and falling edge (TBPHSHR or TBPRDHR)

Selections 2 and 3 are for normal duty cycle control using HRPWM, while selection 4 is for variable frequency control with HRPWM.

Loads of CMPBHR:

The selections available here for the moment of loading the CMPBHR register are:

1. Load on counter = 0.
2. Load on counter = Period.
3. Load on counter = 0 or Period.

The register loading configuration here should be set identically to that of the corresponding normal PWM register loading.

HR control mode on PWMB:

The selections available here are:

1. Duty cycle (CMPBHR) or period (TBPRDHR)
2. Phase control (TBPHSHR).

Select output PWMB:

The selections available here are:

1. PWMB output
2. PWMA output inverted.

Swap PWMA and PWMB outputs:

Checking this option will swap the PWMA and PWMB outputs.

Enable autoscaling:

Check this option to enable autoscaling of the MEP function. The TI SFO needs to be called and this will be performed if the HR option is checked in the embedded ePWM block.

Enable HR period control:

Checking this option will enable period control with HRPWM. This is not valid when using only down count mode of the PWM. With this option checked, both duty cycle and period control can be performed when using HRPWM.

Enable HR synchronisation on SYNCIN:

Check this to enable high-resolution synchronisation using the SYNCIN signal event.

PWM sync source select:

The selections available here are:

1. PWMSYNC on CTR = Period
2. PWMSYNC on CTR = 0
3. PWMSYNC on CMPC Up
4. PWMSYNC on CMPC Down
5. PWMSYNC on CMPD Up
6. PWMSYNC on CMPD Down

High-resolution on Dead-band:

Edge mode on dead-band:

The selections available here are:

1. Dead-band on HRPWM disabled
2. MEP control on rising edge (DBREDHR)
3. MEP control on falling edge (DBFEDHR)
4. MEP control on both rising edge and falling edge (DBREDHR and DBFEDHR)

PWMSYNC Loads of DBREDHR:

The selections available here for the moment of loading the DBREDHR register are:

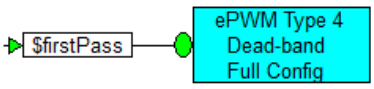
1. Load on counter = 0.
2. Load on counter = Period.
3. Load on counter = 0 or Period.

Loads of DBFEDHR:

The selections available here for the moment of loading the DBFEDHR register are again:

1. Load on counter = 0.
2. Load on counter = Period.
3. Load on counter = 0 or Period.

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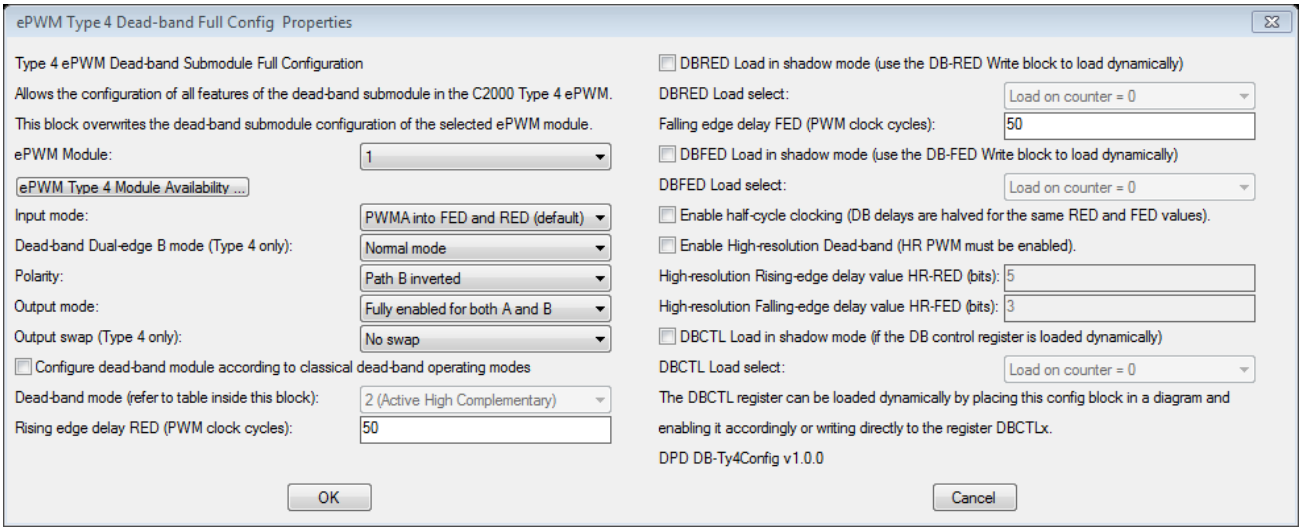
Dead-band Full Config (ePWM Type 4)

This block can be used to completely configure the TI C2000 Type 4 ePWM dead-band sub-module.

A corresponding ePWM block from the embedded menu for the C2000 target support must be placed in the diagram.

Dialog properties:

The Dead-band Full Config block properties menu is shown in the following box which appears when right-clicking on the block.



ePWM module:

Select the ePWM module to be configured for dead-band.

Input mode:

The selections available here are:

1. PWMA into FED and RED
2. PWMB into RED, PWMA into FED
3. PWMB into FED, PWMA into RED
4. PWMB into RED and FED

Dead-band Dual-edge B mode:

The selections available here are:

1. Normal mode
2. RED and FED applied to path B.

Polarity:

The selections available here are:

1. No inversion on Path A or B
2. Path B inverted, Path A not inverted
3. Path A inverted, Path B not inverted
4. Both paths A and B inverted

Output mode:

The selections available here are:

1. Both paths bypassed (dead-band is disabled from output)
2. Falling edge delay on PWMB; PWMA is not delayed
3. Rising edge delay on PWMA; PWMB is not delayed
4. Fully enabled for both A and B

Output Swap:

The selections available here are:

1. No swapping
2. Output B is swapped
3. Output A is swapped
4. Both outputs swapped

Configure dead-band module according to classical dead-band operating modes:

If selected, the dead-band can be configured for the following modes:

Dead-band mode:

1. Fully bypassed
2. Active high complementary
3. Active low complementary
4. Active High
5. Active Low
6. Refer to the table in the TI documentation and given internally for viewing in this block.
7. Refer to the table in the TI documentation and given internally for viewing in this block.

Rising edge delay, RED (pwm clock cycles):

Enter the value of the rising-edge delay (RED) in PWM clock cycles.

DBRED Load in shadow mode:

The dead-band value can be selected to be loaded in shadow mode.

DBRED Load in shadow mode:

The selections here are:

1. Load on counter = 0.
2. Load on counter = Period.
3. Load on counter = 0 or Period.
4. Freeze (no loads).

Falling edge delay, FED (pwm clock cycles):

Enter the value of the falling-edge delay (FED) in PWM clock cycles.

DBFED Load in shadow mode:

The dead-band value can be selected to be loaded in shadow mode

DBFED Load in shadow mode:

Again the selections here are:

1. Load on counter = 0.
2. Load on counter = Period.
3. Load on counter = 0 or Period.
4. Freeze (no loads).

Enable half-cycle clocking:

Enables double-resolution of the dead-band delay clocking. In this case, the value for RED and FED above must be doubled for the same delay time. This must be enabled for high-resolution dead-band.

Enable High-resolution dead-band:

This option will enable high-resolution dead-band.

High-resolution rising-edge delay value HR-RED:

Enter the value of the high-resolution part of the rising-edge delay

High-resolution falling-edge delay value FR-RED:

Enter the value of the high-resolution part of the falling-edge delay

DBCTL load in shadow mode:

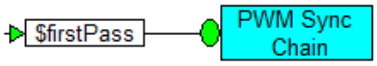
The dead-band configuration register can be loaded in shadow mode.

DBCTL load select:

Again the selections here are:

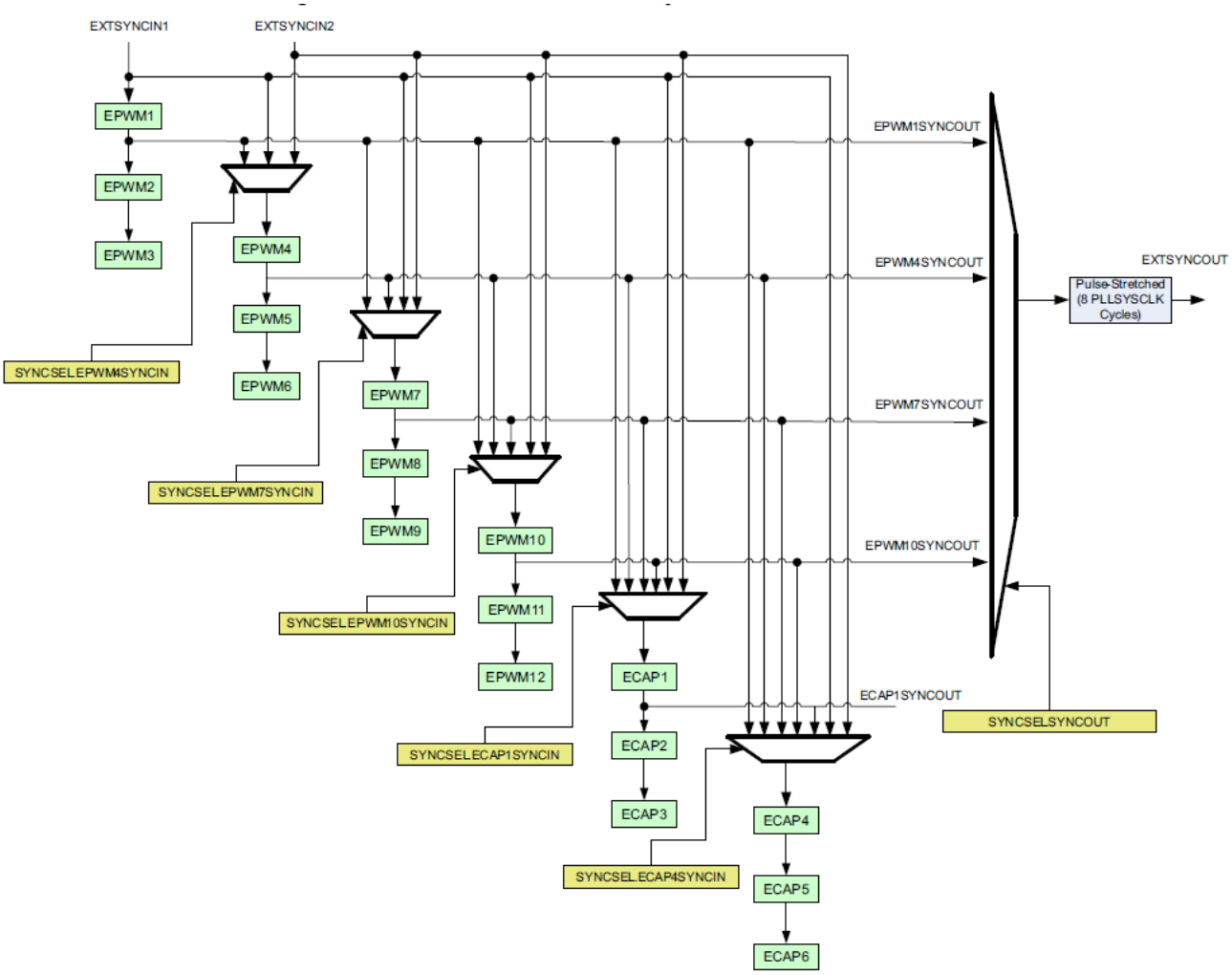
1. Load on counter = 0.

2. Load on counter = Period.
3. Load on counter = 0 or Period.
4. Freeze (no loads).



PWM Sync Chain

This block can be used to configure the TI C2000 ePWM and eCAP PWM synchronisation chain(s), particularly for F28x7x and F28004x devices. The synchronisation chain configuration possibilities varies from device to device. The synchronisation chain for the TMS320F2837x is given in the following figure:



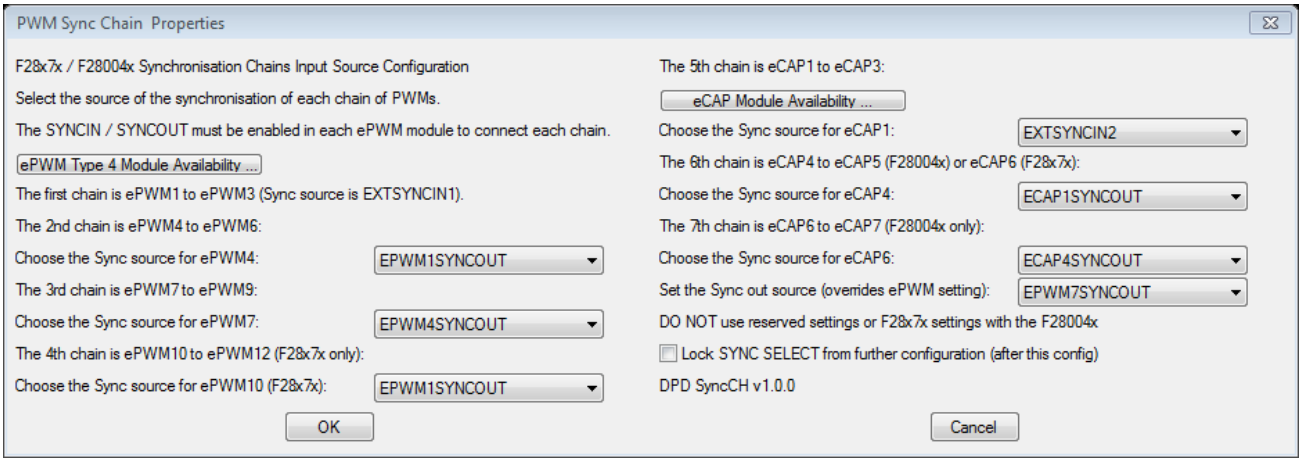
Extract from the Texas Instruments TMS320F2837xD Dual-core Delfino Microcontrollers Technical Reference Manual.

Application:

C2000 Type 4 ePWM (F28004x, F2837x, F2807x, F2838x)

Dialog properties:

The PWM Sync Chain Config block properties menu is shown in the following box which appears when right-clicking on the block.



The first chain is ePWM1 to ePWM3.

The second chain is ePWM4 to ePWM6:

Choose the sync source for ePWM4:

Select the source for the synchronisation of the ePWM modules 4 to 6. An ePWM module will be synchronised to this source only if enabled in the embedded ePWM block dialog.

The third chain is ePWM7 to ePWM9:

Choose the sync source for ePWM7:

Select the source for the synchronisation of the ePWM modules 7 to 9. An ePWM module will be synchronised to this source only if enabled in the embedded ePWM block dialog.

The 4th chain is ePWM10 to ePWM12 (if these ePWM modules are present in the device):

Choose the sync source for ePWM10:

Select the source for the synchronisation of the ePWM modules 10 to 12. An ePWM module will be synchronised to this source only if enabled in the embedded ePWM block dialog.

The 5th chain is eCAP1 to eCAP3:

Choose the sync source for eCAP1:

Select the source for the synchronisation of the eCAP modules 1 to 3. An eCAP-PWM module will be synchronised to this source only if enabled in the embedded eCAP-PWM block dialog.

The 6th chain is eCAP4 to eCAP5/6:

Choose the sync source for eCAP4:

Select the source for the synchronisation of the eCAP modules 4 to 6 (F283x7x) or 4 to 5 (F28004x). An eCAP-PWM module will be synchronised to this source only if enabled in the embedded eCAP-PWM block dialog.

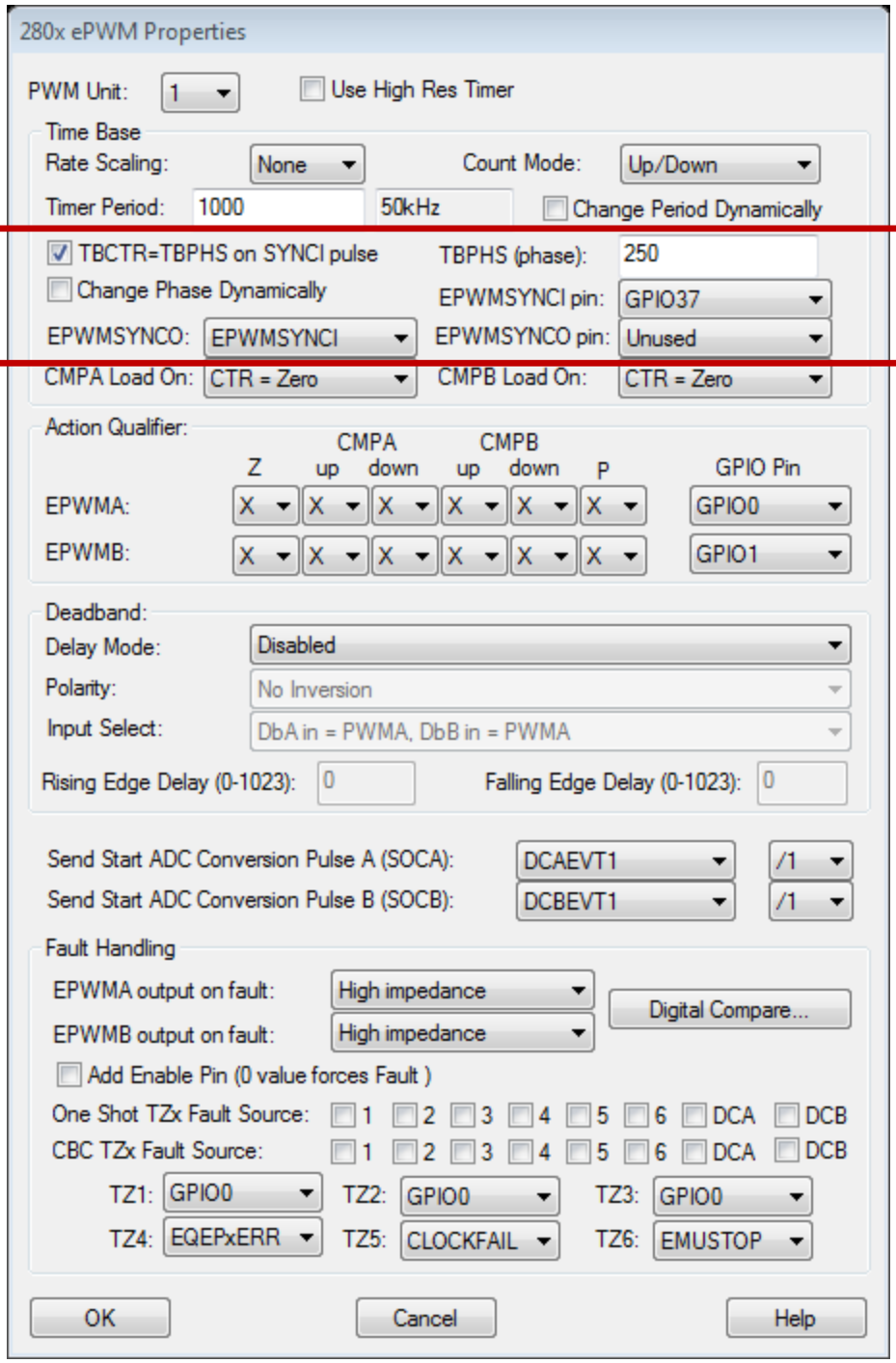
The 7th chain is eCAP6 to eCAP7 (F28004x):

Choose the sync source for eCAP6:

Select the source for the synchronisation of the eCAP modules 6 to 7. An eCAP-PWM module will be synchronised to this source only if enabled in the embedded eCAP-PWM block dialog.

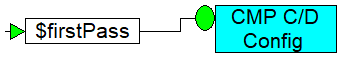
Lock Sync Select from further configuration:

If selected here, the PWM sync chain cannot be reconfigured within a diagram.



To completely configure the links within each synchronisation chain, each ePWM module within the chain must be configured to receive the synchronisation event (if they are to be synchronised) and to output the synchronisation event by selecting EPWMSYNCI for EPMWSYNCO above if any one of the following ePWM modules in the chain is to be synchronised.

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Compare C / D Config

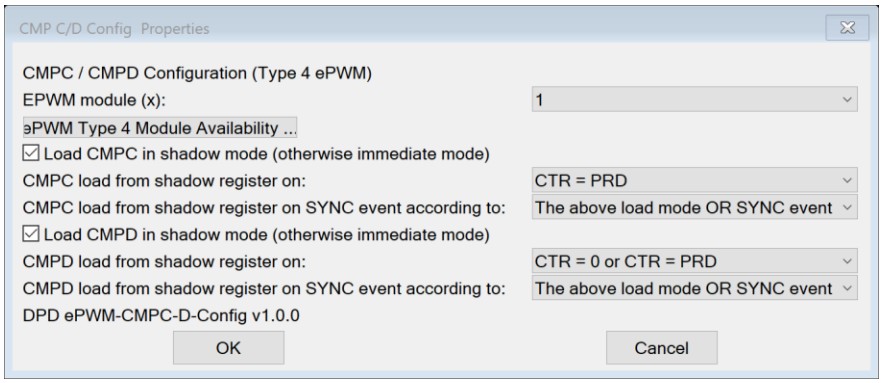
These blocks allow writing to the compare C and compare D registers of ePWM Type 4 modules.

Application:

C2000 Type 4 ePWM (F28004x, F2837x, F2807x, F2838x)

Dialog properties:

The Compare C/D Config properties menu is shown in the following box which appears when right-clicking on the block.



EPWM Module:

Select the ePWM module in which the compare C / D is to be configured.

Load CMPC/D in shadow mode:

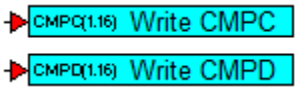
Select to load the CMPC or CMPD value in shadow mode, otherwise it will be loaded immediately.

CMPC/D load from shadow register on:

Select the counter moment to load the shadow register to the active register.

CMPC/D load from shadow register on SYNC event:

Either select to load on the above load mode or only on a Sync event.



Compare C / D write

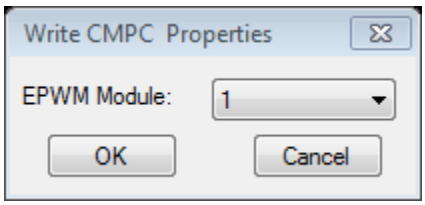
These blocks allow writing to the compare C and compare D registers of ePWM Type 4 modules.

Application:

C2000 Type 4 ePWM (F28004x, F2837x, F2807x, F2838x)

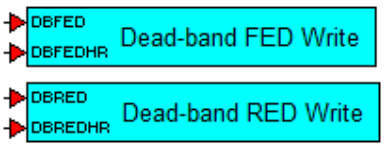
Dialog properties:

The Compare C/D properties menu is shown in the following box which appears when right-clicking on the block.



EPWM Module:

Select the ePWM module in which the compare C / D is to be set.



Sync Event Phase Direction (Config)

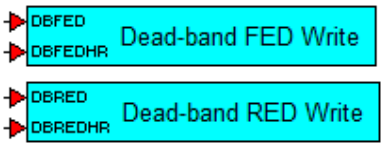
These blocks allow writing to the dead-band delay registers of ePWM modules. In this way, the dead-band can be varied dynamically within a diagram.

Dialog properties:

The Dead-band RED / FED write block properties menu is shown in the following box which appears when right-clicking on the block.

EPWM Module:

Select the ePWM module in which the dead-band RED



Sync Event Phase Direction (Dynamic)

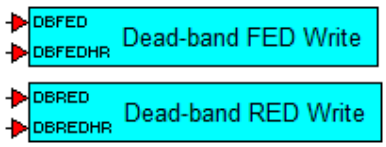
These blocks allow writing to the dead-band delay registers of ePWM modules. In this way, the dead-band can be varied dynamically within a diagram.

Dialog properties:

The Dead-band RED / FED write block properties menu is shown in the following box which appears when right-clicking on the block.

EPWM Module:

Select the ePWM module in which the dead-band RED

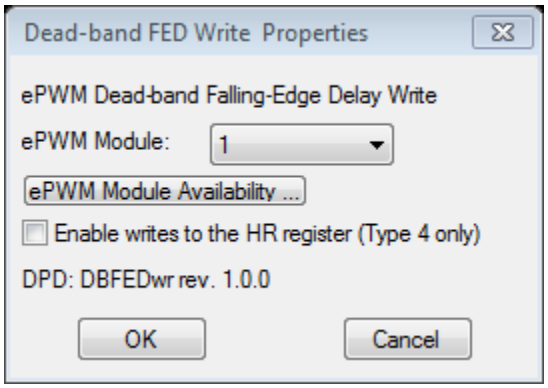


Dead-band RED / FED Write

These blocks allow writing to the dead-band delay registers of ePWM modules. In this way, the dead-band can be varied dynamically within a diagram.

Dialog properties:

The Dead-band RED / FED write block properties menu is shown in the following box which appears when right-clicking on the block.

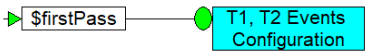


EPWM Module:

Select the ePWM module in which the dead-band RED/FED is to be set dynamically.

Enable writes to HR register:

Select this if it is desired to include writes to the high-resolution part of the dead-band delay value. This is valid for Type 4 ePWM. A Dead-band Full config block should be included in the diagram.

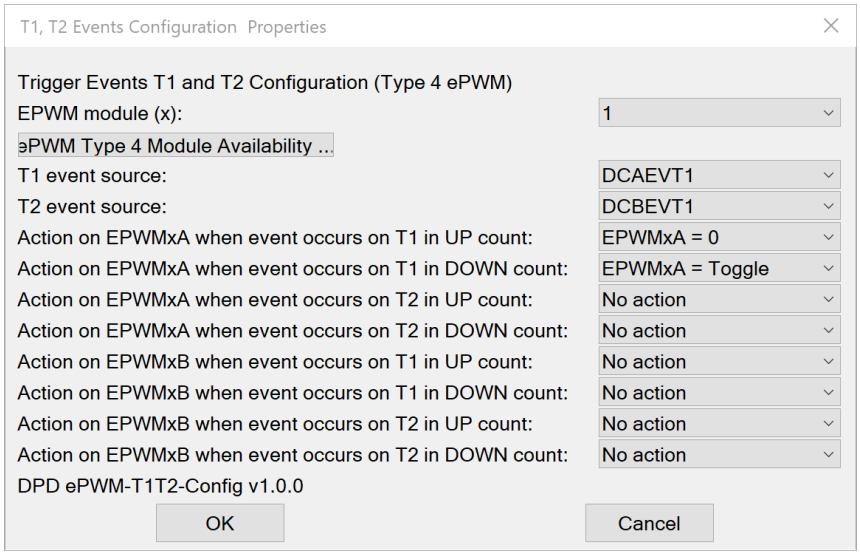


T1, T2 Events Config

This block allows the configuration of the T1 and T2 trigger events in the type 4/5 ePWM.

Dialog properties:

The T1, T2 events config block properties menu is shown in the following box which appears when right-clicking on the block.



EPWM Module:

Select the ePWM module in which the T1 and / or T2 events are to be configured.

T1 and T2 event source:

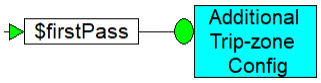
Select the source of the event from:

- DCAEVT1
- DCAEVT2
- DCBEVT1
- DCBEVT2
- TZ1
- TZ2
- TZ3
- EPWMxSYNCI
- DCEVTFILT

Action on EPWMxA/B when event occurs on T1/T2 in UP/DOWN count:

For any of the combinations of events, the following actions can be selected:

- No action
- EPWMxA = 0
- EPWMxA = 1
- EPWMxA = Toggle

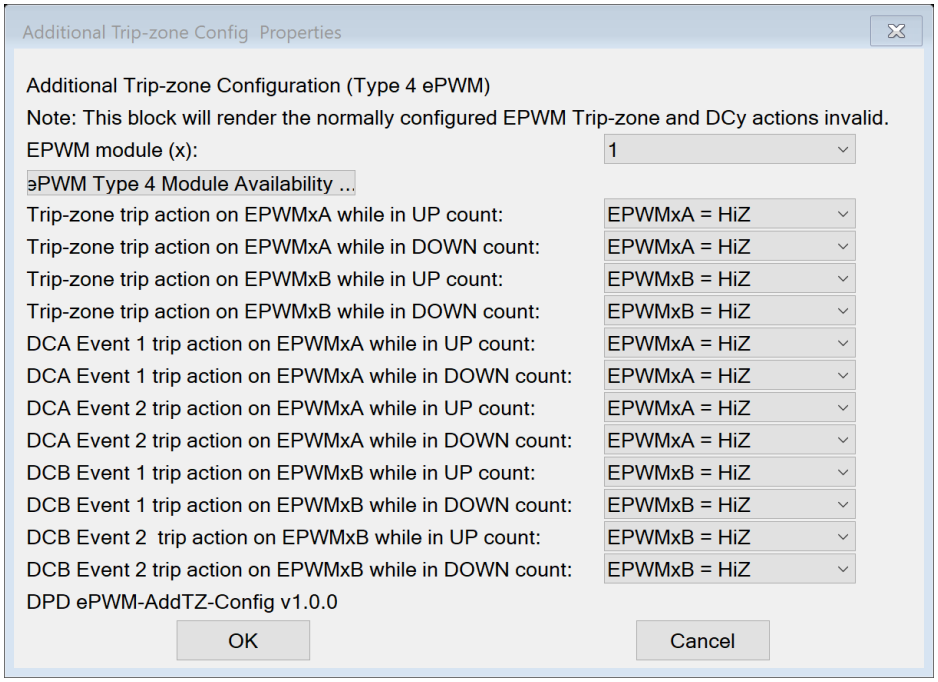


Additional Trip-zone Config

This block allows the configuration of the additional Trip-zone triggers for type 4/5 ePWM. Configuring this block in a diagram will invalidate the normal Trip-zone and Digital Compare trips configured in the corresponding Embedded ePWM block.

Dialog properties:

The additional trip-zone config block properties menu is shown in the following box which appears when right-clicking on the block.



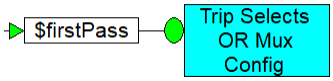
EPWM Module:

Select the ePWM module for which the additional trip zone configuration is to apply.

…. Action on EPWMxA/B while in UP/DOWN count:

Select the action to occur on the selected EPWM channel during the counter direction using the trip-zone, DCA or DCB event. The choices are:

EPWMxA = HiZ
EPWMxA = 1
EPWMxA = 0
EPWMxA = Toggle
Reserved
Reserved
Reserved
EPWMxA = No action

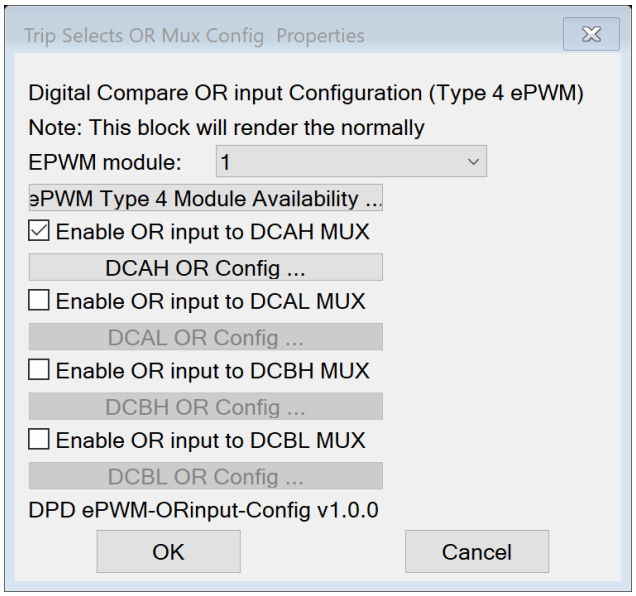


Trip Selects OR-Mux Config

This block allows the configuration of the OR-Mux for the trip selects in the type 4/5 ePWM.

Dialog properties:

The trip selects OR mux config block properties menu is shown in the following box which appears when right-clicking on the block.

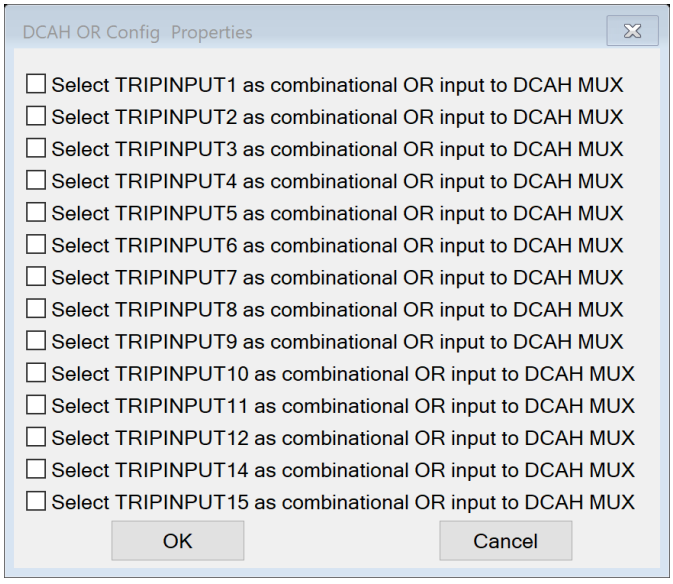


EPWM Module:

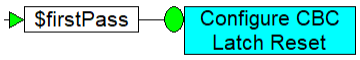
Select the ePWM module in which the configuration is to apply.

DCxy OR Config:

Each nested dialog has a selection as follows::



Select which inputs are to be fed into the OR gate to trigger the DC event.

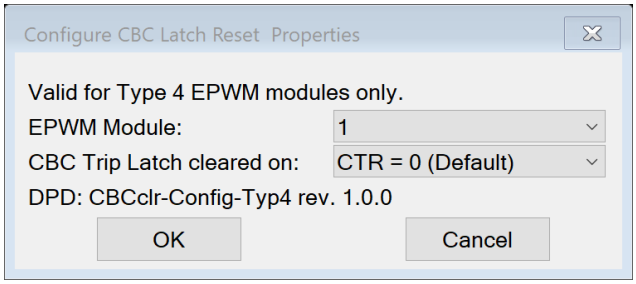


CBC Latch Reset Config

This block allows the configuration of the clearing of the cycle-by-cycle (CBC) trip latch (Type 4/5 ePWM). For previous ePWM types, the trip latch was always reset at the Counter = 0.

Dialog properties:

The CBC latch reset config block properties menu is shown in the following box which appears when right-clicking on the block.



EPWM Module:

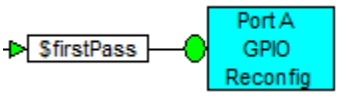
Select the ePWM module in which the reset configuration is to apply.

CBC trip latch cleared on:

Select the instant of clearing the CBC trip latch. The choices are:

CTR = 0 (Default)
CTR = PRD
CTR = 0 or CTR = PRD
Disabled

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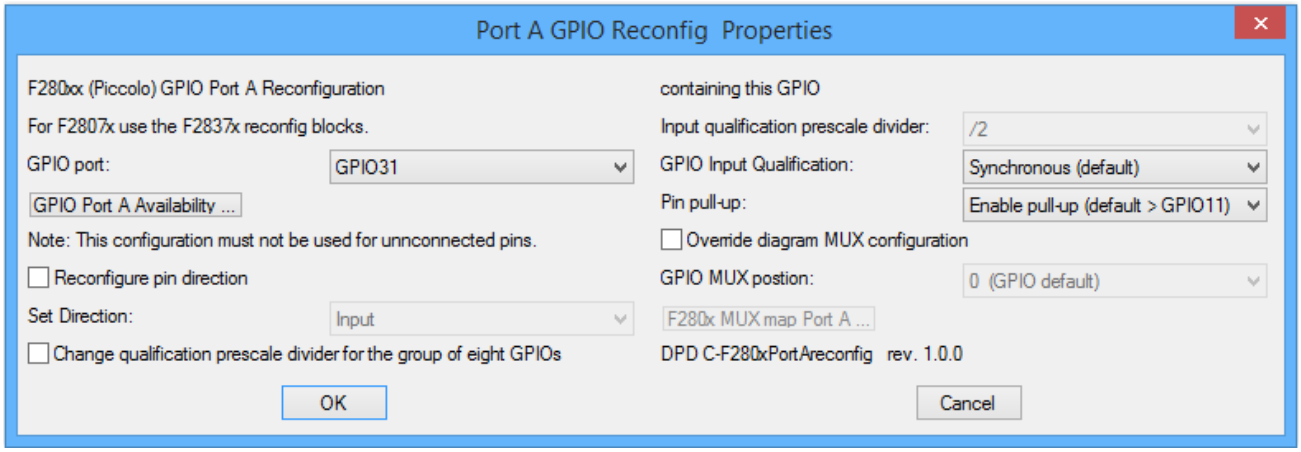
F280x GPIO Port A/B Reconfig

If it is desired to reconfigure a parameter of a specific GPIO port, this can be easily achieved with this block.

The GPIO configuration block can be placed in a diagram if a particular function of a GPIO is desired to be changed from the standard or default setting. The block can be enabled on the first pass (executed once only at the start of a routine) as is the default case or it may be enabled at any time during a diagram execution to change the port configuration.

Dialog properties:

The GPIO config block properties menu is shown in the following box which appears when right-clicking on the block.

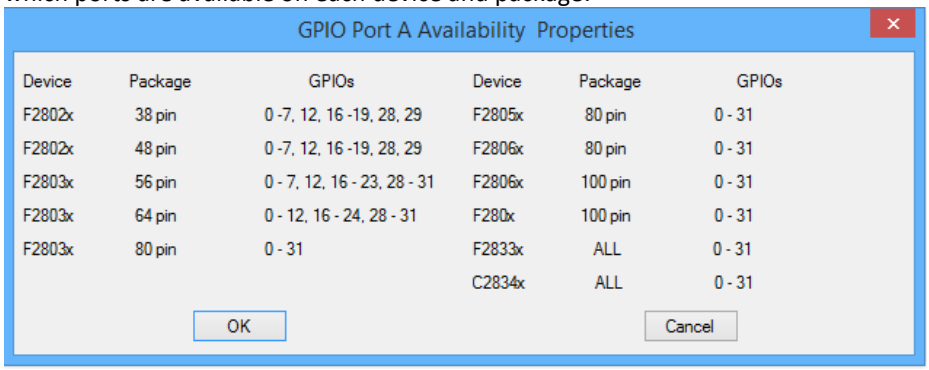


GPIO Port:

Select the GPIO to reconfigure with this configuration block.

GPIO Port A/B availability:

The port availability is tabled for convenience here in order to quickly determine which ports are available on each device and package.



Reconfigure pin direction:

Select this only if the pin direction reconfiguration is required.

The GPIO can be reconfigured as:

1. Input
2. Output
3. Bidirectional

The bidirectional configuration is identical to an output configuration.

Change qualification prescale divider:

Select this if it is desired to change the input qualification of the input port for the group of 8 GPIOs containing the selected GPIO port.

Input qualification prescale divider:

Select the value of the divider.

GPIO input qualification qualification:

Select from:

1. Synchronous
2. Qualification to 3 samples
3. Qualification to 6 samples
4. Asynchronous

Pin pull-up:

Choose whether the pin pull-up is to be enabled or disabled.

Override diagram MUX configuration:

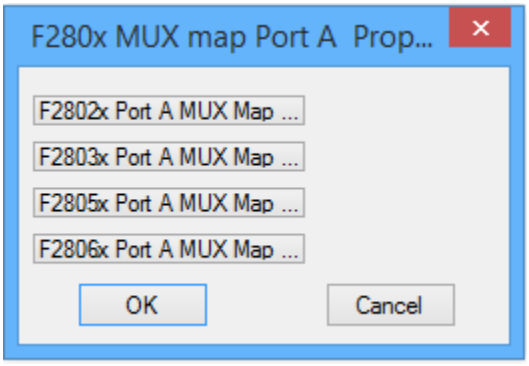
Select this if the MUXing of the pin needs to be changed from the Embed default setting.

GPIO MUX position:

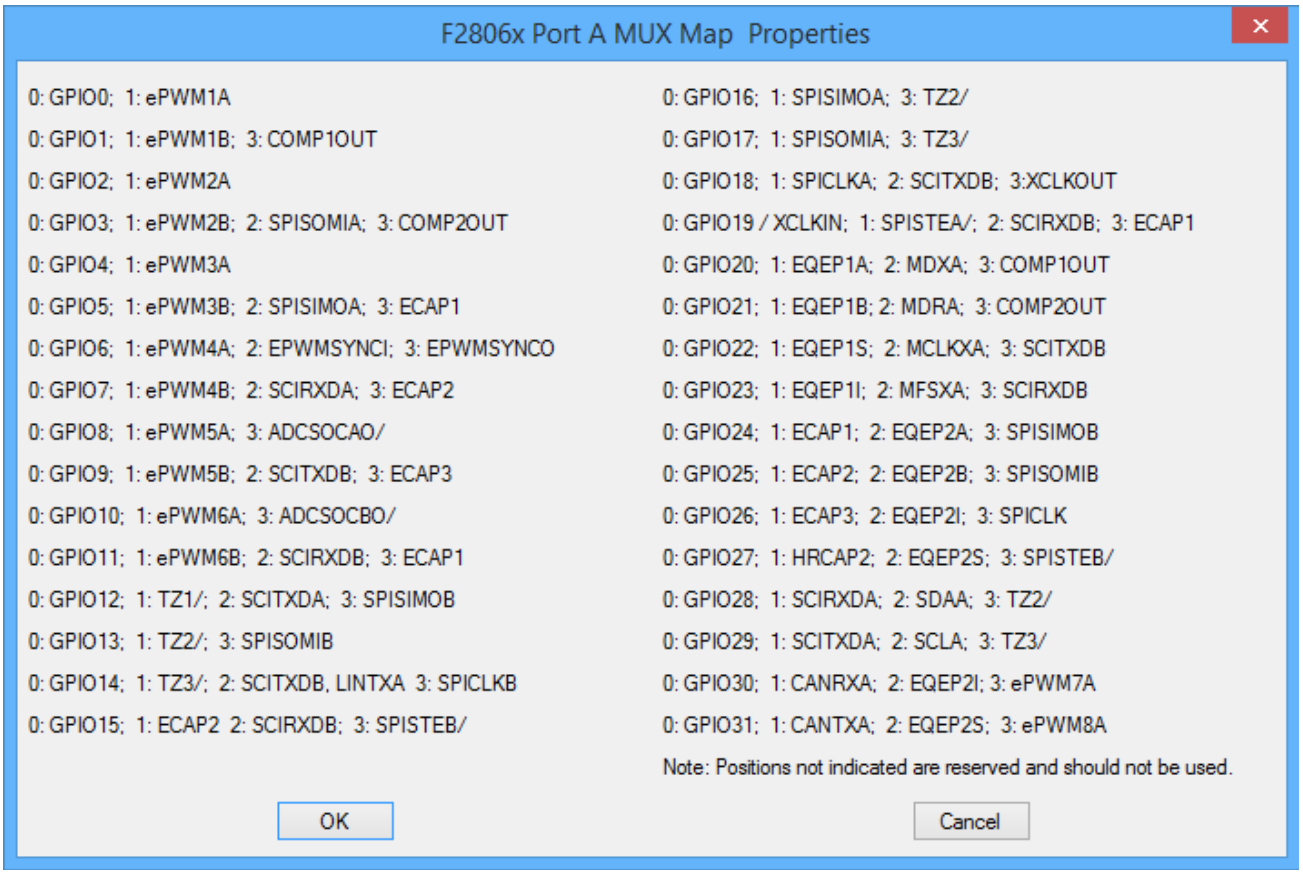
Select the MUX position, the positions are given below for the various devices.

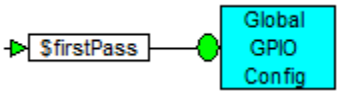
F280x MUX map port A/B:

The will bring up a dialog for each device to select the MUX mapping.



The MUX mapping for the F2806x device is given as follows:



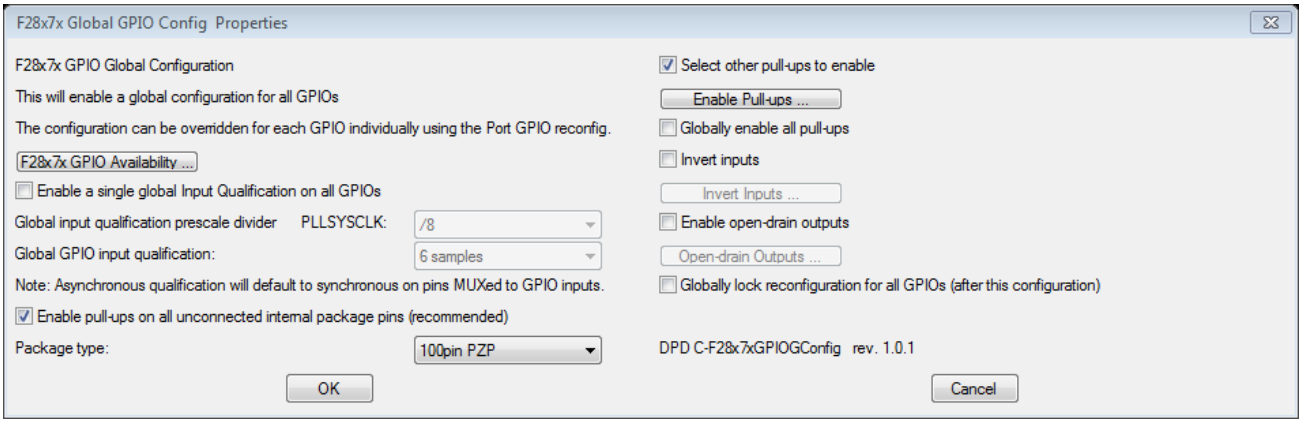


F28x7x GPIO Global Config

The GPIOs for the F2837x and piccolo F2807x can be set-up globally using this configuration block. All individual GPIOs can be given a global setting or in some cases each individual GPIO can have a particular configuration set with this block.

Dialog properties:

The GPIO Global reconfig block (F28x7x) properties menu is shown in the following box which appears when right-clicking on the block.



F28x7x GPIO availability:

The device and package dependent GPIO availability can be inspected in this dialog.

Enable a single global input qualification on all GPIOs:

A single input qualification can be set here for all GPIOs. Individual groups of GPIOs can be otherwise setup in the GPIO port reconfig blocks or within the embedded menu.

Global input qualification prescale divider:

Set the desired input qualification divider.

GPIO input qualification:

Select from:

1. Synchronous
2. Qualification to 3 samples
3. Qualification to 6 samples
4. Asynchronous

Enable all Pull-ups on unconnected internal package pins:

This is recommended by TI for the F28x7x where pull-ups are disabled as a default. This option will connect pull-ups to all internal pins that are not brought out to physical pins on smaller device packages.

Select other pull-ups to enable:

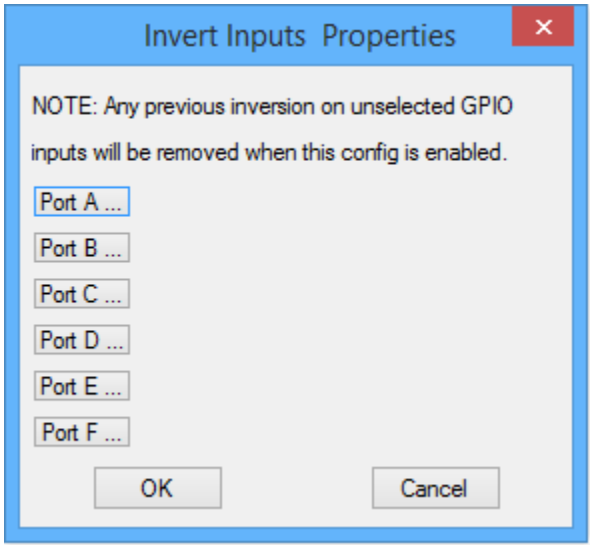
Any GPIO can be selected here in order to enable individual pull-ups at the pin. The dialogs are similar to the input inversion below. In this case, if a GPIO is not selected, no action will occur on that GPIO.

Globally enable all pull-ups:

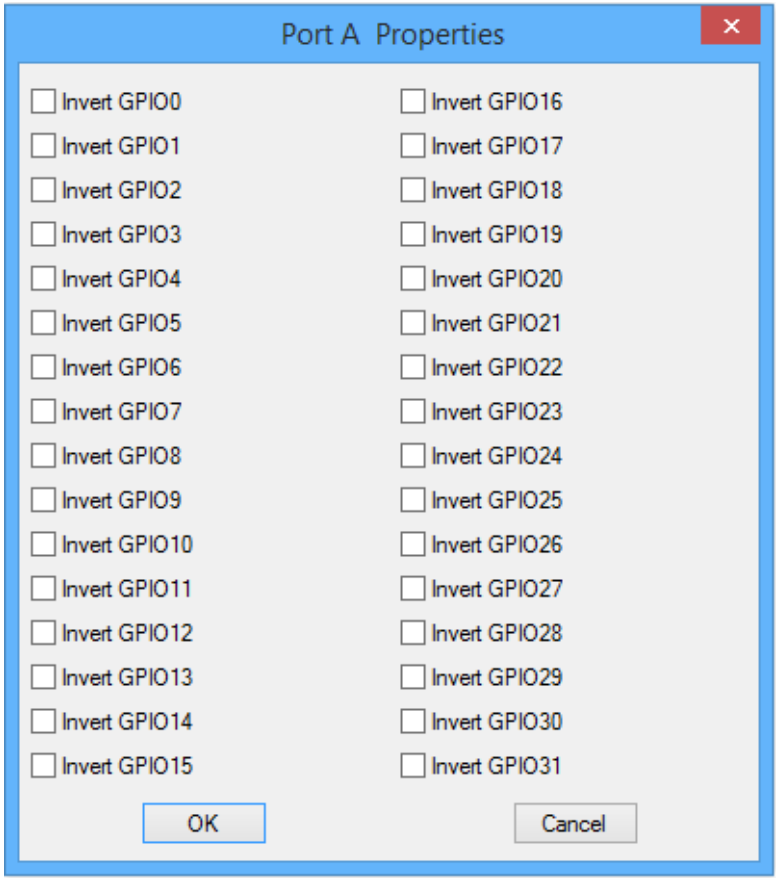
The pull-ups (disabled as a default) can be enabled for all pins with this option.

Input inversion:

Where the GPIO is an input, it can be inverted in hardware if so desired.
Select the port with the input pins to be inverted.



Select the GPIO inputs which are to be inverted in hardware.



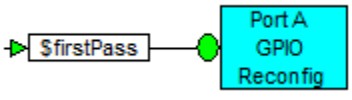
Open-drain output:

Here, if the GPIO is an output, it can be selected as an open-drain output. The setup is similar to the invert inputs above.
Note that if the input inversion and / or the open-drain options are selected, if a input inversion was previously configured on a GPIO input or if open-drain was previously configured on a GPIO output, then this configuration will override that and the previously configured GPIOs should be re-selected here.

Globally lock reconfiguration of all GPIOs:

Further reconfiguration of the GPIO ports can be locked out with this option.

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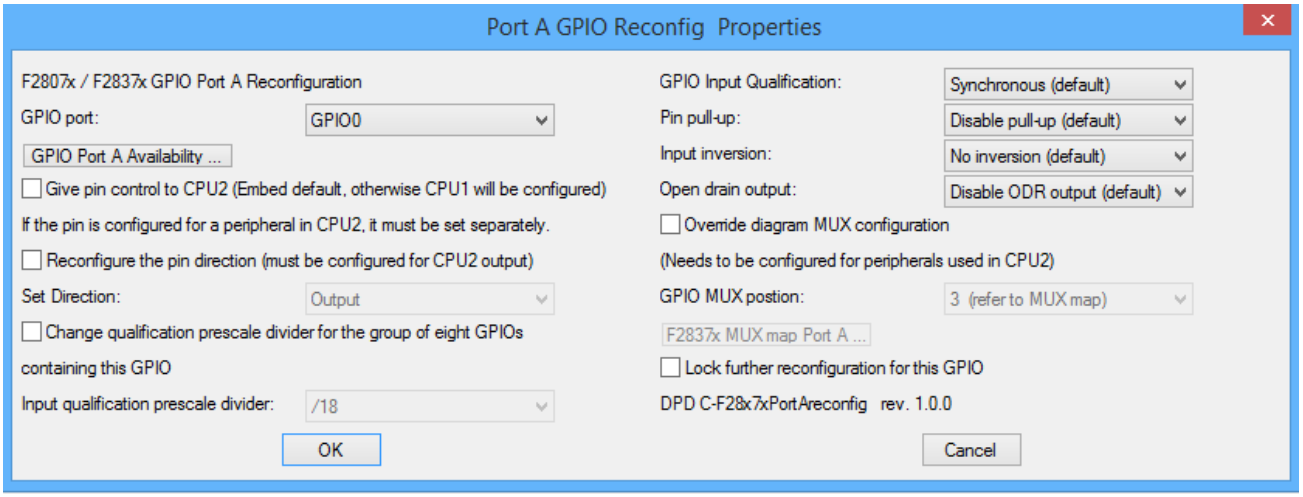


F28x7x GPIO Port A/B/C/D/E/F Reconfig

The GPIOs for the F2837x and piccolo F2807x can be set-up for each port using the configuration blocks for ports A to F.

Dialog properties:

The F28x7x GPIO config block properties menu is shown in the following box which appears when right-clicking on the block.



GPIO Port:

Select the GPIO to reconfigure with this configuration block.

GPIO Port A(to F) availability:

The port availability is tabled for convenience here in order to quickly determine which ports are available on each device and package.

Give pin control to CPU2:

Select this only if the control is to be given to the other CPU. If a port is used in a diagram, it will be automatically configured for the specified CPU. This option can override that configuration or give pin access to both CPUs.

Reconfigure pin direction:

Select this only if the pin direction reconfiguration is required or if the pin is to be controlled from CPU2.

The GPIO can be reconfigured as:

1. Input
2. Output
3. Bidirectional

The bidirectional configuration is identical to an output configuration.

Change qualification prescale divider:

Select this if it is desired to change the input qualification of the input port for the group of 8 GPIOs containing the selected GPIO port.

Input qualification prescale divider:

Select the value of the divider.

GPIO input qualification:

Select from:

1. Synchronous
2. Qualification to 3 samples
3. Qualification to 6 samples
4. Asynchronous

Pin pull-up:

Choose whether the pin pull-up is to be enabled or disabled.

Input inversion:

If the GPIO is an input, it can be inverted in hardware if so desired.

Open-drain output:

If the GPIO is an output, it can be selected as an open-drain output if required.

Override diagram MUX configuration:

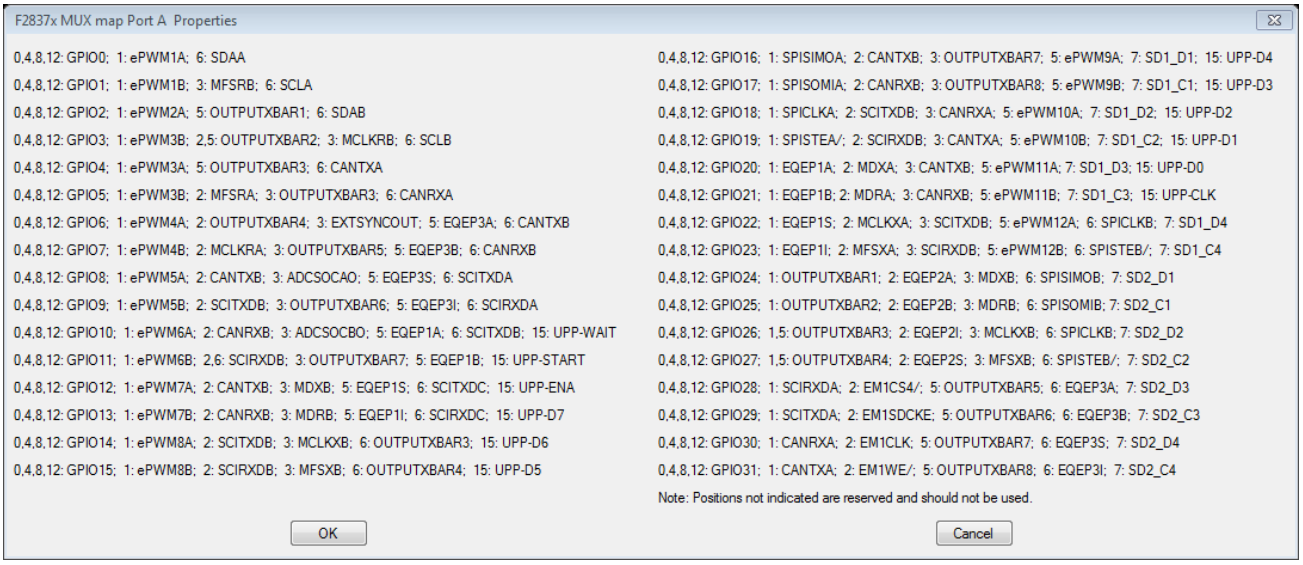
Select this if the MUXing of the pin needs to be changed from the Embed default setting.

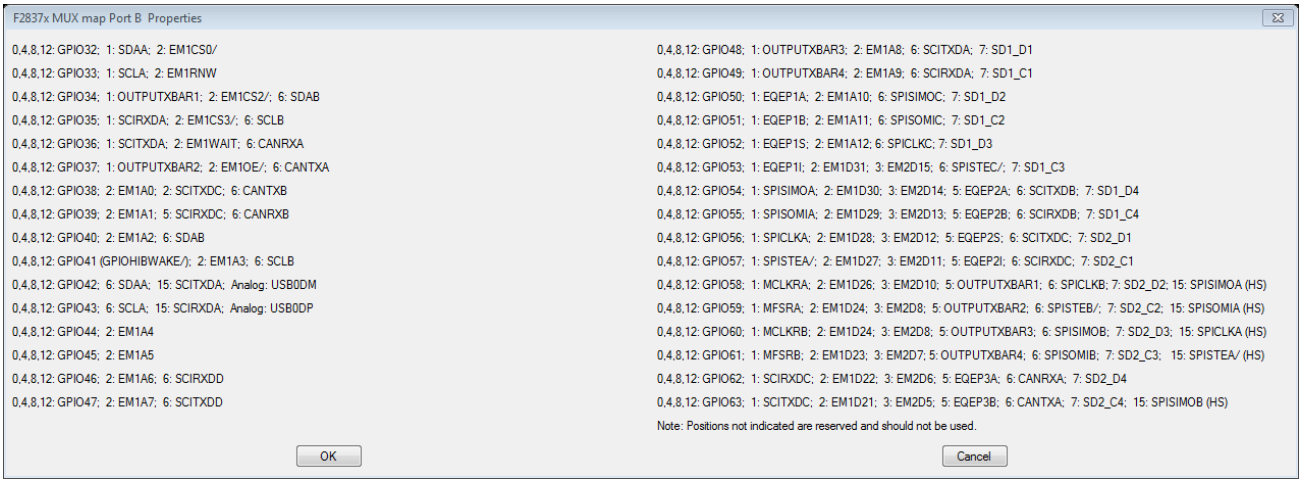
GPIO MUX position:

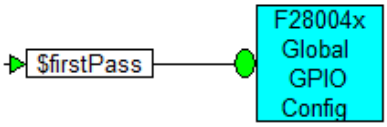
Select the MUX position, the positions are given below for the various devices.

F28x7x MUX map port A - F:

This tab will bring up a dialog for each device to select the MUX mapping.





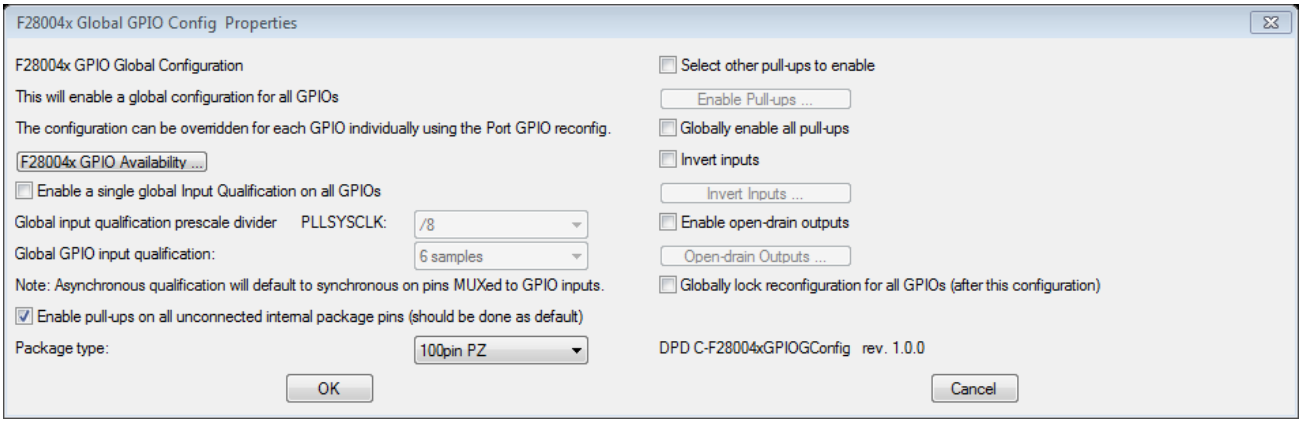


F28004x GPIO Global Config

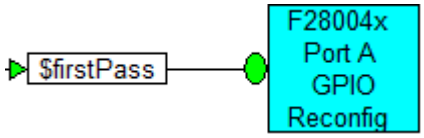
The GPIOs for the F28004x devices can be set-up globally using this configuration block. All individual GPIOs can be given a global setting or in some cases each individual GPIO can have a particular configuration set with this block.

Dialog properties:

The GPIO Global reconfig block (F28004x) properties menu is shown in the following box which appears when right-clicking on the block.



The configuration options are similar to the F28x7x devices.

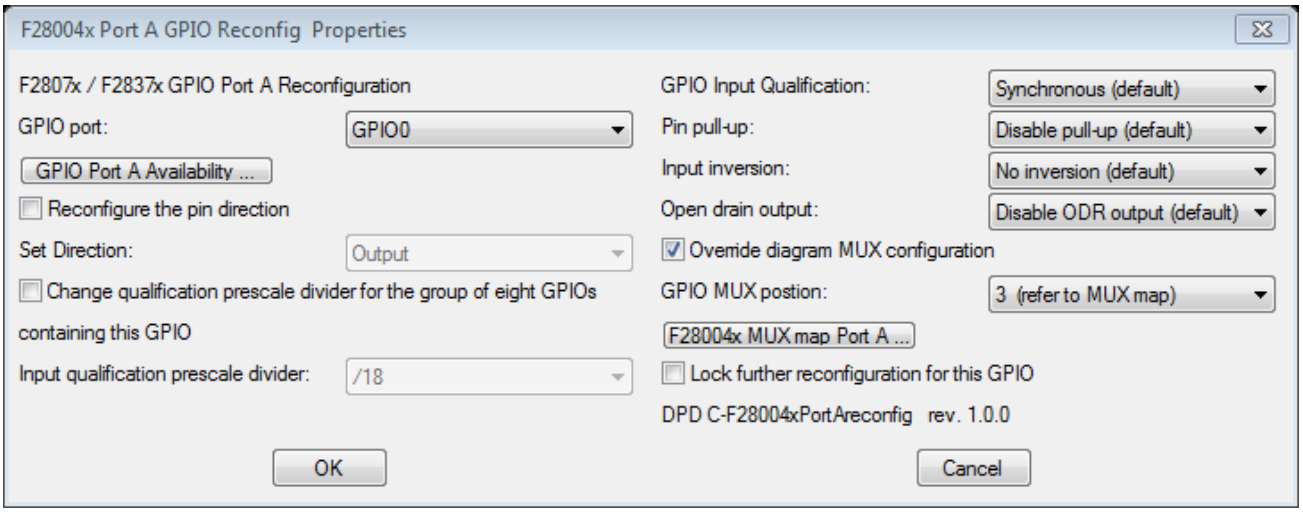


F28004x GPIO Port A/B Reconfig

The GPIOs for the F28004x can be set-up for each port using the configuration blocks for ports A to B.

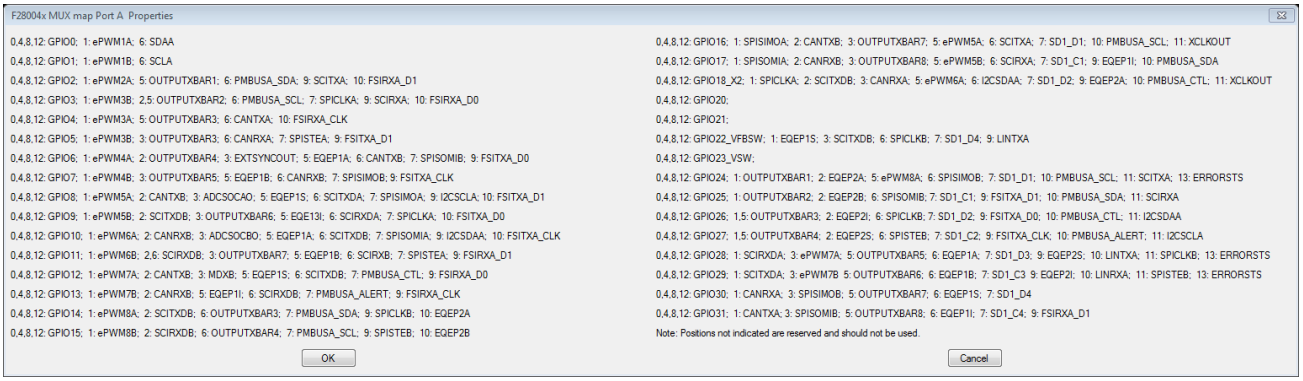
Dialog properties:

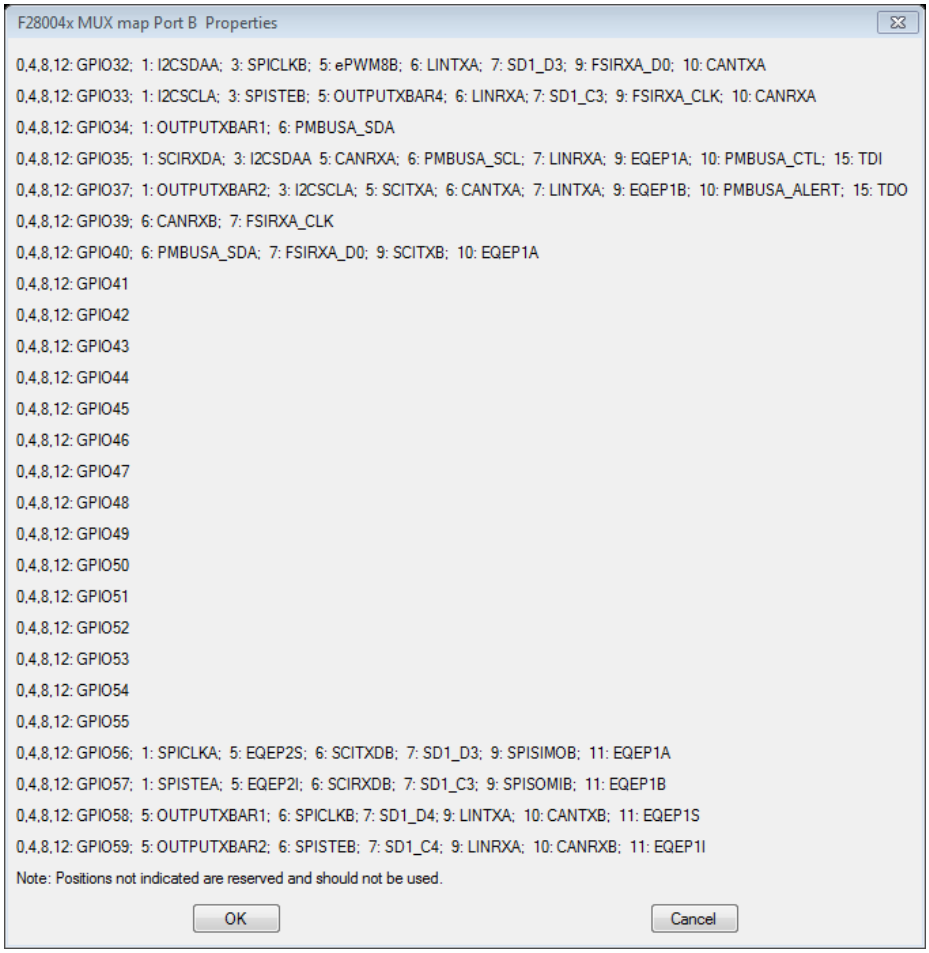
The F28004x GPIO reconfig block properties menu is shown in the following box which appears when right-clicking on the block.



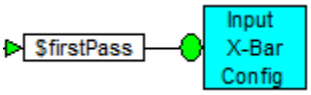
The GPIO reconfiguration options are similar to the F28x7x devices.

The MUX ports for the F28004x are:





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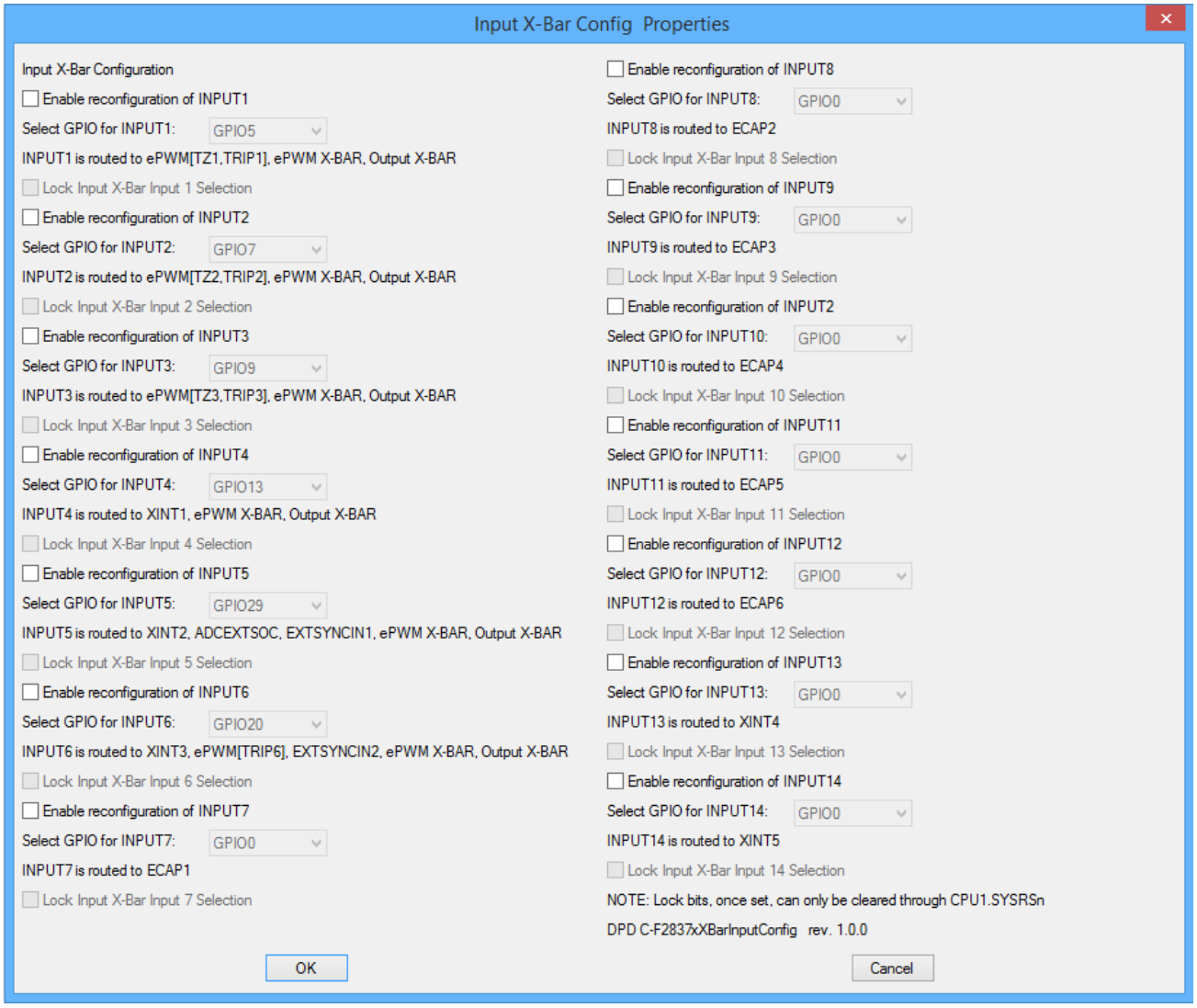


Input X-Bar Config

The input X-Bar can be directly configured within this block. Otherwise, many of the input X-Bar functions such as eCAP will be configured automatically when configuring those blocks.

Dialog properties:

The Input X-Bar config block properties menu is shown in the following box which appears when right-clicking on the block.



Enable reconfiguration of input x:

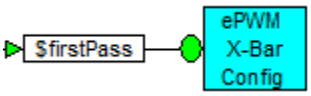
The input X-Bar can be reconfigured for each input from 1 to 14.

Select GPIO for input x:

The GPIO for the input X-Bar can be selected individually.

Lock input X-Bar Input x selection:

Further input X-Bar reconfiguration can be locked.

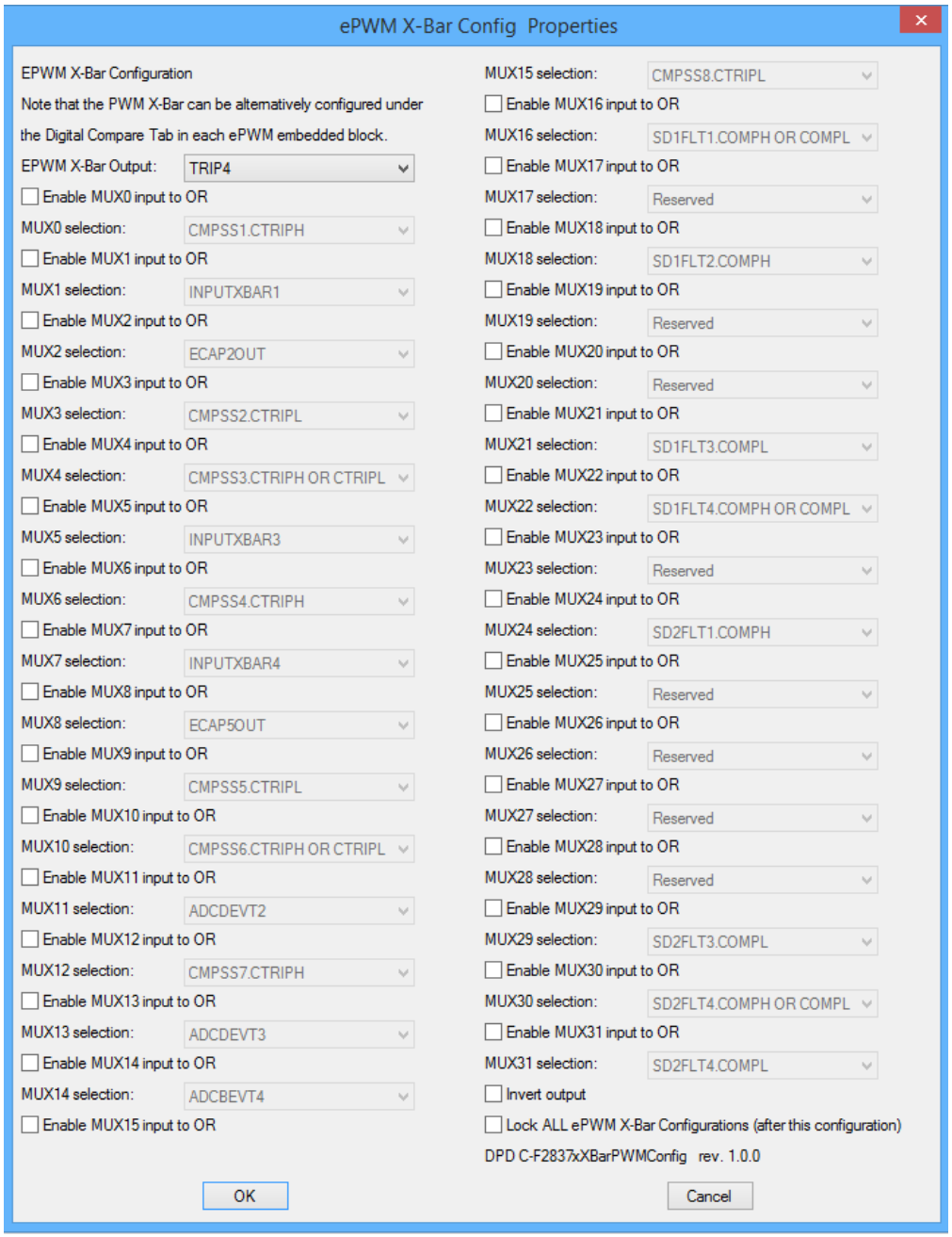


ePWM X-Bar Config

The ePWM X-Bar can be configured (or reconfigured) within this block. Note that the ePWM X-Bar can also be configured within the embedded ePWM blocks.

Dialog properties:

The ePWM X-Bar config block properties menu is shown in the following box which appears when right-clicking on the block.



ePWM X-Bar output:

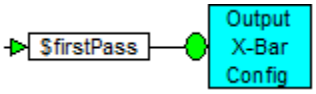
Select the desired ePWM X-Bar Trip output from 4 to 12.

Enable MUXx input into OR:

Select this to enable the desired MUX input into the output ePWM X-Bar OR.

MUXx selection:

Select the signal for each MUX of the ePWM X-Bar.

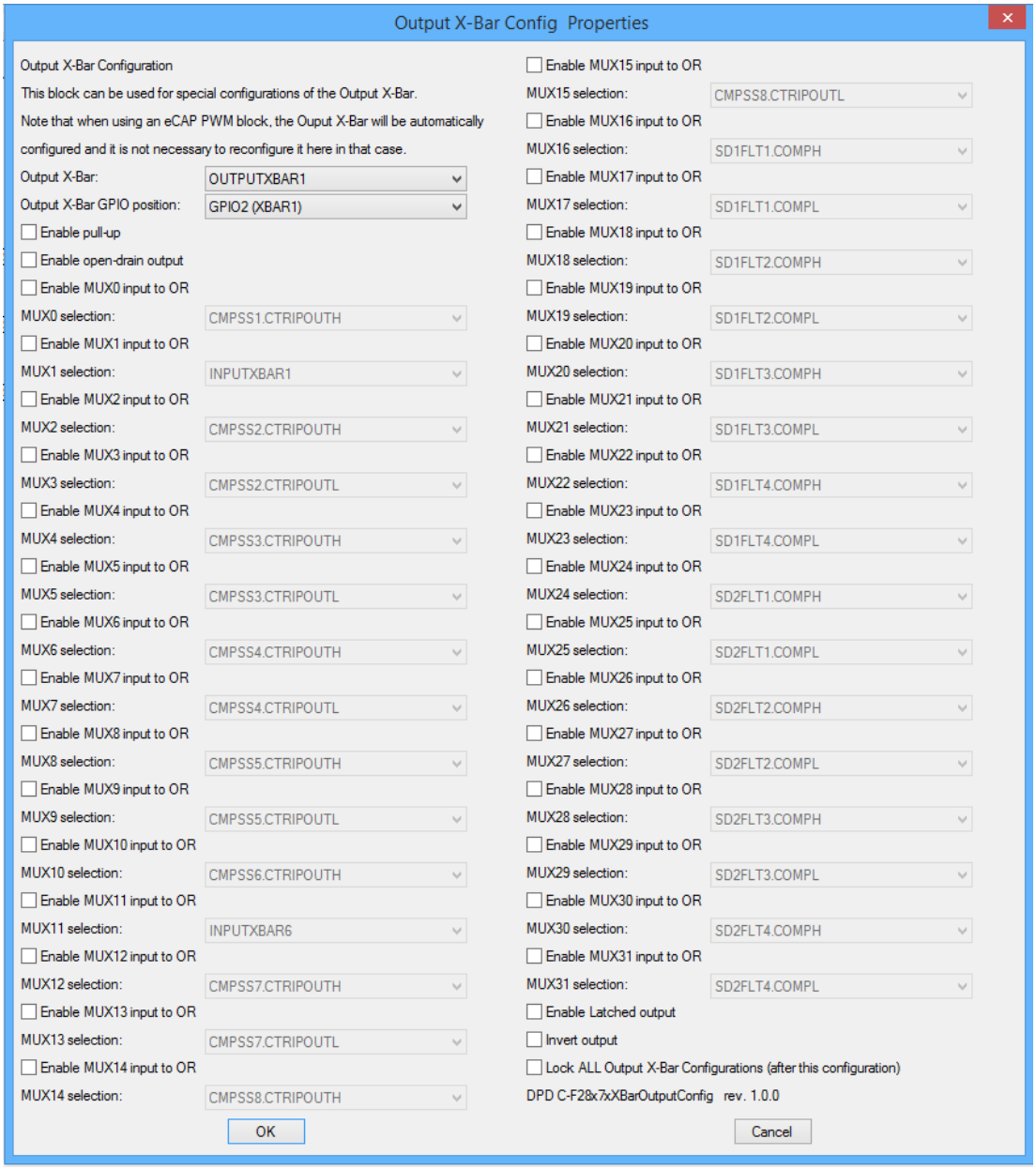


Output X-Bar Config

The output X-Bar can be directly configured within this block.

Dialog properties:

The Output X-Bar config block properties menu is shown in the following box which appears when right-clicking on the block.



Output X-Bar:

Select the desired output X-Bar from 1 to 8.

Output X-Bar GPIO selection:

Select the required GPIO for this X-Bar output.

Enable pull-up:

The pull-up can be enabled on this output.

Enable Open drain output:

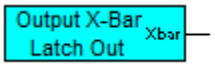
The output can be configured as open-drain.

Enable MUXx to OR:

Select this to enable the desired MUX input into the output X-Bar OR.

MUXx selection:

Select the appropriate function of the MUX.

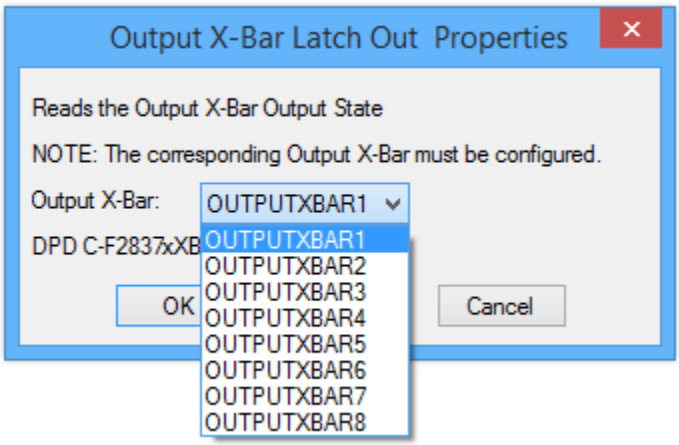


Output X-Bar Read Latch

The state of the output X-Bar latches can be read and monitored with this block.

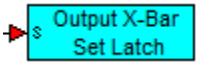
Dialog properties:

The Output X-bar read latch block properties menu is shown in the following box which appears when right-clicking on the block.



Output X-Bar:

Select the desired Output X-Bar to be read and monitored.

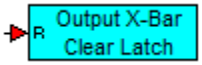


Output X-Bar Set Latch

This block can set the selected output X-Bar Latch.

Dialog properties:

The dialog is the same as the output X-Bar read latch above.

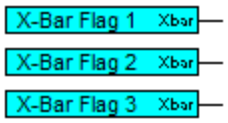


Output X-Bar Clear Latch

This block can clear the selected output X-Bar latch.

Dialog properties:

The dialog is the same as the output X-Bar read latch above.

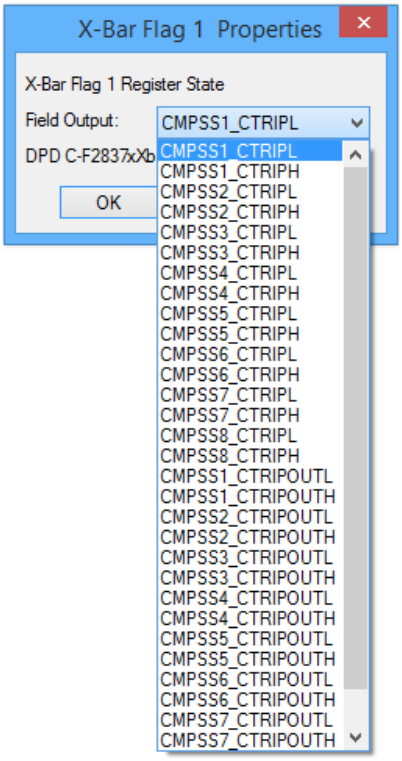


X-Bar Read Flag 1/2/3/4

The X-Bar flags can be conveniently read and monitored with these blocks.

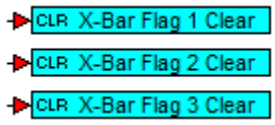
Dialog properties:

The X-Bar Read Flag config block properties menu for Flag 1 is shown in the following box which appears when right-clicking on the block.



Field Output:

Select the field of the X-Bar flag which is to be read with this block.



X-Bar Clear Flag 1/2/3/4

These blocks can clear the flag of the output X-Bar.

Dialog properties:

The dialog is similar to the X-Bar read flag.

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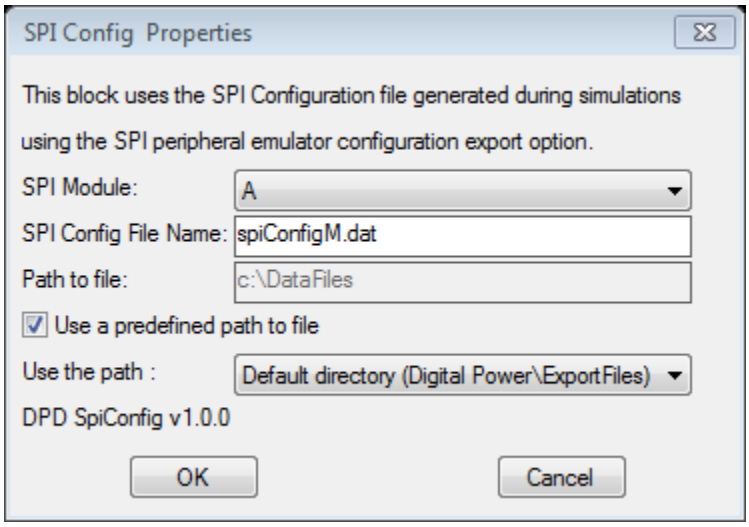


SPI Config

This block can be used with an import file containing the register values for the configuration of the SPI communication interface. The configuration import file can be generated by the SPI master or SPI slave emulator block under MCU peripherals in the simulation section of DPD.

Dialog properties:

The SPI config block properties menu is shown in the following box which appears when right-clicking on the block.



SPI Module:

Select the SPI module to be configured.

SPI Config file name:

Enter the full file name of the import file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

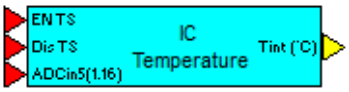
Select this if the file is located in one of the pre-defined paths.

Use the path:

The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

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IC Temperature

This block can be placed in a code-generable diagram to measure the internal MCU temperature.

Input Pins: **EN TS** A value of one here will enable the

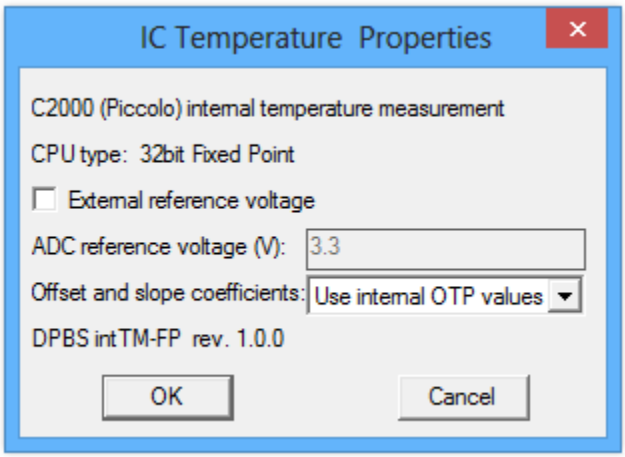
Dis TS A clock input which will determine the internal delay times.

ADCin5 The input signal to be monitored.

Output Pins: **Tint (°C)** The internal IC temperature in degrees Celcius.

Dialog properties:

The IC temperature block properties menu is shown in the following box which appears when right-clicking on the block.



External reference voltage:

Enter the desired value of the lower trip level.

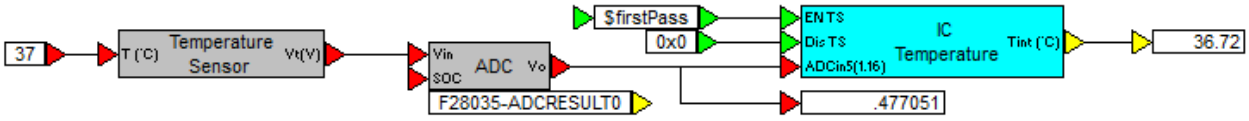
ADC reference voltage:

Enter the desired value of the upper trip level.

Offset and slope coefficients:

Enter the delay time of the fault activation. For a fault to be activated (output = 1), the input level must remain outside the trip levels for the duration of this delay.

The following diagram shows an implementation for the IC temperature measurement block, both for simulation and for code generation.





Internal Oscillator Compensation

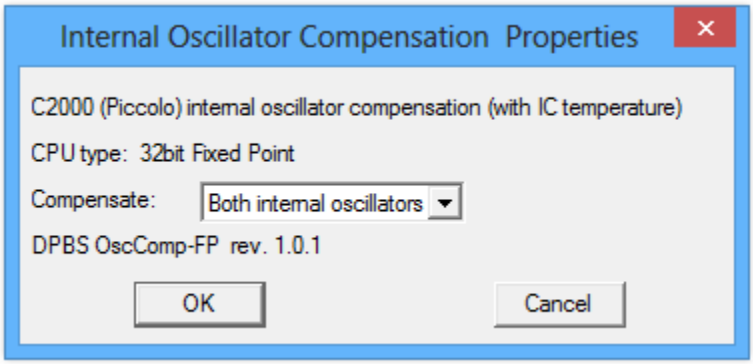
This block, when compiled in a diagram for a piccolo MCU, will compensate for the internal oscillator frequency drift with respect to its operating temperature.

Input Pins: **IC Temp**

The MCU internal temperature measurement is connected here, usually from the output of the IC temperature block.

Dialog properties:

The internal oscillator compensation block properties menu is shown in the following box which appears when right-clicking on the block.



Compensate:

Either the internal oscillator 1 or the internal oscillator 2 or both can be compensated for with a drift in the IC temperature.

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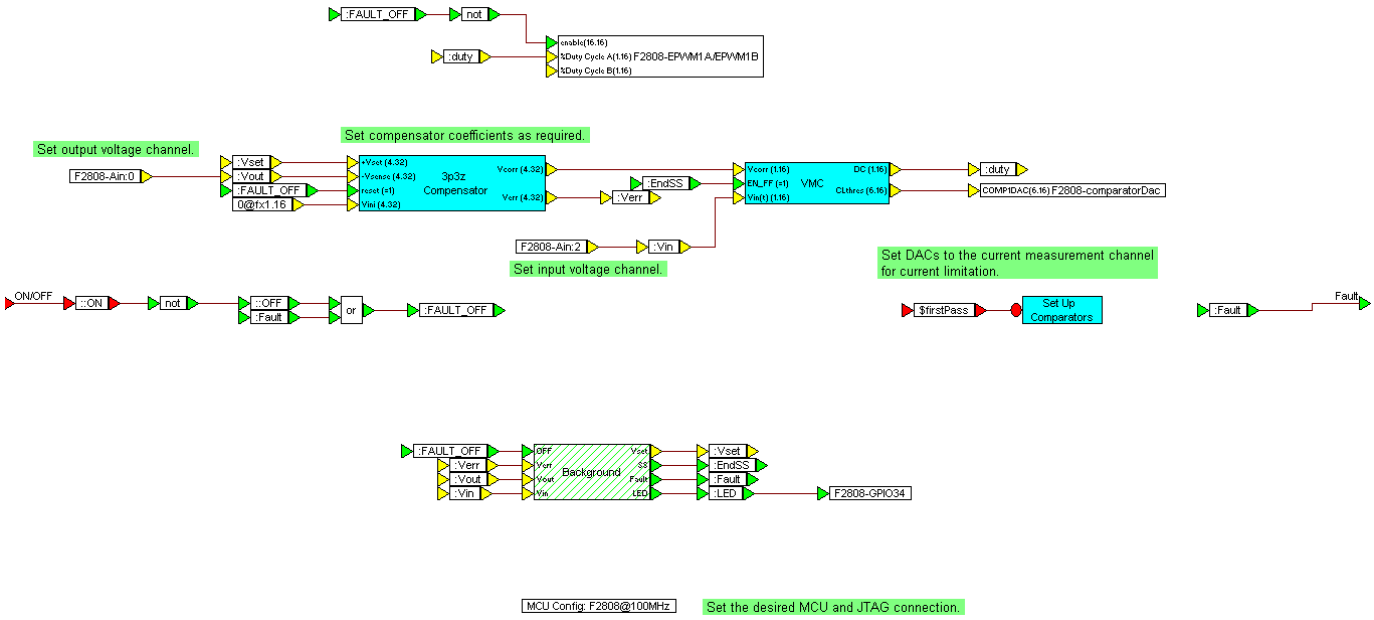
Code-generable Control Loops



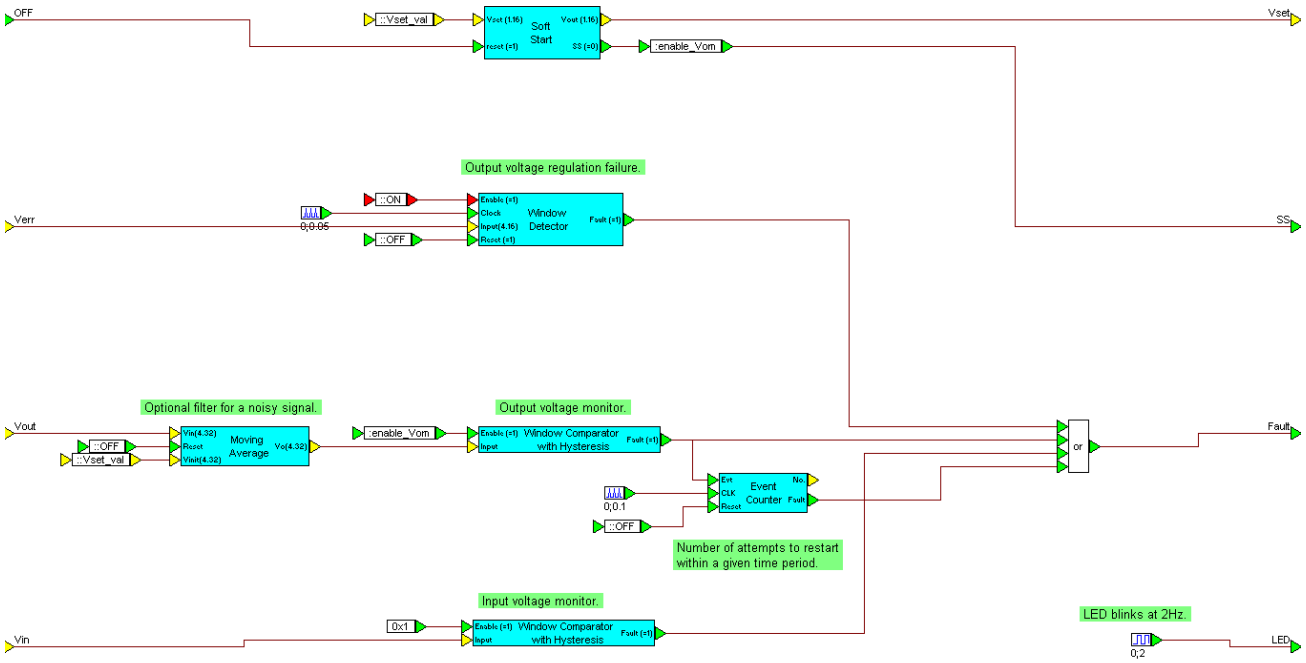
Voltage Mode Control (VMC)

This block presents an example only of how the blocks from the codegen section can be arranged in order to realize a practical control loop for Voltage Mode Control, with background control functions and supervision of the power supply parameters. The block can be code-generated and compiled directly in Embed and downloaded to a MCU.

The following figure is the upper level of the routine – the Interrupt Service Routine (ISR) where the MCU rate is the simulation rate of the Embed diagram in which the block resides. This level can be visualized by double clicking on the Voltage Mode Control block.

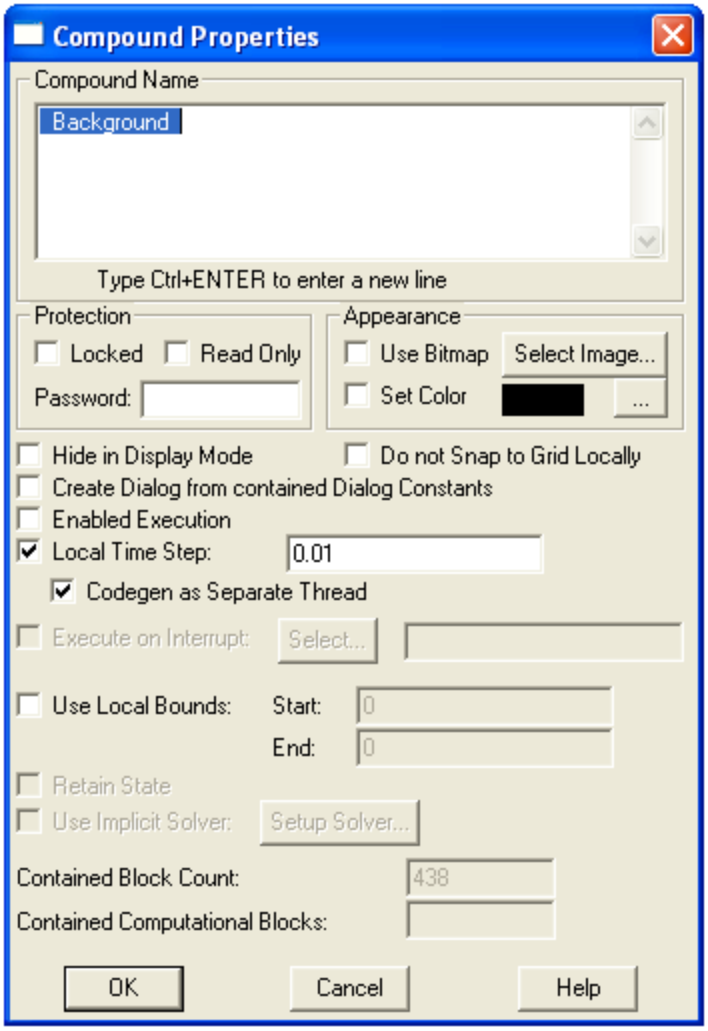


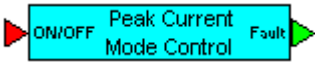
The following figure is the background routine for soft start and power supply supervision which can be found by simply right-clicking on the background block in the above figure. The background block contains tasks which are not timing critical.



By CTRL + right clicking on the background block, one will bring up the compound block properties dialog. It can be seen that a new local time step has been set for this block and its sub-contents and the “Code-gen as separate thread” has been selected. The block will run at the specified rate, reducing CPU workload for less critical functions or for functions which do not need to be calculated every PWM switching cycle. Any simulation using this block will also be performed as a multi-rate simulation (see the Embed manual for more details).

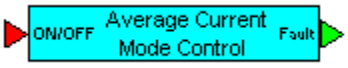
By enabling the code-gen as separate thread option, the block contents will be code generated in a way to be separated from the ISR main timing. The ISR will be given priority for the time critical tasks while the background loop will be executed at the lower defined rate with the calculations for these tasks spread between each part of the remaining time at the end of each ISR cycle, after the calculation of the critical tasks.





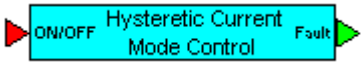
Peak Current Mode Control (PCMC)

This block presents an example only of how the blocks from the codegen section can be arranged in order to realize a practical control loop for Peak Current Mode Control, with background control functions and supervision of the power supply parameters. The block can be code-generated and compiled directly in Embed and downloaded to a MCU. The organisation of the blocks at the lower levels are similar to the voltage mode control code generable block.



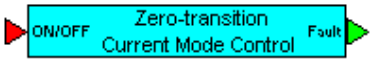
Average Current Mode Control (ACMC)

This block presents an example only of how the blocks from the codegen section can be arranged in order to realize a practical control loop for Average Current Mode Control, with background control functions and supervision of the power supply parameters. The block can be code-generated and compiled directly in Embed and downloaded to a MCU. The organisation of the blocks at the lower levels are similar to the voltage mode control code generable block.



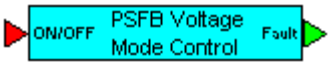
Hysteretic Current Mode Control (HCMC)

This block presents an example only of how the blocks from the codegen section can be arranged in order to realize a practical control loop for Hysteretic Current Mode Control, with background control functions and supervision of the power supply parameters. The block can be code-generated and compiled directly in Embed and downloaded to a MCU. The organisation of the blocks at the lower levels are similar to the voltage mode control code generable block.



Zero-transition Current Mode Control (ZCMC)

This block presents an example only of how the blocks from the codegen section can be arranged in order to realize a practical control loop for Zero-transition Current Mode Control, with background control functions and supervision of the power supply parameters. The block can be code-generated and compiled directly in Embed and downloaded to a MCU. The organisation of the blocks at the lower levels are similar to the voltage mode control code generable block.



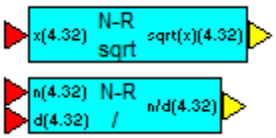
Phase Shifting Full-bridge Voltage Mode Control (PSFB-VMC)

This block presents an example only of how the blocks from the codegen section can be arranged in order to realize a practical control loop for Phase-shifting Full-bridge Voltage Mode Control, with background control functions and supervision of the power supply parameters. The block can be code-generated and compiled directly in Embed and downloaded to a MCU. The organisation of the blocks at the lower levels are similar to the voltage mode control code generable block.

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Extra

This section contains additional blocks which can be useful in digital control routines.



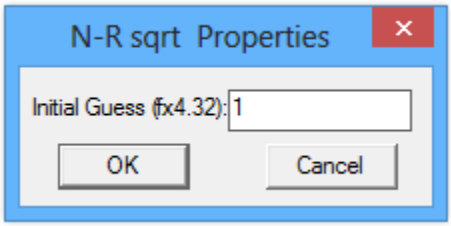
Newton-Raphson Divide and Square-root

These blocks perform the normally CPU intensive divide and square-root using the iterative Newton-Raphson technique.

Input Pins:	**x**	The input value for the square-root.
	n	The numerator input of the divide.
	d	The denominator input of the divide.
Output Pins:	**sqrt(x)**	The result of the Newton-Raphson square-root operation.
	n/d	The result of the Newton-Raphson divide.

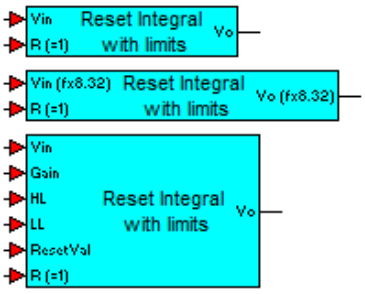
Dialog properties:

The Newton-Raphson square-root block properties menu is shown in the following box which appears when right-clicking on that block.



Initial guess:

An initial guess closer to the expected value will ensure faster convergence and stability.



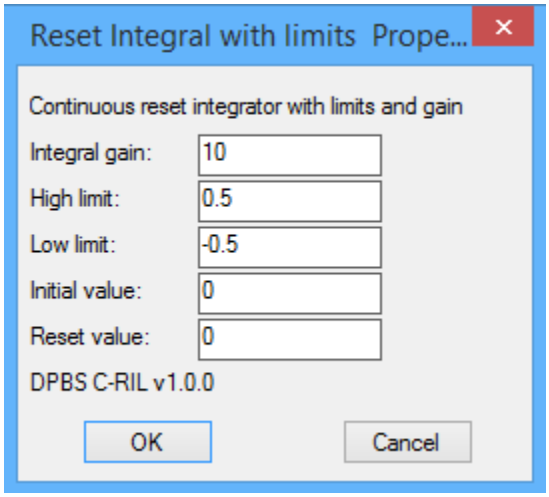
Reset Integrals with Limits

These blocks are some models of integrals which have both a reset and internal limits. The blocks can be used for code generation or in simulations where both the limits of the integral and the ability to reset the integral to a given value duration a simulation is required.

Dialog properties:

The reset integrals with limits blocks properties menu is can be viewed by right-clicking on each block. Shown is the dialog for the reset integral with limits for the continuous (floating point) model. The reset integral with reset and limits and input

pins has only the initial value in the dialog in order that the parameters can be changed dynamically at the input pins.



Integral gain:

Enter the desired gain of the integrator.

High limit:

Enter the high-level limit of the integrator.

Low limit:

Enter the low level limit of the integrator.

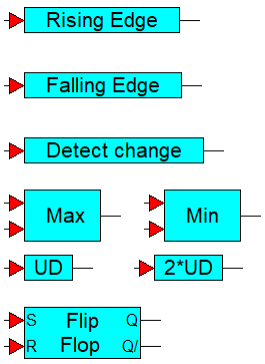
Initial value:

Enter the value of the integrator at the start of simulation.

Reset value:

Enter the value to which the integrator will be set on a reset action.

Frequently Used



This section of blocks within the codegen section consists of a set of modifiable blocks which are frequently used in developing digital control algorithms. The blocks in this location can be added to by the user by simply saving a diagram with the desired name into this directory.

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Main Contents

Block Reference - Simulation

The simulation environment of the digital power designer block set consists of a series of blocks aimed at enabling the simulation of power converters with their supporting circuits and respective control algorithms and various control techniques. Simulations of control loops can be performed by appropriately connecting together the blocks within the block set. Examples are given in the block set to demonstrate many of the capabilities of the simulation section of the block set. The aim of the simulations is to develop control algorithms, and particularly digital control algorithms and therefore the features of the various blocks are aimed at this purpose. The block set is not intended to simulate the various features of power converters which are not related to the digital control loop design, however the majority of features of analog converter control can also be simulated.

Block Convention

The blocks within the simulation environment are designed for simulation purposes only and are not code-generable.

The blocks within the simulation environment have different default colouring in order to distinguish them from normal code-generable blocks and to identify their application (external hardware, MCU peripherals inside an MCU chip or firmware).

The majority of the blocks in the simulation environment are representations of hardware (electronic) circuits. However, some of the blocks can be represented in hardware such as compensators in analog mode and in firmware on a MCU when the compensators are selected to be discrete. Some blocks, such as the moving average filter, can only be implemented in firmware on a MCU.

The colour coding within the simulation section of the block set generally reflect the functioning of the block. For blocks that represent external hardware functions (such as power converters or sensors and electronics), the blocks are as a default blue. For blocks that are intended to model software functions implemented in an MCU (such as compensators, filters and controllers), they are as a default yellow. Note that these blocks often have an option to function in an analog domain, in which case they would represent hardware functions, or in a digital domain, in which case they would generally represent functions to be implemented in firmware (software). The blocks coloured grey as a default represent MCU peripherals which are hardware-based but realised internally within an MCU and directly accessible by software functions.

For blocks representing hardware electronic circuits, they will be modelled as such although the input and output pins should not be considered as electrical connections between the blocks. The pin outputs are designed to give information about the block and the pin inputs to control each block. Blocks can be connected together to perform desired functions in a simulation or, in particular, perform digital power control loop simulations.

Right clicking on a block will open a dialog where values can be entered to configure that block. The entered dialog values are constants and will remain at the given value during a simulation. The values at the input pins however can be varied dynamically during a simulation.

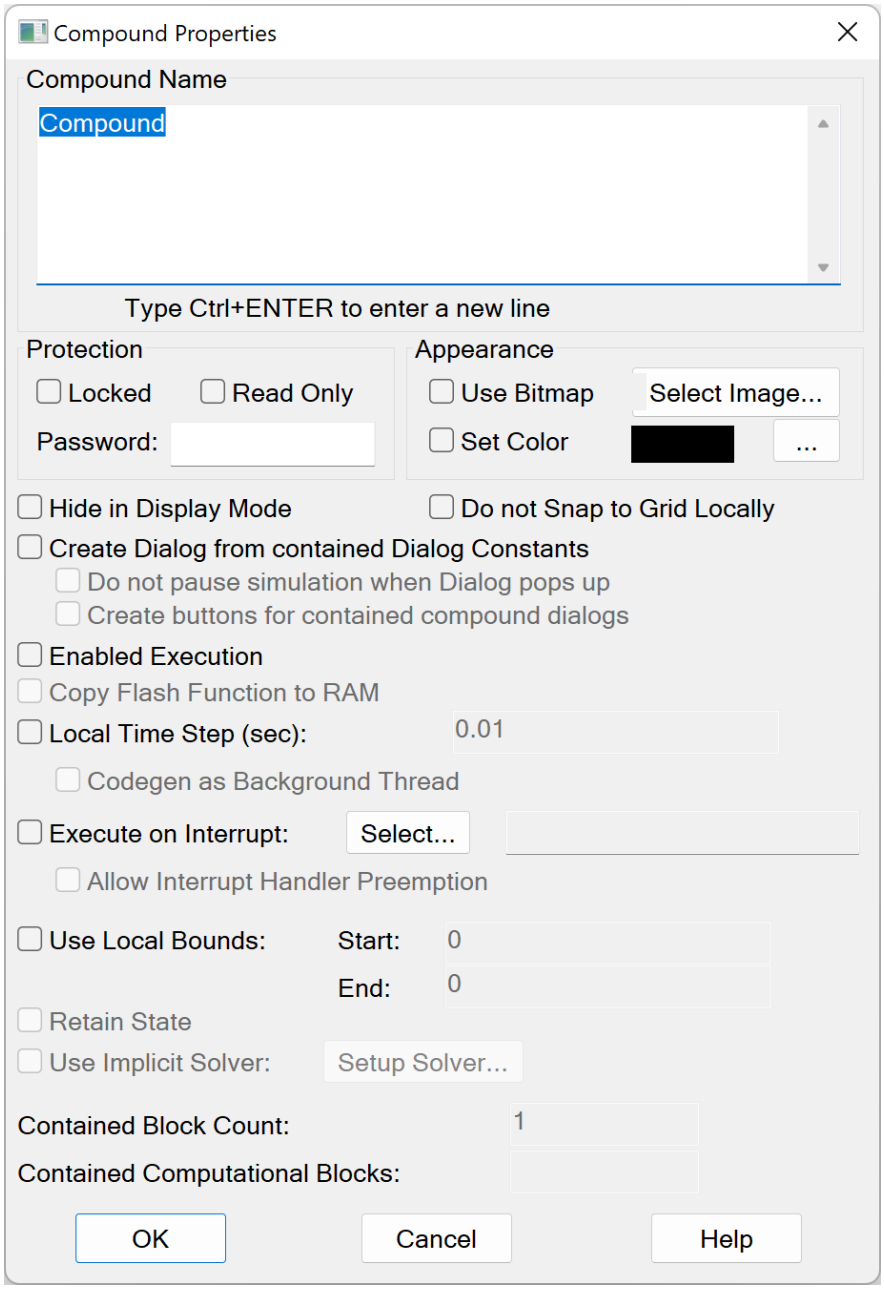
Double-left clicking on many of the blocks (power converter blocks, compensators, controllers, sensors etc) will open a second level inside the block with an interactive

circuit schematic or characteristic equation. These circuit diagrams or equations will vary during a simulation depending upon the options selected at the time.

File importing can be accessed at this second level, the import file selected, configured, viewed and/or edited.

Customizing Blocks

The blocks within the simulation environment can be customized to change their appearance by CTRL + right clicking on the block.



The compound properties dialog will appear and a customized image such as a circuit schematic can be added to change the appearance of the block.

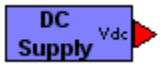
The power converter blocks already have a circuit schematic on the second level inside the block. The compensator blocks have a characteristic equation inside.

All block properties are available to be adjusted by the user however it is recommended to use the default colour settings. This will allow the visualization of the block in the familiar Embed DPD default colours.

Sources

The sources in the digital power block set are ideal sources (zero output impedance) with the possibility of summing together a large choice of options to create many types of waveforms typically seen in digital power applications.

Although the sources are voltage sources as default and so described herein, they can also be considered as ideal current or power sources, depending upon their use within a simulation.

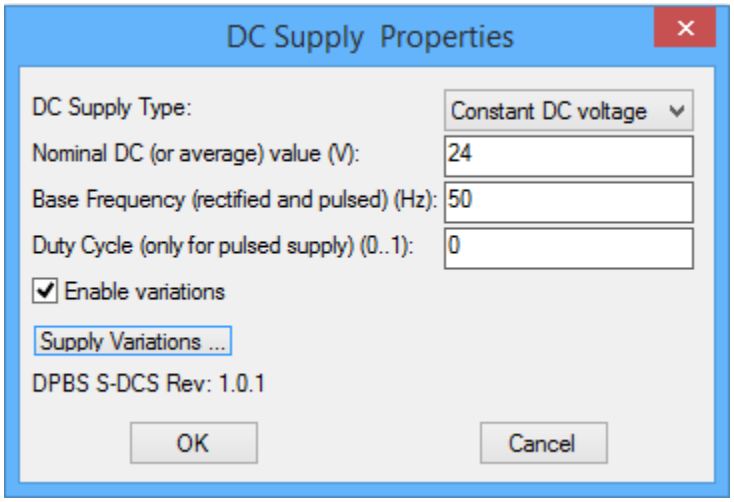


DC supply

Output Pins: **Vdc** DC supply output voltage (V)

Dialog properties:

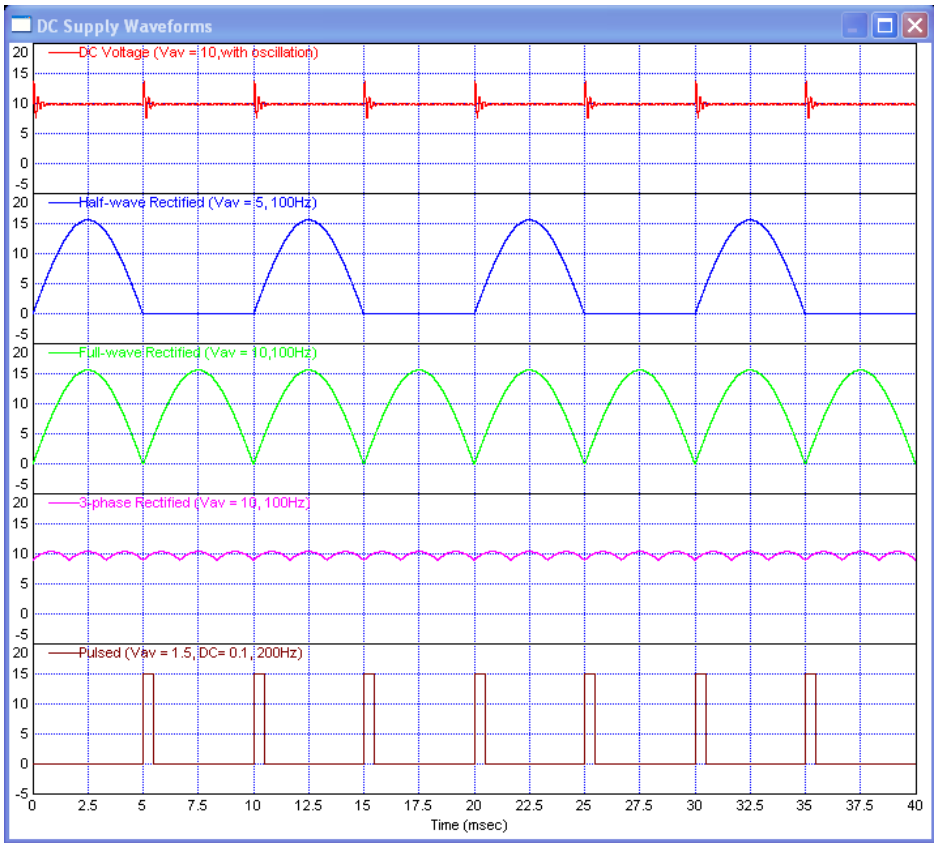
The DC supply properties menu is shown in the following box which appears when right-clicking on the block.



DC supply type:

Choose the type of DC supply. The choices are:

1. DC voltage
2. Half-wave rectified (single diode rectified)
3. Full-wave rectified (full-bridge or centre-tapped rectifier)
4. Three-phase rectified (three-phase bridge rectified)
5. Pulsed



Nominal DC (average) value:

Enter the DC voltage in Volts (this is the average value for pulsed waveforms).

Frequency:

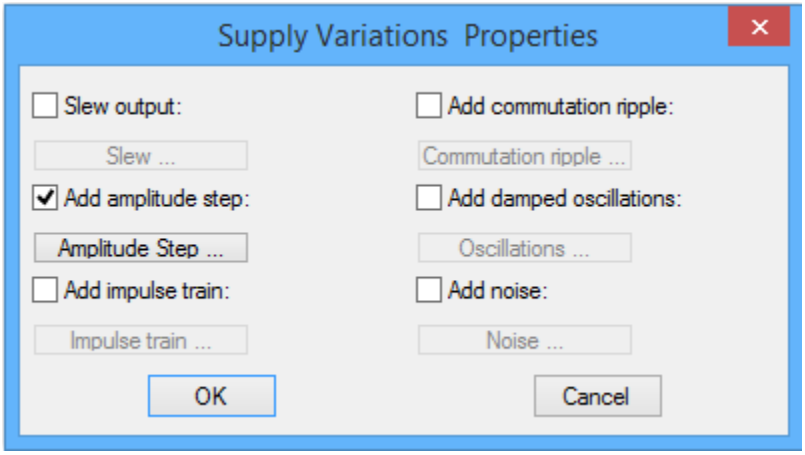
Enter the frequency of the rectified voltage ripple or pulsed waveform.

Duty cycle:

Enter the duty cycle for pulsed waveforms only.

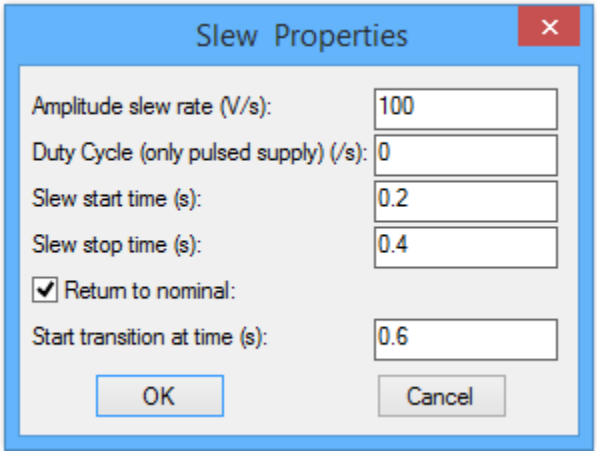
Enable supply variations:

Enables any dynamic or functional variations to the DC supply.



Slew output:

Check this box to slew (linearly vary over time) either the amplitude or the duty cycle (pulsed waveforms).



Amplitude slew rate:

Enter the desired amplitude slew rate in V/s.

Duty cycle:

Enter the desired duty cycle slew rate /s.

Slew start time:

Enter the start time of the slewed parameter in seconds.

Slew stop time:

Enter the stop time of the slewed parameter in seconds.

Return to normal:

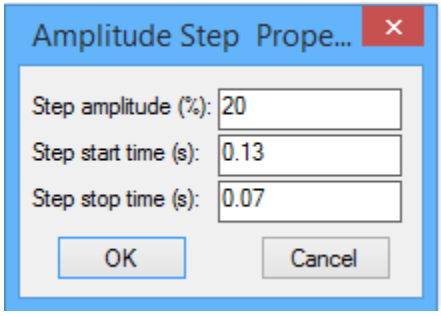
Check this box if the slewed parameters should return to the nominal setting.

Start transition time:

Enter the start time of the return slew to the nominal value.

Add amplitude step:

Check this box to add an instantaneous step to the output.



Step amplitude:

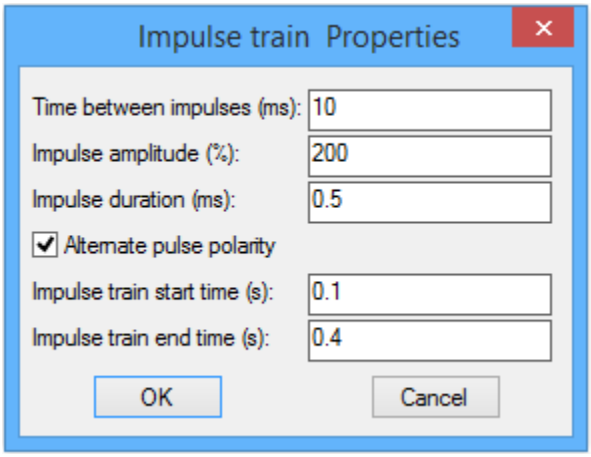
Enter the amplitude step required in percent of the DC voltage value.

Step start time:

Enter the start time of the amplitude step in seconds.

Step stop time:

Enter the end time of the amplitude step (returns to the nominal DC value) in seconds.



Add impulse train:

Check this box to add impulses to the DC supply.

Time between impulses:

Enter the period of the impulses in milliseconds.

Impulse amplitude:

Enter the impulse amplitude in percent of the DC voltage.

Impulse duration:

Enter the duration of each impulse in milliseconds.

Alternate polarity:

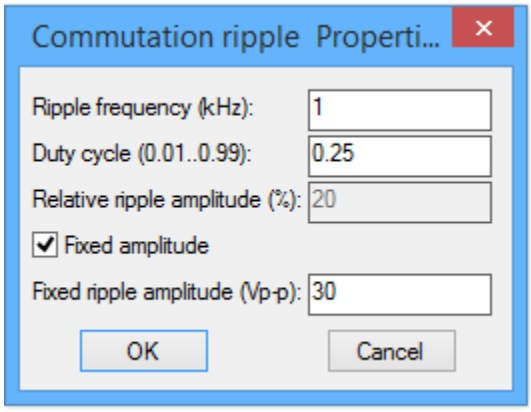
Check this box if successive impulses are to alternate their polarity.

Impulse train start time:

Enter the start time of the impulse train.

Impulse train end time:

Enter the end time of the impulse train.



Add commutation ripple:

Check this box to include a triangular commutation ripple. This type a waveform can be superimposed upon another waveform, for example, to construct a typical power converter current waveform.

Ripple frequency:

Enter the frequency of the triangular ripple in kilohertz.

Duty cycle:

Enter the duty cycle of the triangular ripple.

Relative ripple amplitude:

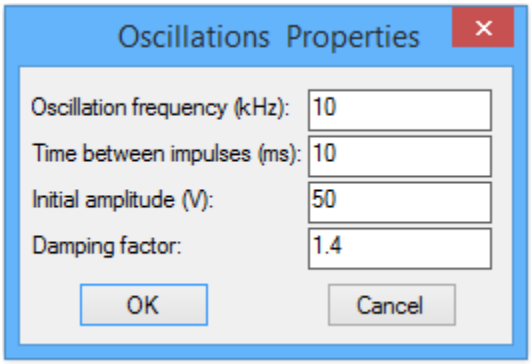
Enter the amplitude of the triangular ripple relative to the amplitude of the DC amplitude of the DC voltage.

Fixed amplitude:

Check this box to provide a fixed ripple amplitude independent upon the DC voltage.

Fixed ripple amplitude:

Enter the peak to peak amplitude in Volts.



Add damped oscillations:

Check this box to include repetitive damped oscillations. Damped oscillations would be typically seen superimposed on a voltage waveform at the instance of the switching of a power component.

Oscillation frequency:

Frequency of oscillation in kilohertz.

Time between impulses:

Repetition period of the oscillations in milliseconds..

Initial amplitude:

Initial amplitude (first peak) of the oscillations.

Damping factor:

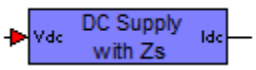
The rate at which the oscillations will be damped.

Add noise:

A noise signal can be added to the source when this box is checked.

Noise amplitude:

Enter the relative amplitude of the noise in %.

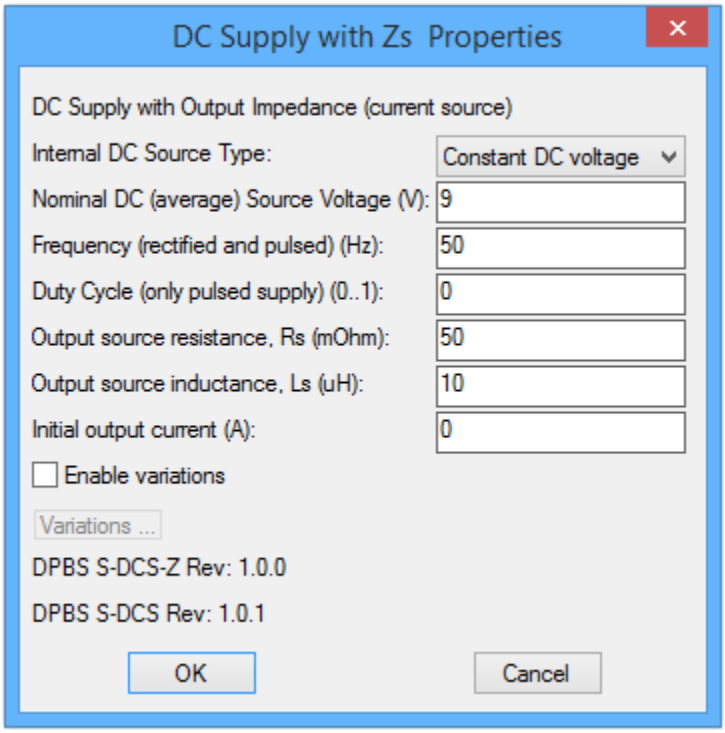


DC Supply with Source Impedance

Input Pin:	**Vdc**	Resultant source output voltage input (V).
Output Pin:	**Idc**	DC source output current (A).

Dialog properties:

The DC source with Zs properties menu is shown in the following box which appears when right-clicking on the block



The dialog is similar to the DC supply dialog except for:

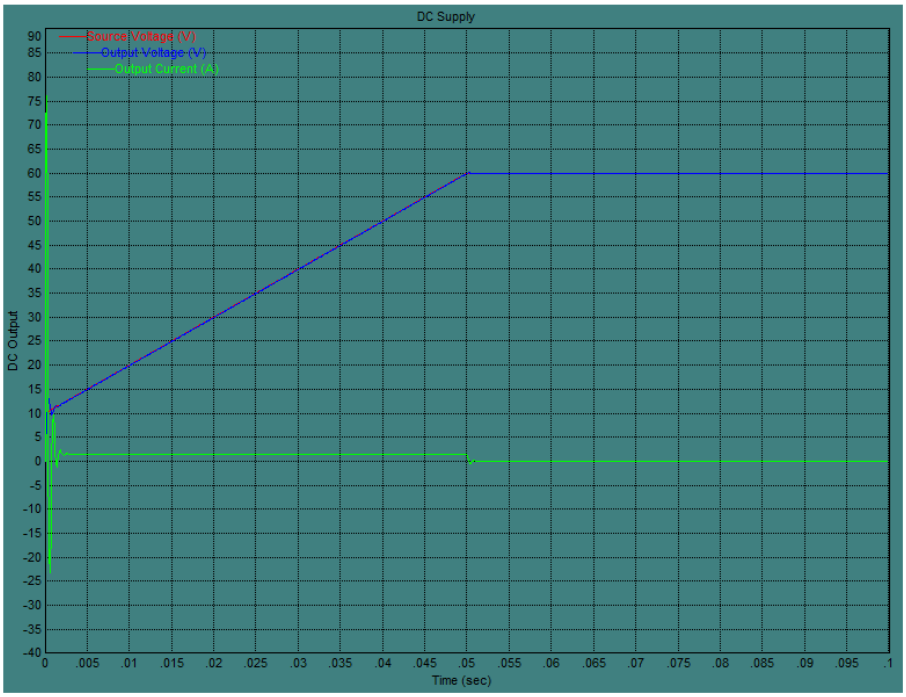
Output series source resistance:

Enter the series source resistance in milli-Ohms.

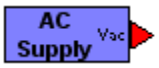
Output series source inductance:

Enter the series source inductance in micro-Henrys.

DC Supply with Output Impedance



The DC source voltage, resultant output voltage and current are given internally in the block (double-left click).

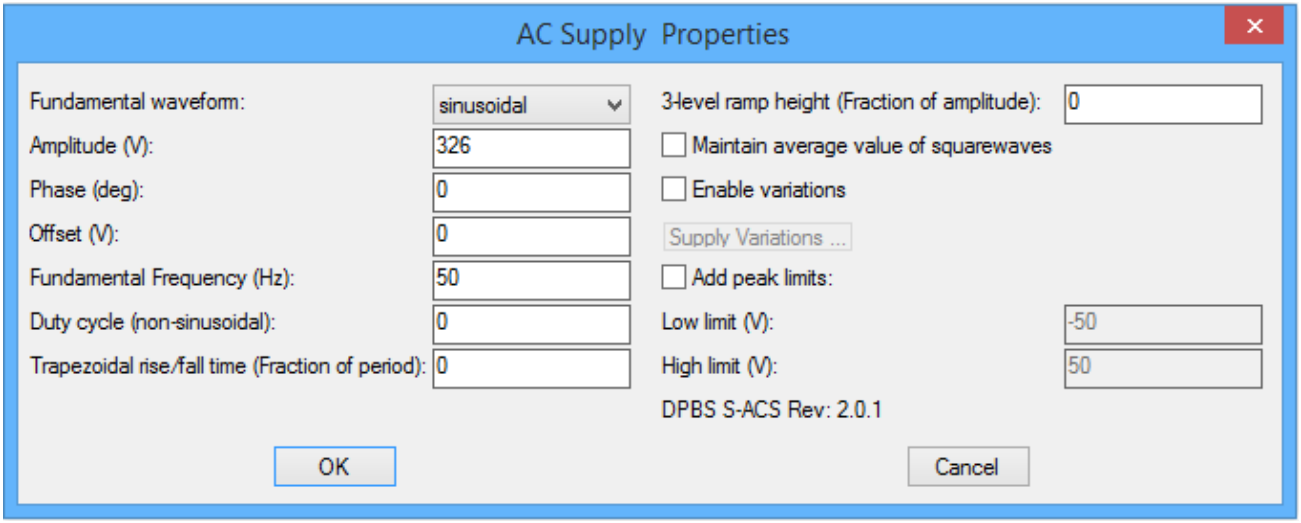


AC supply

Output Pins: **Vac** AC supply output voltage (V)

Dialog properties:

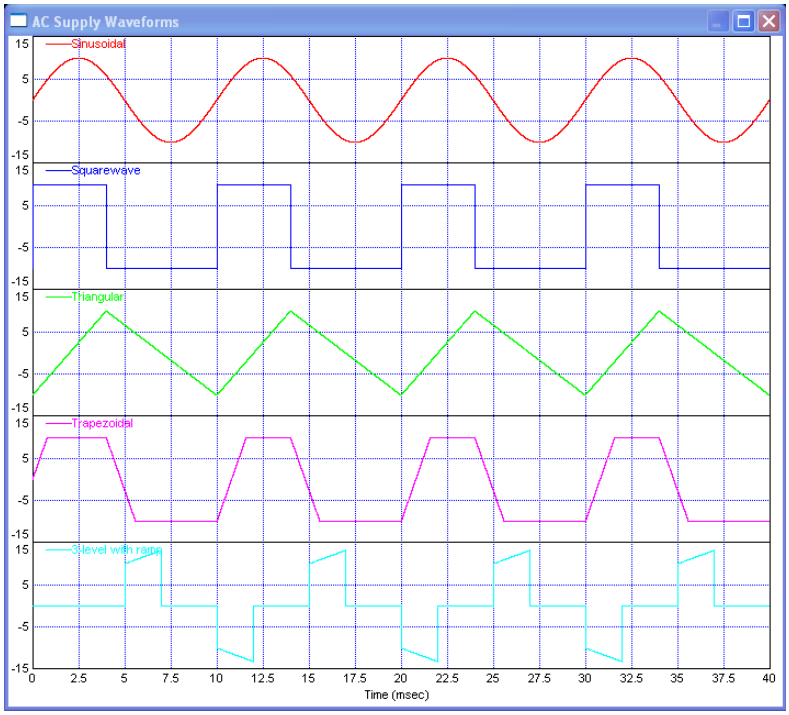
The AC supply properties menu is shown in the following box which appears when right-clicking on the block.



Fundamental waveform:

Choose the AC supply type. The choices are:

1. Sinusoidal
2. square-wave
3. triangular
4. trapezoidal
5. three-level with ramp



Amplitude:

Enter the nominal amplitude of the AC waveform in Volts.

Phase:

Enter the desired phase (delay) of the AC waveform in degrees.

Offset:

Enter the required DC offset of the AC waveform in Volts.

Frequency:

Enter the desired nominal frequency of the AC waveform in Hertz.

Duty Cycle:

Enter the desired duty cycle (not valid for sinusoidal waveforms).

Trapezoidal rise / fall time:

Enter the rise / fall time of the trapezoidal (0 = square wave).

3-level ramp height:

Enter the height of the ramp which will be added (placed on top) of the 3 level square wave.

Maintain average value of square waves:

If checked, when varying the duty cycle of square waves, the average value of the waveform will be maintained.

Add peak limits:

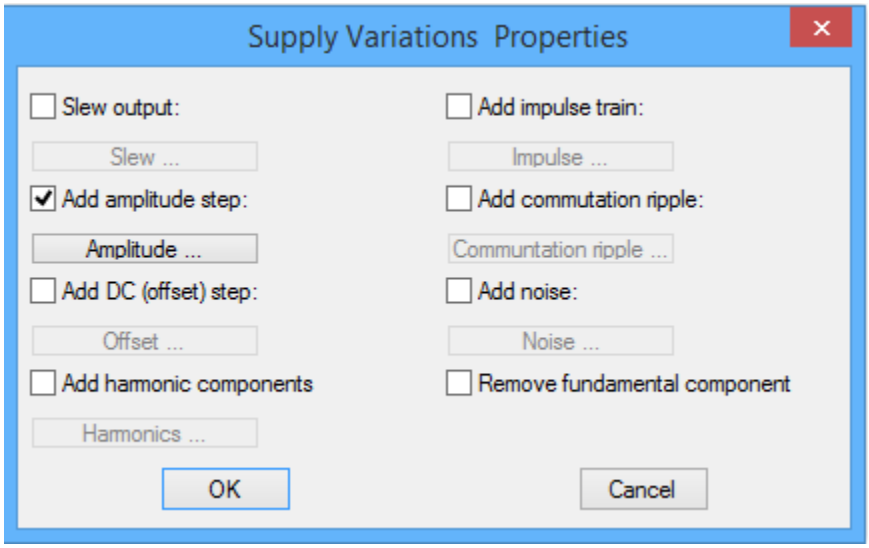
Check this box to limit the output peaks between the given limits.

Low and High limits:

Enter the high and low limits for the selected output phases.

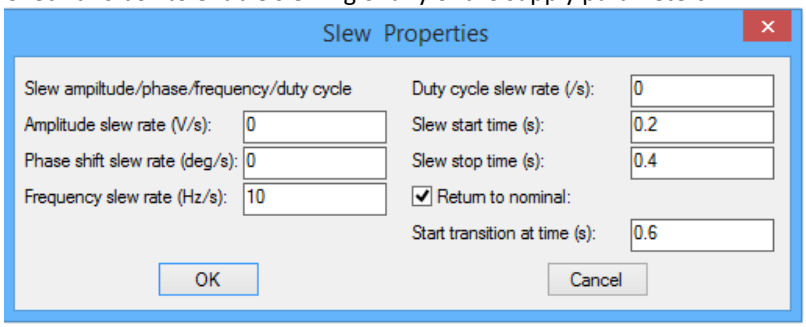
Enable supply variations:

Enables any dynamic or functional variations to the AC supply.



Slew amplitude/phase/frequency/duty cycle:

Check this box to enable slewing of any of the supply parameters.



Amplitude slew rate:

Enter the required amplitude slew rate in Volts / s.

Phase shift slew rate:

Enter the required phase difference slew rate in degrees / s.

Frequency slew rate:

Enter the required frequency slew rate in Hz / s.

Duty cycle slew rate:

Enter the required duty cycle slew rate (s^{-1}).

Slew start time:

Enter the start time of the parameter(s) slew.

Slew stop time:

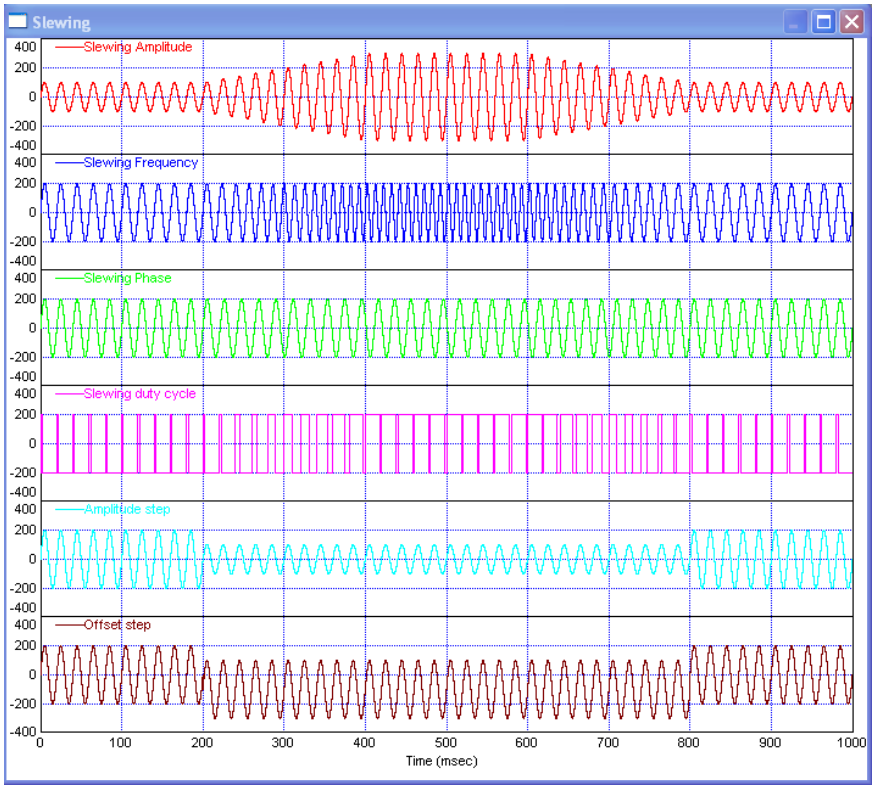
Enter the end time of the parameter(s) slew.

Return to normal:

Check this box if it is desired that the slewed parameter(s) return to their nominal values.

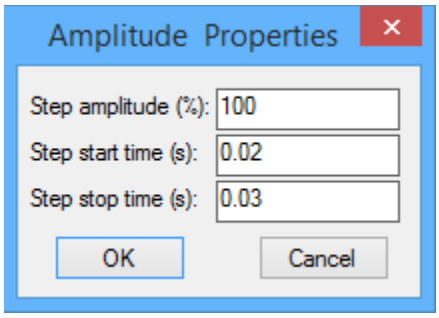
Start transition at time:

Enter the time at which the return slew should begin.



Add amplitude step:

Check this box to add an instantaneous step to the output.



Step amplitude:

Enter the amplitude step required in percent of the nominal amplitude.

Step start time:

Enter the start time of the amplitude step.

Step stop time:

Enter the end time of the amplitude step (returns to the nominal amplitude).

Add DC (offset) step:

Check this box to add a DC offset step.

DC amplitude step:

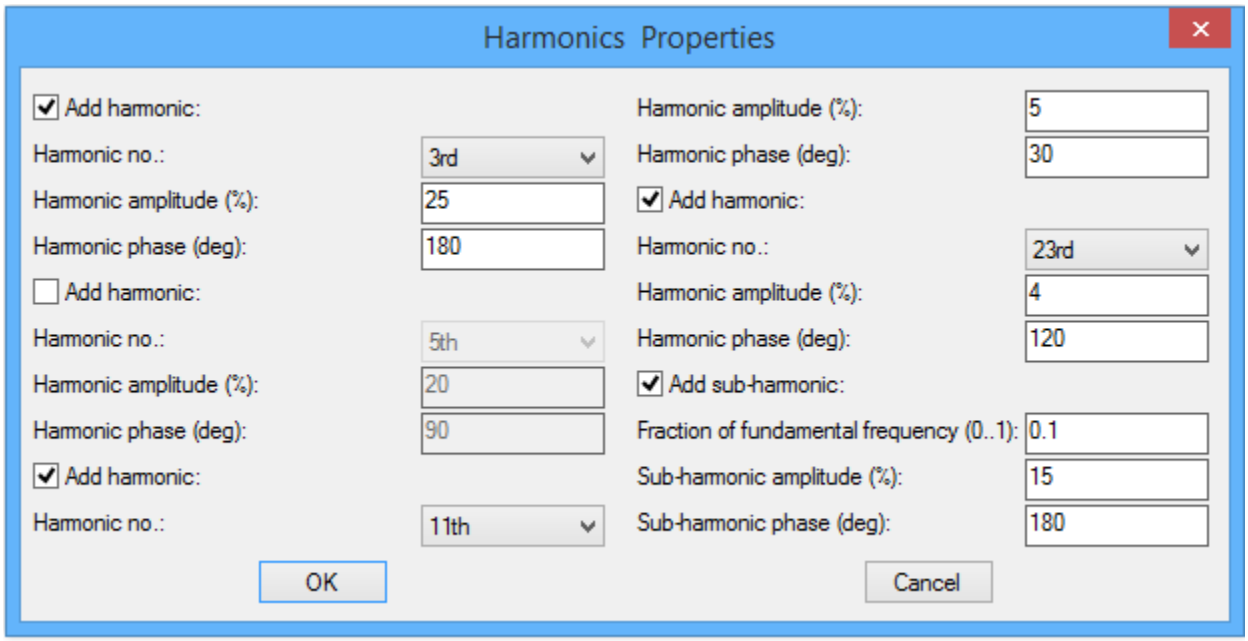
Enter the amplitude step required in percent of the nominal amplitude.

DC step start time:

Enter the start time of the step in the DC offset.

DC step stop time:

Enter the end time of the step in the DC offset.



Add harmonic:

Up to four different harmonics can be added to the waveform by enabling the respective check box.

Harmonic no.:

Select a harmonic number (multiple of the nominal frequency) from 2 to 49.

Harmonic amplitude:

Enter the harmonic amplitude in percent of the nominal amplitude for each required harmonic.

Harmonic phase:

Enter the phase in degrees of each harmonic component.

Add sub-harmonic:

A sub-harmonic component (frequency lower than the fundamental frequency) can be added to the waveform by checking this check box.

Fraction of fundamental frequency:

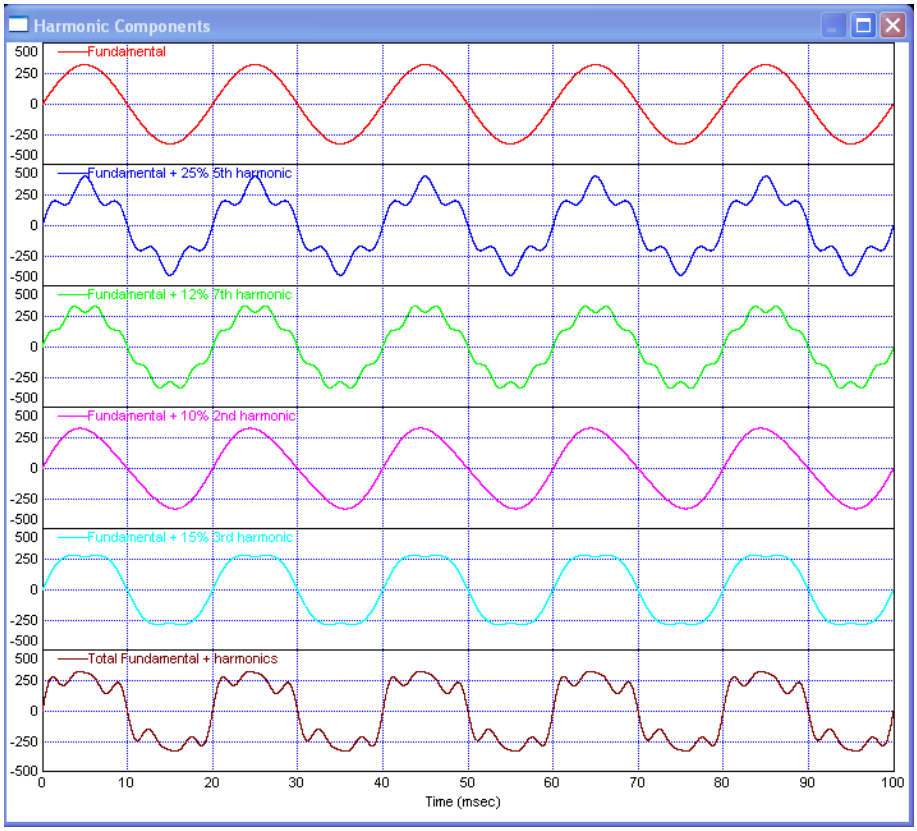
Enter the frequency of the sub-harmonic component as a fraction of the nominal (fundamental) frequency.

Sub-harmonic amplitude:

Enter the sub-harmonic amplitude in percent of the nominal amplitude.

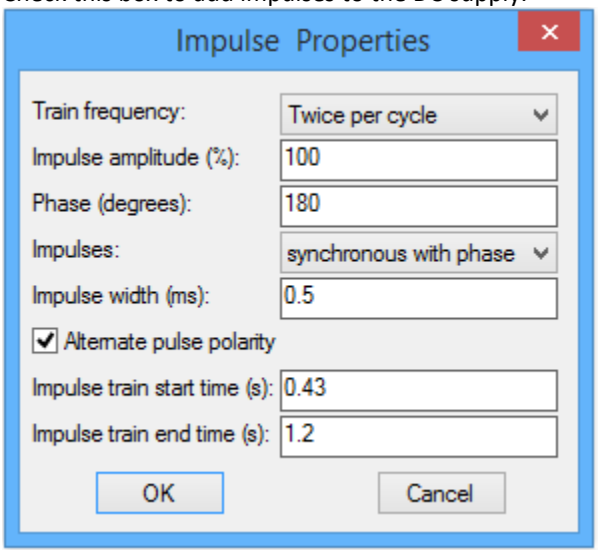
Sub-harmonic phase:

Enter the phase of the sub-harmonic component in degrees.



Add impulse train:

Check this box to add impulses to the DC supply.



Train frequency:

The frequency of the train of impulses can be selected with respect to the main waveform as follows:

1. Once only
2. Once every 4, 3 or 2 cycles.
3. Every cycle

4. 2, 3, 4, 5 or 6 times per cycle.

Impulse amplitude:

Enter the impulse amplitude in percent of the main waveform AC amplitude.

Phase (degrees):

Enter the value of the phase of the impulse train with respect to the main waveform.

Impulses:

The impulses can be selected as asynchronous to the main waveform or synchronous.

Impulse width:

Enter the width (duration) of each impulse in milliseconds.

Alternate polarity:

Check this box if successive impulses are to alternate their polarity.

Impulse train start time:

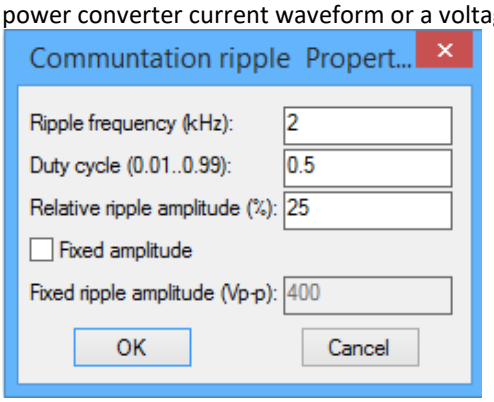
Enter the start time of the impulse train.

Impulse train end time:

Enter the end time of the impulse train.

Add commutation ripple:

Check this box to include a triangular commutation ripple. This type a waveform can be superimposed upon another waveform, for example, to construct a typical power converter current waveform or a voltage ripple.



Ripple frequency:

Enter the frequency of the triangular ripple in kilohertz.

Duty cycle:

Enter the duty cycle of the triangular ripple.

Relative ripple amplitude:

Enter the amplitude of the triangular ripple relative to the amplitude of the DC amplitude of the DC voltage.

Fixed ripple amplitude:

Check this box to provide a fixed ripple amplitude independent upon the DC voltage.

Fixed ripple amplitude:

Enter the peak to peak amplitude in Volts.

Add damped oscillations:

Check this box to include repetitive damped oscillations. Damped oscillations would be typically seen superimposed on a voltage waveform at the instance of the switching of a power component.

Oscillation frequency:

Frequency of oscillation in kilohertz.

Time between impulses:

Repetition period of the oscillations in milliseconds..

Initial amplitude:

Initial amplitude (first peak) of the oscillations.

Damping factor:

The rate at which the oscillations will be damped.

Add noise:

A noise signal can be added to the source when this box is checked.

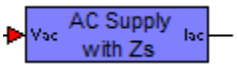
Noise amplitude:

Enter the relative amplitude of the noise in %.

Remove fundamental component from output:

Check this box if the fundamental component is to be removed from the AC supply output (only the individual harmonic components and / or other components remain).

Contents - Simulation



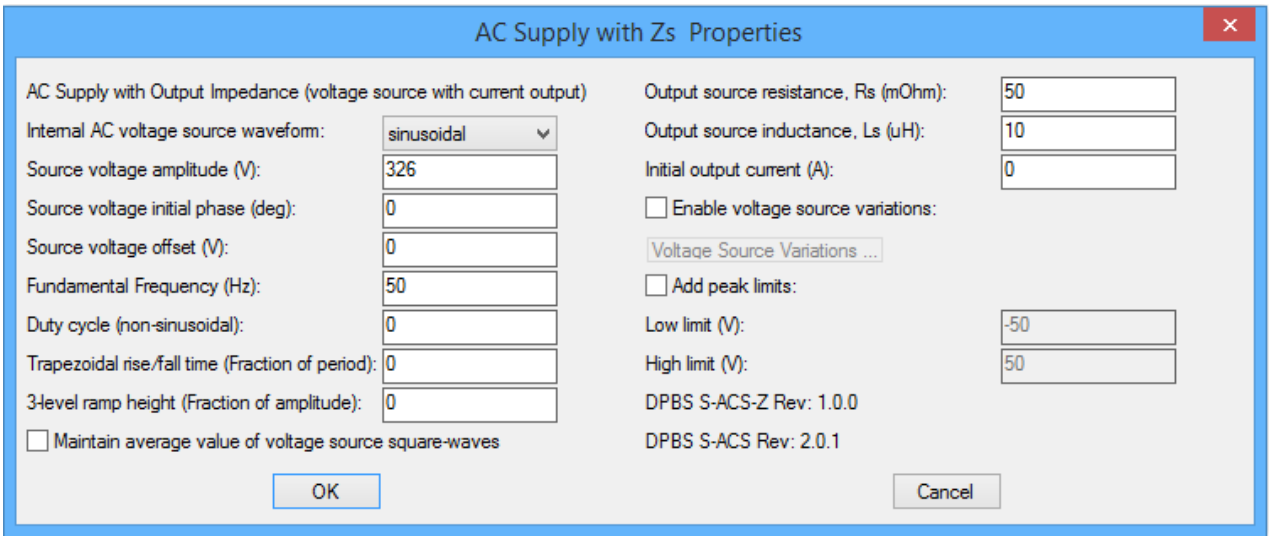
AC Supply with Source Impedance

Input Pins: **Vac** Output voltage (V) of the system input to the supply with impedance.

Output Pins: **Iac** AC supply output current (A).

Dialog properties:

The AC Supply with Zs properties menu is shown in the following box which appears when right-clicking on the block



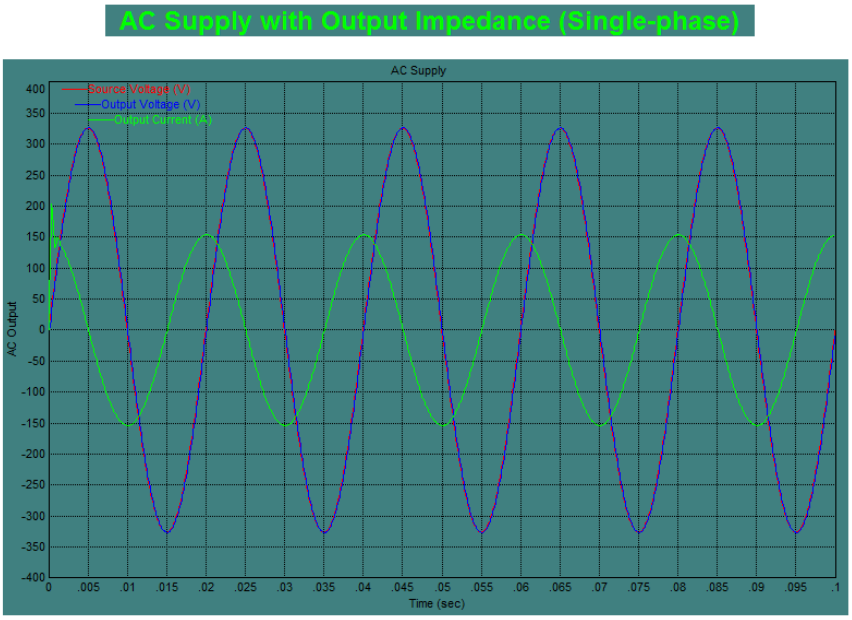
The dialog is similar to the AC supply dialog except for:

Output series source resistance:

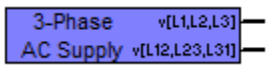
Enter the series source resistance in milli-Ohms.

Output series source inductance:

Enter the series source inductance in micro-Henrys.



The AC source voltage, resultant output voltage and current are given internally in the block.



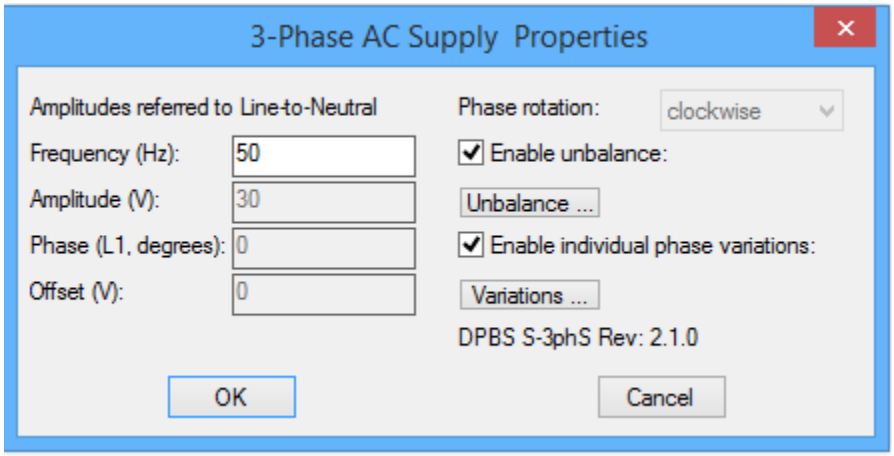
Three-phase AC supply

Output Pins: **V[L1, L2, L3]** Three-phase output line-to-neutral voltage (V), vector (rows = 1, columns = 3).

V[L12,L23,L31] Three-phase line-to-line voltages (V), vector (rows = 1, columns = 3).

Dialog properties:

The three-phase AC supply properties menu is shown in the following box which appears when right-clicking on the block.



Frequency:

Enter the nominal default frequency of the AC waveform in Hertz.

Amplitude:

Enter the nominal default amplitude of the AC waveform in Volts.

Phase:

Enter the phase in degrees with reference to phase L1. In the default case here, the phase lag of the other two phases will be phase + 120° and phase + 240°.

Offset:

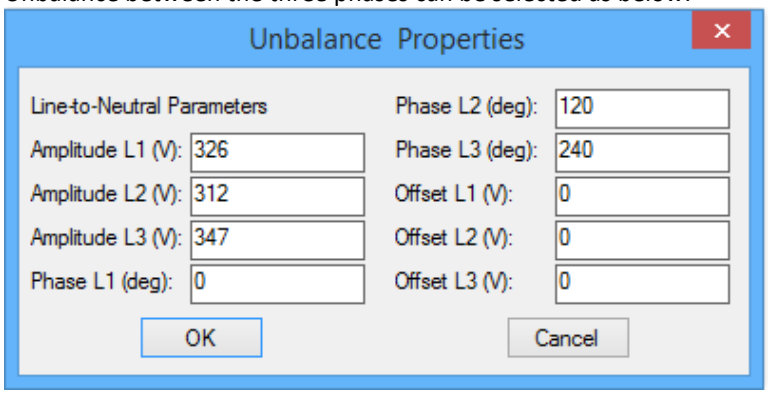
Enter the default DC offset of the AC waveform in Volts.

Phase Rotation:

The phase sequence can be selected as clockwise or anti-clockwise.

Enable unbalance:

Unbalance between the three phases can be selected as below:



Amplitude L1, L2 and L3:

Enter the nominal amplitude individually for the three phases of the AC waveforms in Volts.

Phase L1, L2 and L3:

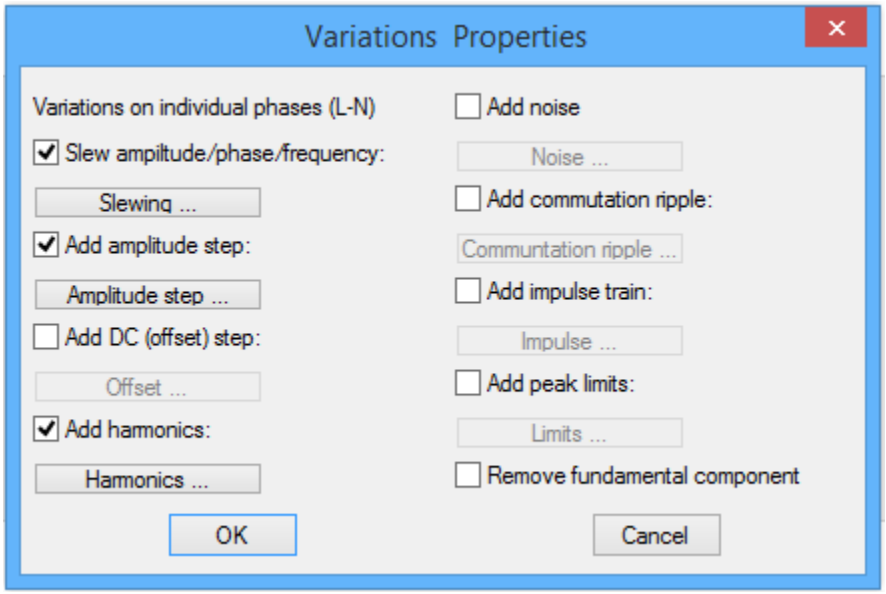
Enter the nominal phase difference individually for the three phases of the AC waveform in degrees.

Offset L1, L2 and L3:

Enter the default DC offset of the three phases individually.

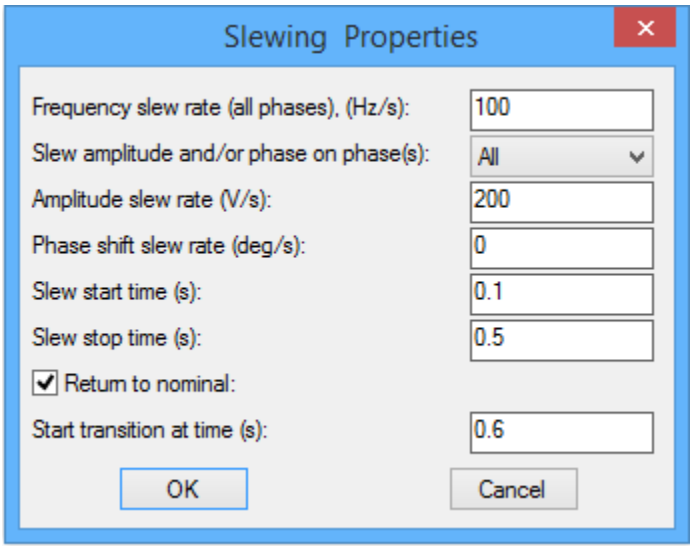
Enable individual phase variations:

Check this box to enable all the possible variations of the three-phase AC supply, otherwise the default values or the unbalanced values are used.



Slew amplitude/phase/frequency:

Check this box to enable slewing of any of the supply parameters.



Slew phase(s):

Select the phase or phases to be slewed at the set rate.

Amplitude slew rate:

Enter the required amplitude slew rate in Volts / s.

Phase shift slew rate:

Enter the required phase difference slew rate in degrees / s.

Frequency slew rate:

Enter the required frequency slew rate in Hz / s.

Slew start time:

Enter the start time of the parameter(s) slew.

Slew stop time:

Enter the end time of the parameter(s) slew.

Return to normal:

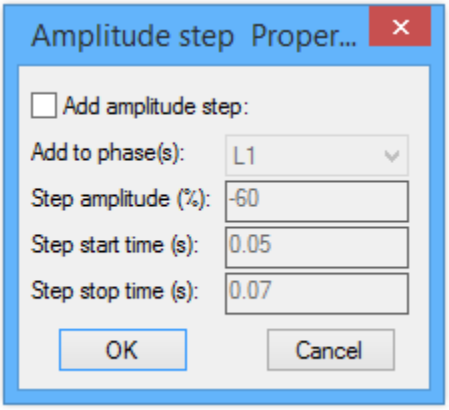
Check this box if it is desired that the slewed parameter(s) return to their nominal values.

Start transition at time:

Enter the time at which the return slew should begin.

Add amplitude step:

Check this box to add an instantaneous step to the output.



Add to phase(s):

Select the phase or phases to add the amplitude step.

Step amplitude:

Enter the amplitude step required in percent of the nominal amplitude.

Step start time:

Enter the start time of the amplitude step.

Step stop time:

Enter the end time of the amplitude step (returns to the nominal amplitude).

Add DC (offset) step:

Check this box to add a DC offset step.

Add to phase(s):

Select the phase or phases to add the offset step.

DC amplitude step:

Enter the amplitude step required in percent of the nominal amplitude.

DC step start time:

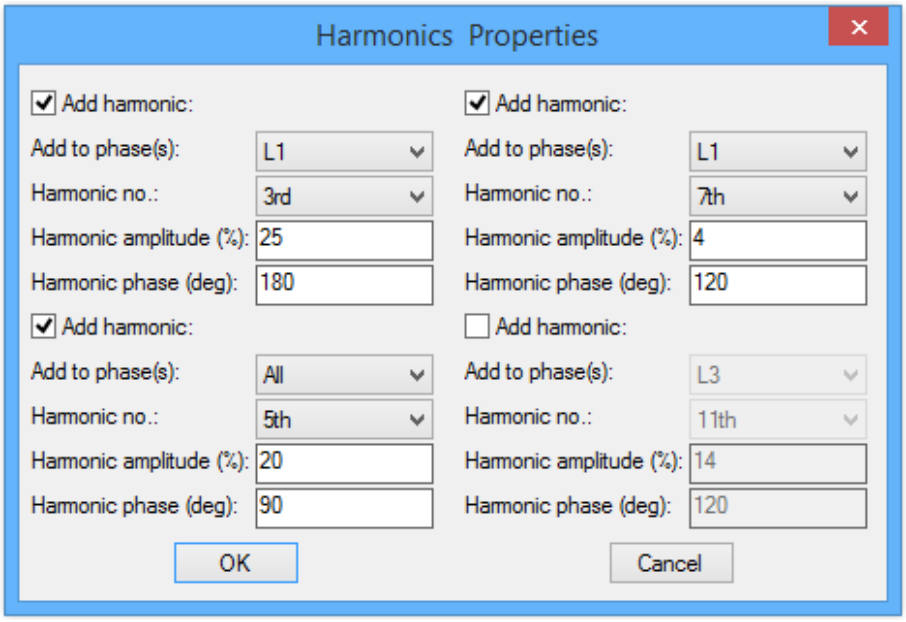
Enter the start time of the step in the DC offset.

DC step stop time:

Enter the end time of the step in the DC offset.

Add harmonics:

Up to four different harmonics can be added to the waveform by enabling the respective check box.



Add to phase(s):

Select the phase or phases to add the harmonic component.

Harmonic no.:

Select a harmonic number (multiple of the nominal frequency) from 2 to 49.

Harmonic amplitude:

Enter the harmonic amplitude in percent of the nominal amplitude for each required harmonic.

Harmonic phase:

Enter the phase in degrees of each harmonic component.

Add noise:

A noise signal can be added to the source when this box is checked.

Add to phase(s):

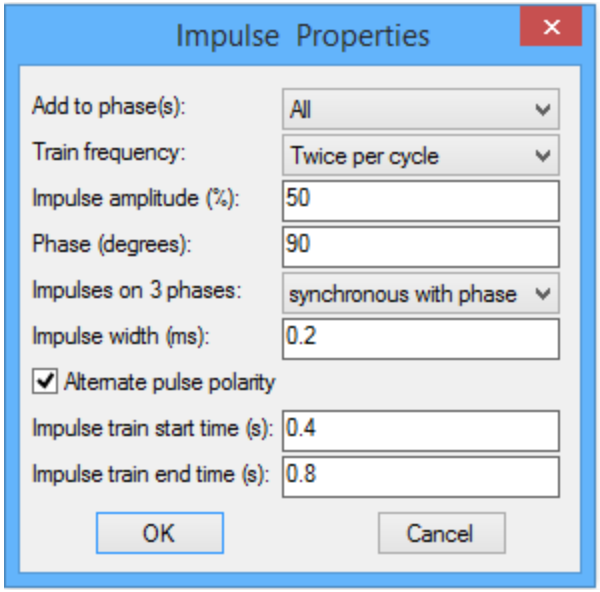
Select the phase or phases to add the noise component.

Noise amplitude:

Enter the relative amplitude of the noise in %.

Add impulse train:

Check this box to add impulses to the AC supply.



Train frequency:

The frequency of the train of impulses can be selected with respect to the main waveform as follows:

1. Once only
2. Once every 4, 3 or 2 cycles.
3. Every cycle
4. 2, 3, 4, 5 or 6 times per cycle.

Impulse amplitude:

Enter the impulse amplitude in percent of the main waveform AC amplitude.

Phase (degrees):

Enter the value of the phase of the impulse train with respect to the main waveform.

Impulses:

The impulses can be selected as asynchronous to the main waveform or synchronous.

Impulse width:

Enter the width (duration) of each impulse in milliseconds.

Alternate polarity:

Check this box if successive impulses are to alternate their polarity.

Impulse train start time:

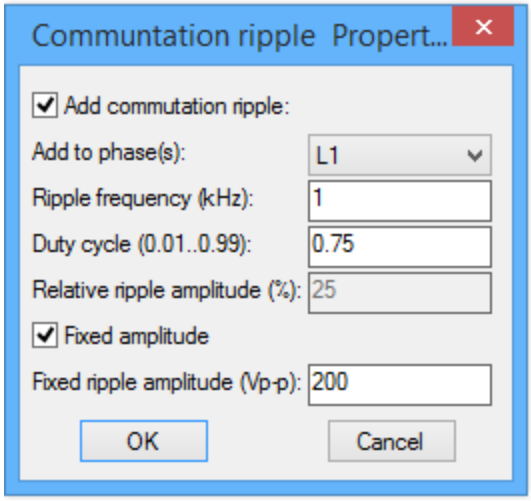
Enter the start time of the impulse train.

Impulse train end time:

Enter the end time of the impulse train.

Add commutation ripple:

Check this box to include a triangular commutation ripple. This type a waveform can be superimposed upon another waveform, for example, to construct a typical power converter current waveform or a voltage ripple.



Add to phase(s):

Select the phase or phases to add the commutation ripple component.

Ripple frequency:

Enter the frequency of the triangular ripple in kilohertz.

Duty cycle:

Enter the duty cycle of the triangular ripple.

Relative ripple amplitude:

Enter the amplitude of the triangular ripple relative to the amplitude of the DC amplitude of the DC voltage.

Fixed amplitude:

Check this box to provide a fixed ripple amplitude independent upon the DC voltage.

Fixed ripple amplitude:

Enter the peak to peak amplitude in Volts.

Add peak limits:

Check this box to limit the output peaks between the given limits.

Add to phase(s):

Select the phase or phases to include peak limits.

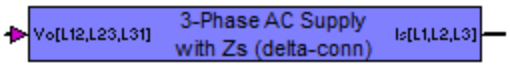
Low and High limits:

Enter the high and low limits for the selected output phases.

Remove fundamental component from output:

Check this box if the fundamental component is to be removed from the three phases of the AC supply output (only the individual harmonic components and / or other components remain).

Contents - Simulation



Three-phase AC supply with Zs (Delta-connected)

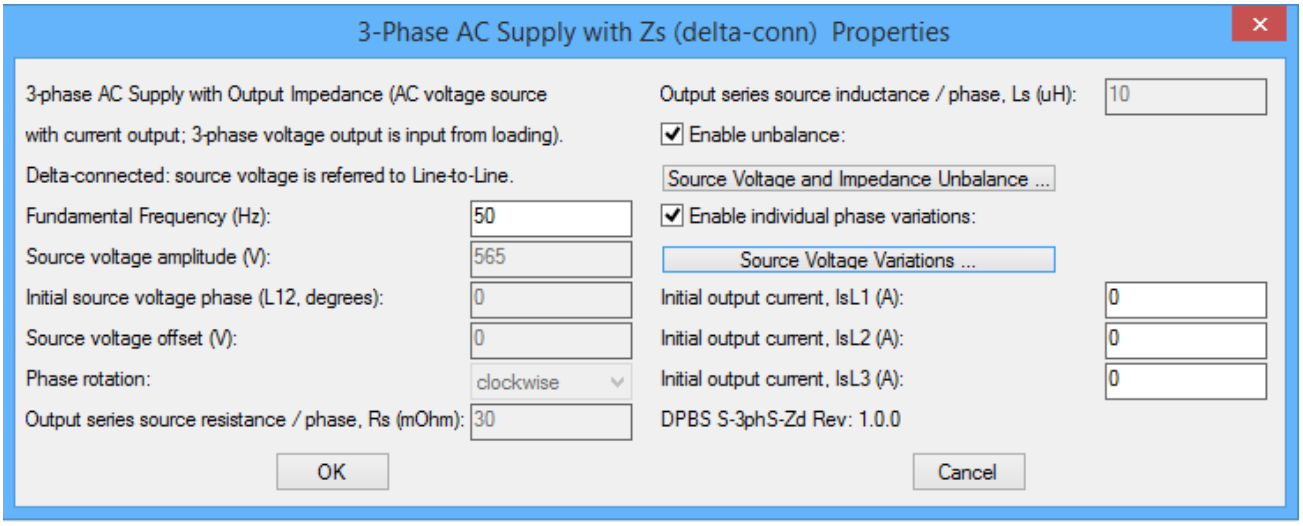
This block simulates a three-phase AC supply with internal source impedance (Zs). The output of the block is the supply current and the input to the block is the source output voltage generated on the supply loading. The block can be completely configured as a balanced supply or unbalanced including unbalanced source impedances.

Input Pins: **Vo[L12, L21, L31]** The 3-phase effective output line-to-line voltage (V), vector (rows = 1, columns = 3).

Output Pins: **Is[L1, L2, L3]** The 3-phase output line current (A), vector (rows = 1, columns = 3).

Dialog properties:

The three-phase AC supply with Zs (delta-connected) properties menu is shown in the following box which appears when right-clicking on the block.



Fundamental Frequency:

Enter the nominal default frequency of the AC waveform in Hertz.

Amplitude:

Enter the nominal default amplitude of the AC waveform in Volts.

Initial source voltage Phase:

Enter the initial phase in degrees with reference to the line-to-line phase L12.

Source voltage Offset:

Enter the default DC offset of the AC waveform in Volts.

Phase Rotation:

The phase sequence can be selected as clockwise or anti-clockwise.

Output series source resistance:

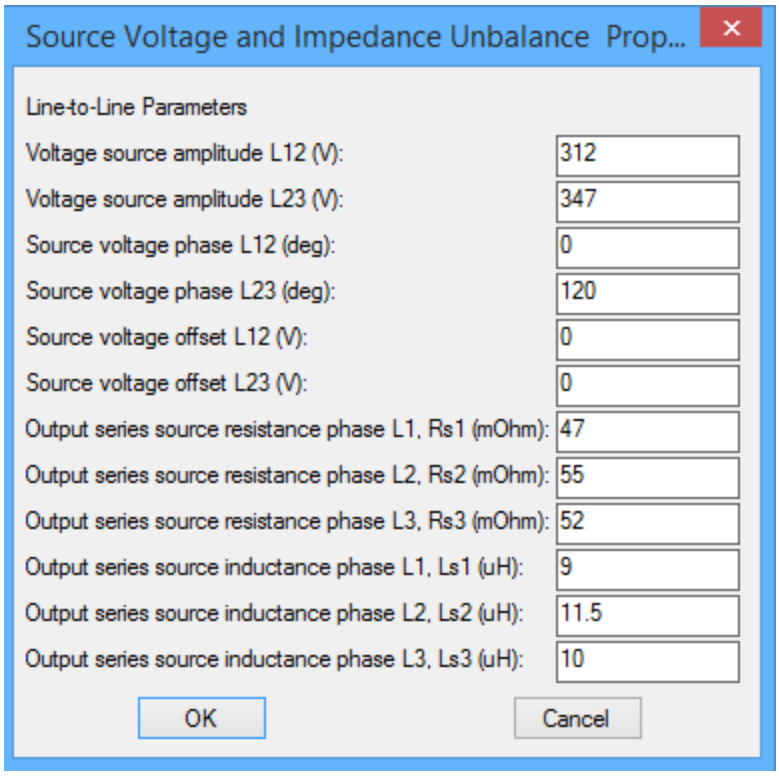
Enter the series source resistance in milli-Ohms.

Output series source inductance:

Enter the series source inductance in micro-Henrys.

Enable unbalance:

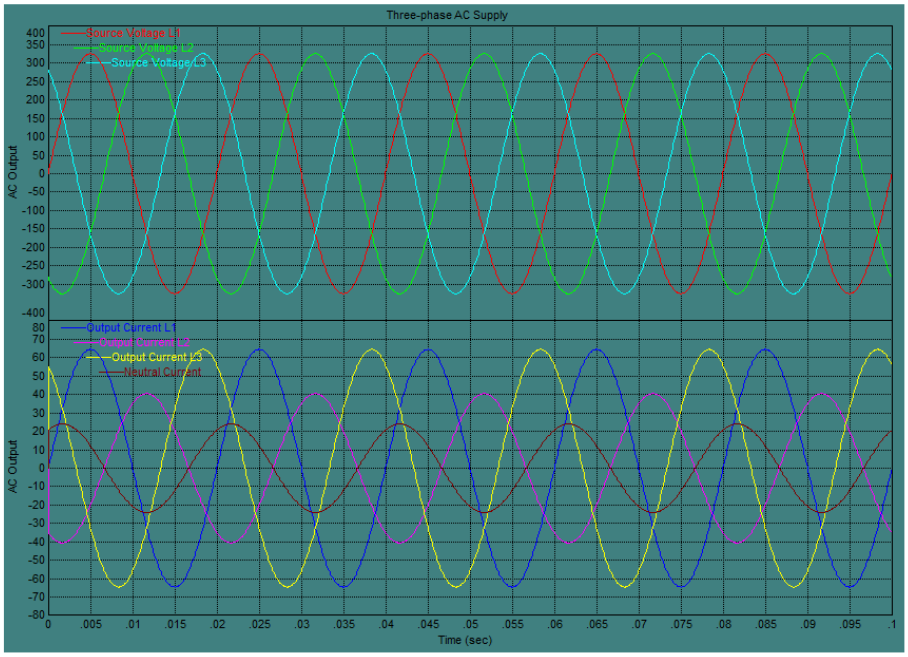
Unbalance between the three phases can be selected in the same manner for the three-phase AC supply except that the unbalance can also be set for the source impedance as shown in the following dialog:



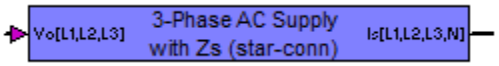
Enable individual phase variations:

Check this box to enable all the desired variations of the three-phase AC supply, otherwise the default values or the unbalanced values are used. This set-up and dialog is identical to the [three-phase AC supply].

Three-phase AC Supply with Output Impedance



The 3-phase AC source waveforms can be viewed internally in the block (double-left click).



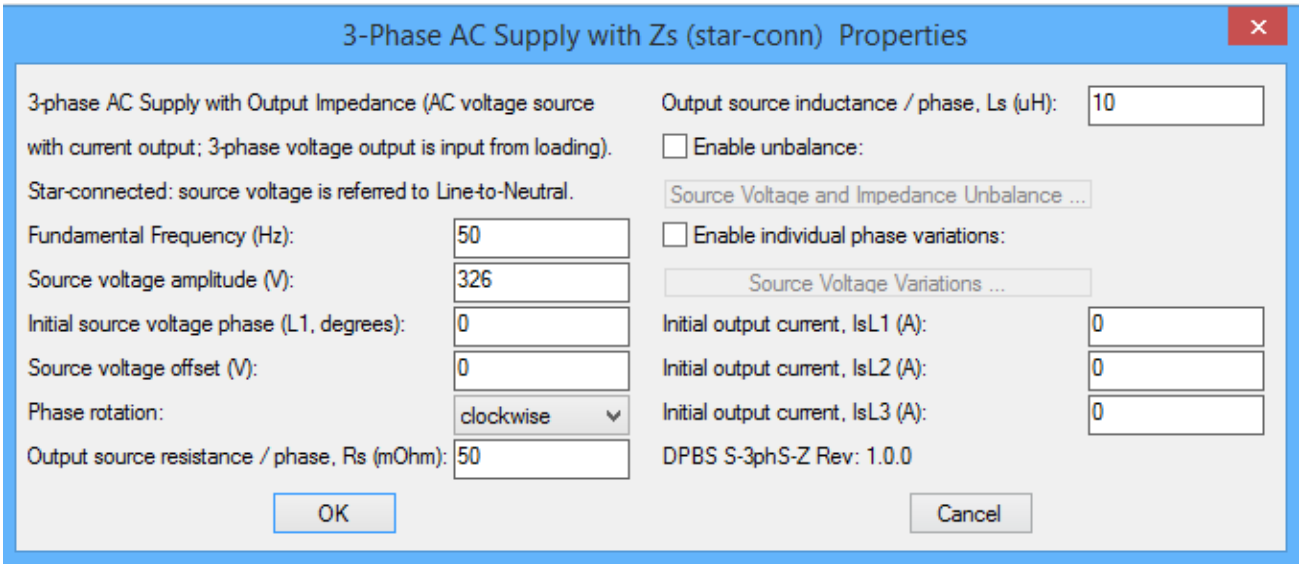
Three-phase AC supply with Zs (Y-connected)

Input Pins: **Vo[L1, L2, L3]**The 3-phase output line-to-neutral voltages (V), vector (rows = 1, columns = 3).

Output Pins: **Is[L1, L2, L3]** The 3-phase output line currents (A), vector (rows = 1, columns = 3).

Dialog properties:

The three-phase AC supply with Zs properties menu is shown in the following box which appears when right-clicking on the block.



Fundamental Frequency:

Enter the nominal default frequency of the AC waveform in Hertz.

Amplitude:

Enter the nominal default amplitude of the AC waveform in Volts.

Initial source voltage Phase:

Enter the initial phase in degrees with reference to the phase voltage L1.

Source voltage Offset:

Enter the default DC offset of the AC waveform in Volts.

Phase Rotation:

The phase sequence can be selected as clockwise or anti-clockwise.

Output source resistance / phase:

Enter the per phase series source resistance in milli-Ohms.

Output source inductance / phase:

Enter the per phase series source inductance in micro-Henrys.

Enable unbalance:

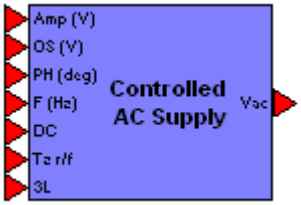
Unbalance between the three phases can be selected in the same manner for the three-phase AC supply and the delta-connected 3-phase supply with Zs.

Enable individual phase variations:

Check this box to enable all the desired variations of the three-phase AC supply, otherwise the default values or the unbalanced values are used. This set-up and dialog is identical to the three-phase AC supply.

Initial output current:

Enter the initial output current of each phase in amperes.

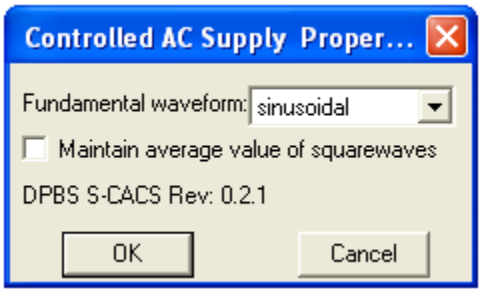


Controlled AC supply

Input Pins:	**Amp**	Set the amplitude of the AC supply using this pin.
	OS	Set the DC offset of the AC supply output using this pin.
	PH	Set the phase of the AC supply output using this pin.
	F	Set the frequency of the AC supply output using this pin.
	DC	Set the duty cycle of the AC supply (non-sinusoidal) output using this pin.
	Tz r/f	Set the rise/fall time of the trapezoidal AC supply output using this pin.
	3L	Set the amplitude of the ramp of the 3-level AC supply output using this pin.
Output Pins:	**Vac**	AC supply output voltage (V).

Dialog properties:

The controlled AC supply properties menu is shown in the following box which appears when right-clicking on the block.



This block is similar to the AC supply block except that the parameters can be varied using the input pins.

Fundamental waveform:

Choose the AC supply type. The choices are:

1. Sinusoidal
2. square-wave
3. triangular
4. trapezoidal
5. three-level with ramp

Contents - Simulation

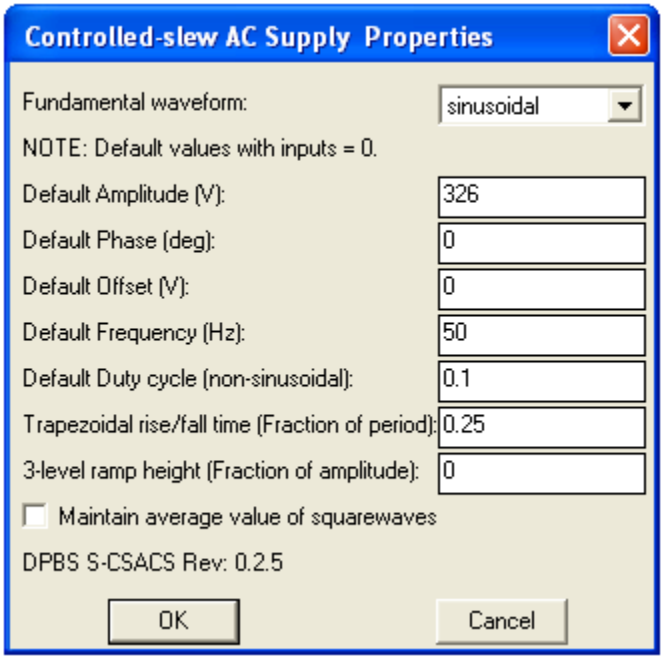


Controlled-slew AC supply

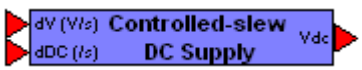
Input Pins:	**dV**	Control the rate of change of amplitude of the AC supply using this pin.
	d**OS**	Control the rate of change offset of the AC supply output using this pin.
	dPH	Control the rate of change of phase of the AC supply output using this pin.
	dF	Control the rate of change frequency of the AC supply output using this pin.
	dDC	Control the rate of change of duty cycle of the AC supply (non-sinusoidal) output using this pin.
Output Pins:	**Vac**	AC supply output voltage (V).

Dialog properties:

The controlled-slew AC supply properties menu is shown in the following box which appears when right-clicking on the block



The base values of the supply are set in the dialog similar to the AC supply block. The value at the input pins will vary these base values at the rate of the input value.



Controlled-slew DC supply

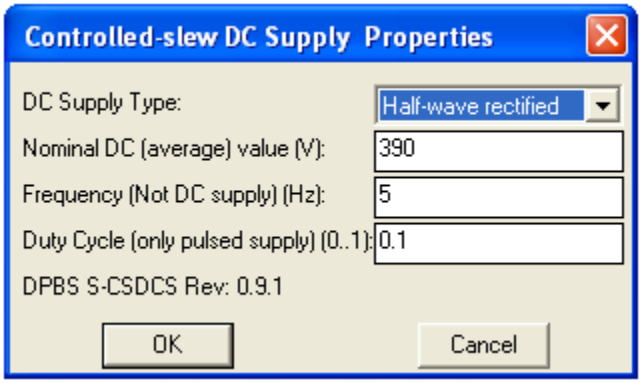
Input Pins: **dV** Control rate of change of amplitude of the DC supply using this pin.

d**DC** Control the rate of change of duty cycle of the DC supply (only pulsed supply) output using this pin.

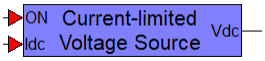
Output Pins: **Vdc** DC output voltage.

Dialog properties:

The controlled-slew DC supply properties menu is shown in the following box which appears when right-clicking on the block



The base values of the supply are set in the dialog similar to the DC supply block. The value at the input pins will vary the output voltage and duty cycle (for pulsed waveforms) at the rate of the input values.



Current-limited DC Voltage Source

This DC source provides a constant output voltage until the output current reaches the current limit value, at which point the output current will be maintained constant (limited). The source can be set as a positive or negative DC voltage source.

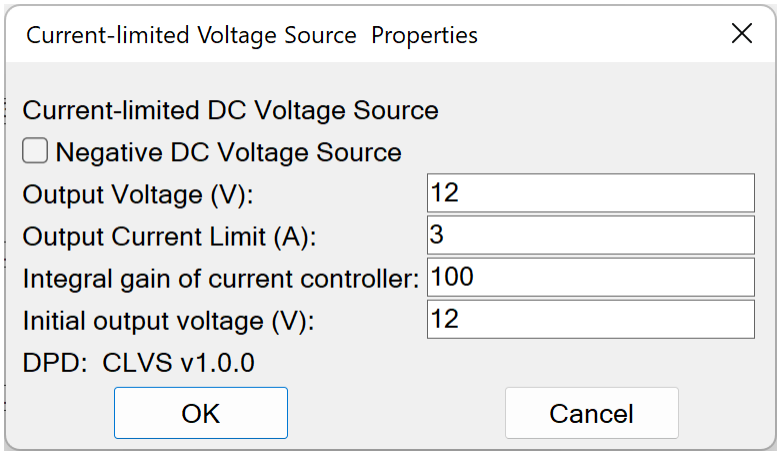
Input Pins: **EN** Enables the source output and the internal integrator.

Idc Source output current input in order to limit the output voltage.

Output Pins: **Vdc** Source output voltage.

Dialog properties:

The current-limited voltage source properties menu is shown in the following box which appears when right-clicking on the block



Negative DC Voltage Source:

Select this for a negative DC voltage source. The output current at the input pin must in this case also be negative.

Output voltage:

Enter the nominal DC output voltage in Volts.

Output current limit:

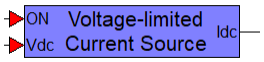
Enter the value at which the output voltage will begin to reduce in order to regulate the output current at this value.

Integral gain of current controller:

Enter the integral gain of the internal integral controller.

Initial output voltage:

Enter the initial (and reset) voltage of the source.



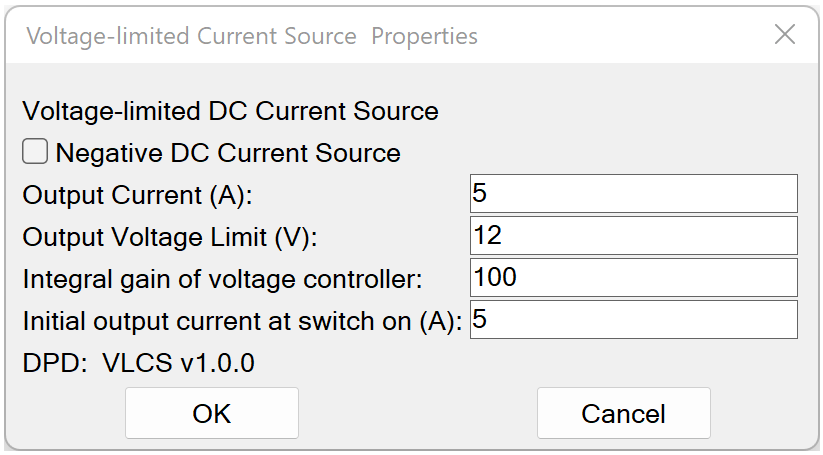
Voltage-limited DC Current Source

This DC source provides a constant output current until the output voltage across a load reaches the limiting voltage value, at which point the output voltage will be maintained constant (limited). The source can be set as a positive or negative DC current source.

Input Pins:	**EN**	Enables the source output and the internal integrator.
	Vdc	Source output voltage input in order to limit the output current.
Output Pins:	**Idc**	Source output current.

Dialog properties:

The voltage-limited current source properties menu is shown in the following box which appears when right-clicking on the block



Negative DC Current Source:

Select this for a negative DC current source. The output voltage at the input pin must in this case also be negative.

Output current:

Enter the nominal DC output voltage in Volts.

Output voltage limit:

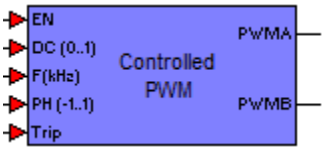
Enter the value at which the output current will begin to reduce in order to regulate the output voltage to maintain a constant output current.

Integral gain of voltage controller:

Enter the integral gain of the internal integral controller.

Initial output current:

Enter the initial (and reset) output current of the source.



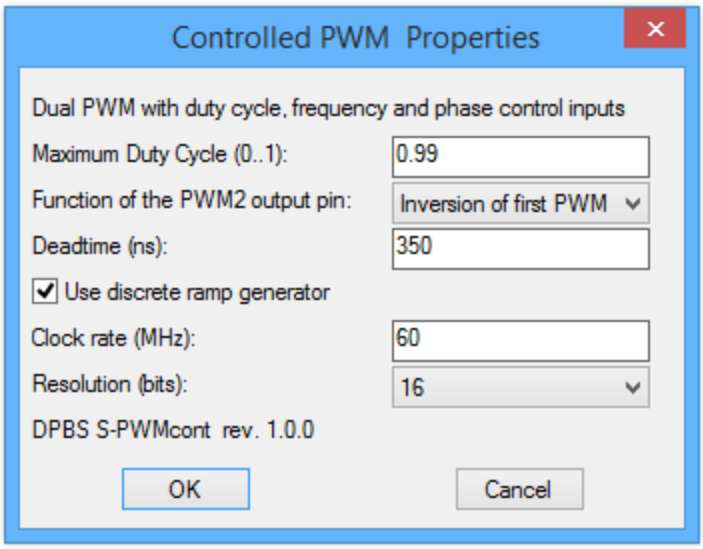
Controlled PWM

The controlled PWM block enables the configuration of generic dual PWM outputs and controlled by duty cycle, frequency, phase and trip inputs.

Input Pins:	**EN**	Enables the internal ramp generation and the two PWM outputs
	DC	Duty Cycle control input from 0 to 1.
	F	PWM frequency control input in kHz.
	PH	Phase control input to control the phase shift between PWMA and PWMB (-1 to 1 corresponds to -360 to 360 degrees).
	Trip	Trip input. A value ≥ 1 at this input will immediately set both PWM outputs to zero.
Output Pins:	**PWMA**	Main PWM output.
	PWMB	Secondary PWM output.

Dialog properties:

The controlled PWM properties menu is shown in the following box which appears when right-clicking on the block



Maximum duty cycle:

The duty cycle of both PWM outputs can be limited to this given value.

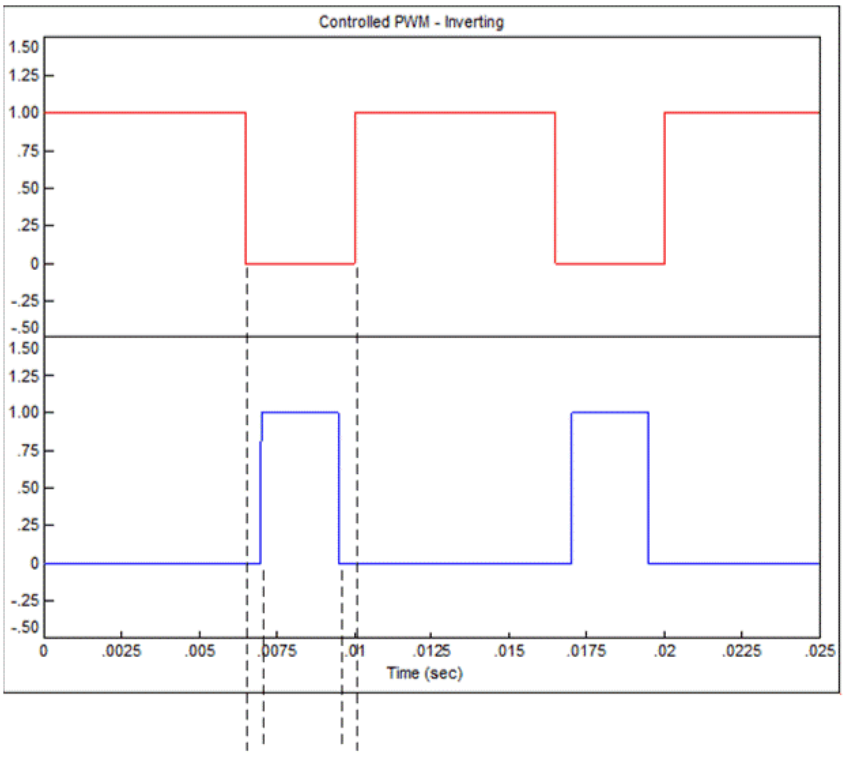
Function of the PWM2(B) output pin:

The following choices are available for the PWM output type:

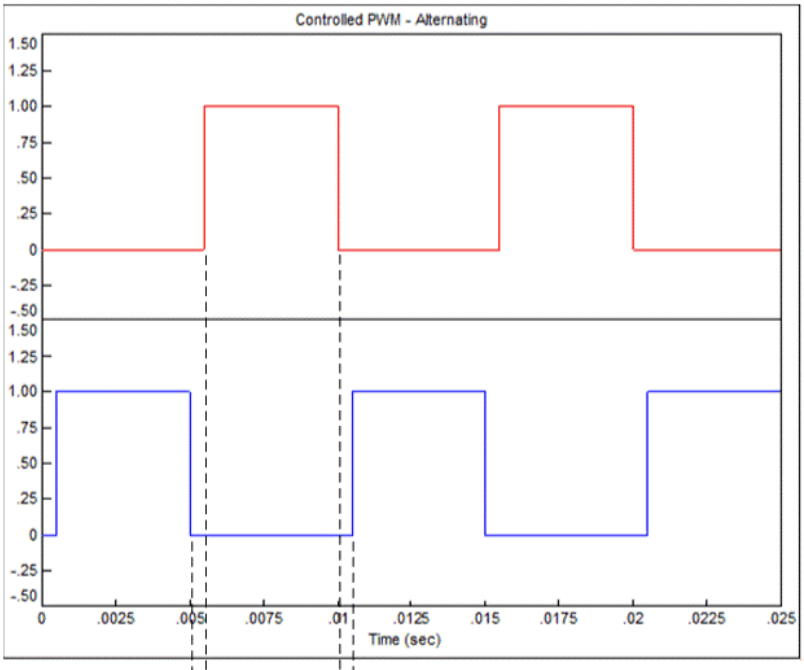
1. Inversion of first PWM
2. Alternating PWM

Deadtime (ns):

Enter the desired value of the dead-time in nanoseconds.
Note that how the dead-time is applied is determined by the PWM type selected as shown in the following figures:



Deadtime on rising and falling edge of PWMB



Deadtime on rising edge of PWMA and PWMB

Use discrete ramp generator:

Select this if a discrete stair-case type ramp generator is desired.

Clock rate:

Enter the clock rate for the discrete ramp generator.

Resolution:

Enter the resolution in bits for the discrete ramp generator.

Contents - Simulation



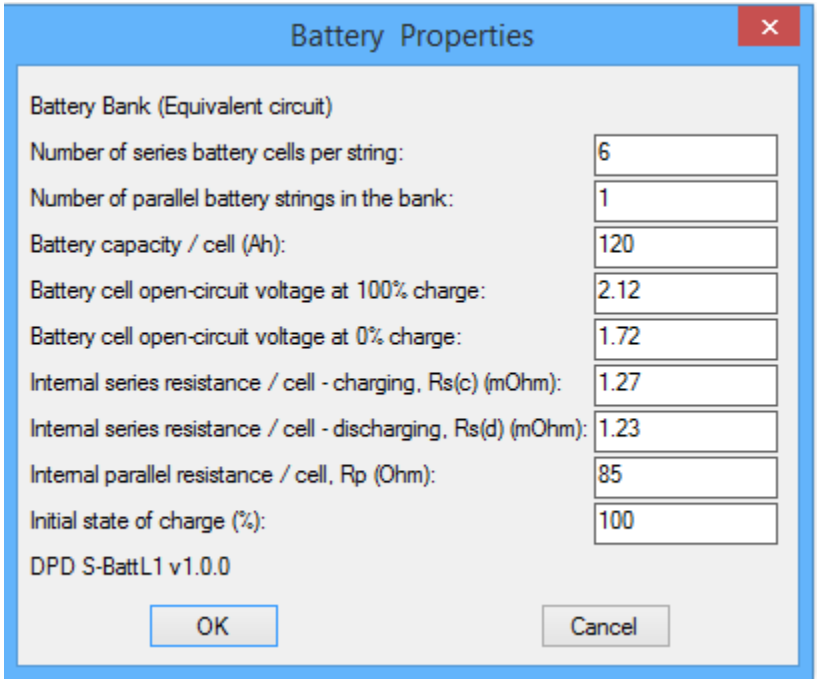
Battery – Dual Internal Resistance

Models a single battery cell or banks of series and parallel-connected cells of a generic type.

Input Pins:	**Vch**	Input voltage typically from a battery charger (V).
	Ibatt	Load current input of the battery (A).
Output Pins:	**Vbatt**	Battery voltage (V), when charging this will be the input Vch voltage.
	Ibatt	Battery current (A), charging or discharging.
	SOC (%)	State of charge of the battery expressed as a percentage.

Dialog properties:

The battery properties menu is shown in the following box which appears when right-clicking on the block



Number of series battery cells per string:

Enter the number of series cells in the battery string.

Number of parallel battery strings in the bank:

Enter the number of parallel battery strings in the battery bank.

Battery capacity / cell (Ah):

Enter the nominal capacity of the battery in Ampere-Hours.

Battery cell open-circuit voltage at 100% charge:

Enter the typical open-circuit voltage (V) of each cell when fully charged.

Battery cell open-circuit voltage at 0% charge:

Enter the typical open-circuit voltage (V) of each cell when completely discharged.

Internal series resistance in charge:

Enter the internal resistance of the battery in milli-ohms (when in the charging state).

Internal series resistance in discharge:

The internal resistance of the battery can be modelled with a different value when in the discharge state. Enter the value in milli-ohms.

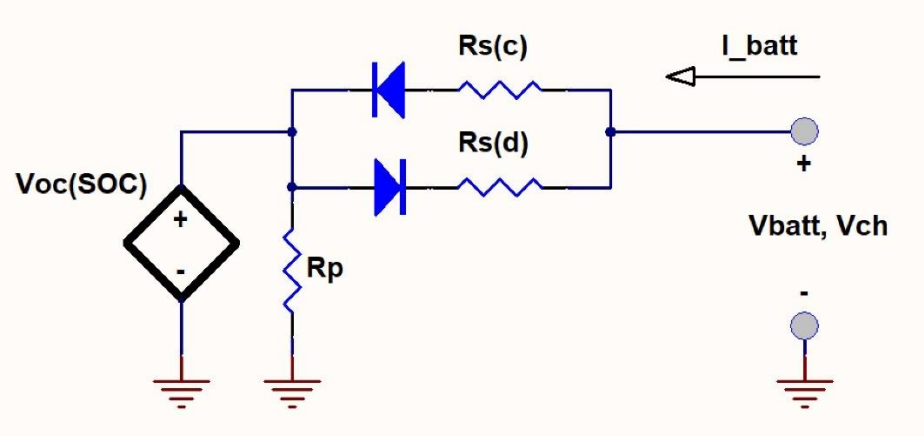
Internal parallel resistance of the battery:

Enter the internal parallel resistance of the battery in ohms. This is the self-discharge of the battery cell.

Initial state of charge:

Enter the initial state of charge (SOC) of the battery as a percentage.

Equivalent circuit modelled:

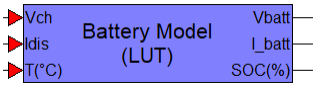


The battery can source or sink current and will source current until the battery is discharged to 0% of SOC.

If the input Vch voltage is > the battery open-circuit voltage (Voc) then the battery will be in charge, otherwise it will discharge into the connected load determined by the Ibatt input.

This model uses constant internal resistance but varies between the charge and discharge states. The self-discharge of the battery is also modelled. The open circuit voltage has a fixed characteristic based upon the values entered at 100% charge and at 0% charge (completely depleted of charge). If a different open-circuit voltage characteristic is required, then it is recommended to use one of the following battery models using look-up tables or a polynomial characteristic. Those models also allow the modelling of the internal resistance value as a function of the state of charge and are also optionally a function of the temperature.

Also, for battery dynamic modelling, it is recommended to use one of the following models rather than this battery model.

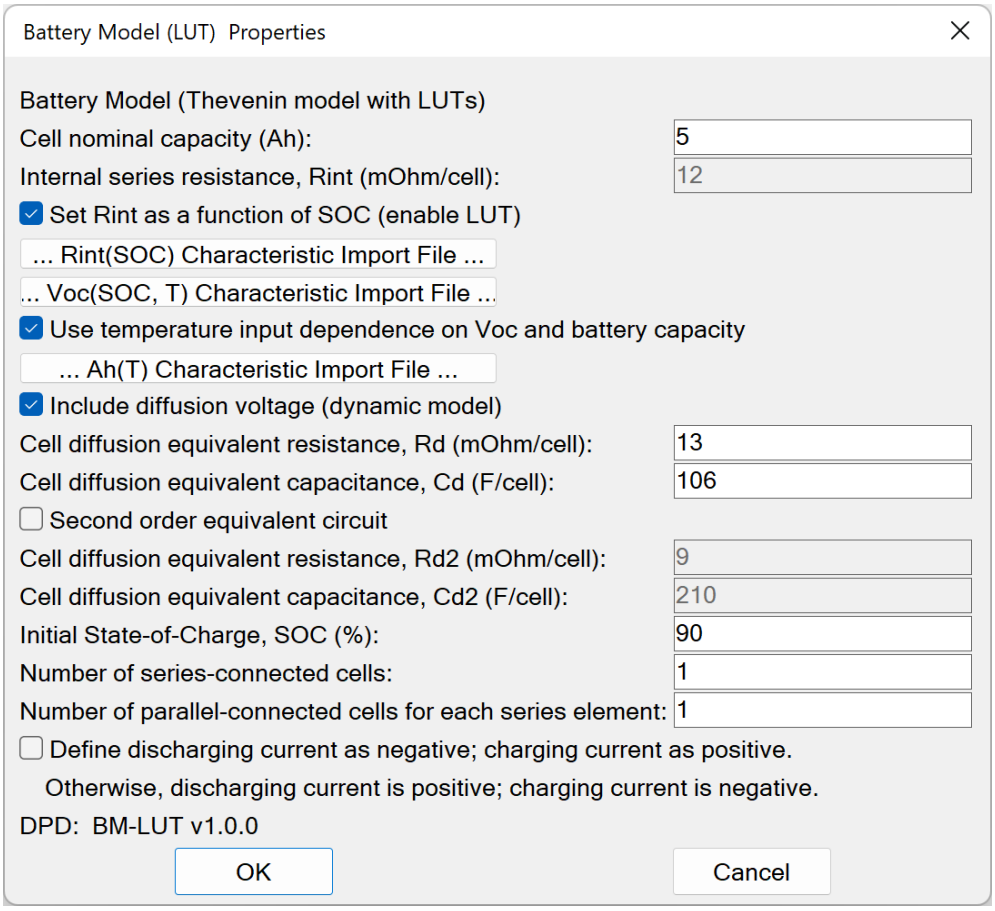


Battery - Thevenin Equivalent Circuit with LUT

Input Pins:	**Vch**	Input voltage (V) typically from a battery charger. This input voltage must be positive and the battery will charge or discharge depending upon the value at this input pin with respect to the internal open-circuit voltage.
	Idis	Load current (A) input of the battery. Depending upon the input polarity, the battery will charge or discharge. Either this pin or the Vch (voltage) input pin can be used to charge or discharge the battery, or a combination of both.
	T(°C)	Temperature input pin (°C).
Output Pins:	**Vbatt**	Battery terminal voltage (V), which is recalculated internally based upon the open-circuit voltage and the output impedance.
	I_batt	Battery current (A), charging or discharging.
	SOC (%)	State of charge of the battery expressed as a percentage.

Dialog properties:

The battery properties menu is shown in the following box which appears when right-clicking on the block



Cell nominal capacity (Ah/cell):

Enter the nominal capacity of each battery cell in Ampere-Hours.

Internal series resistance, Rint (mOhm / cell):

Enter the internal resistance of the battery in milli-ohms.

Set Rint as a function of SOC (enable LUT):

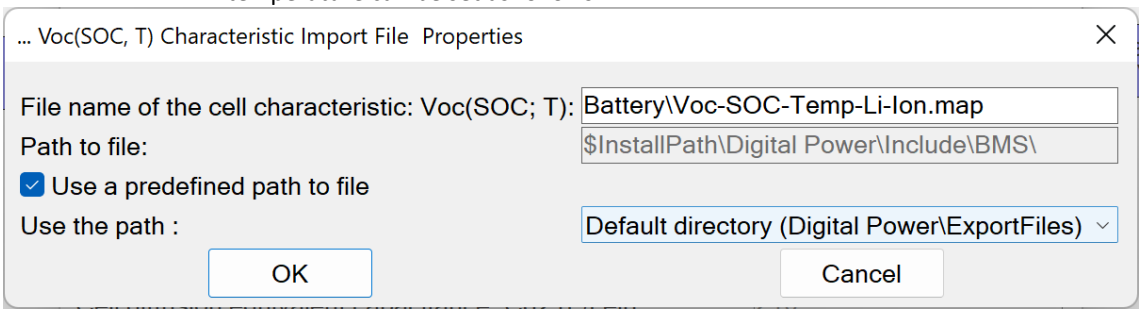
Select this if the internal resistance is to depend upon the state-of-charge.

Rint(SOC) characteristic import file:

If enabled, select the map for the internal resistance characteristic with respect to SOC.

Voc(SOC, T) characteristic import file:

The map file characteristic of the open-circuit voltage with respect to SOC and temperature can be set as follows:



Use temperature input dependence on Voc and battery capacity:

Select this to enable a map file selection with corrections for the Amp-hour rating of the battery with respect to temperature. This must also be selected to enable the temperature dependence on the open-circuit voltage characteristic, otherwise the open-circuit voltage characteristic will be set for 20°C.

Ah(T) characteristic import file:

Select the characteristic map file similarly to the open-circuit voltage map file.

Include diffusion voltage (dynamic model):

This selection will enable a first order equivalent circuit of the battery cell.

Cell diffusion equivalent resistance, Rd (mOhm / cell):

Enter the equivalent resistance of the first order cell diffusion voltage model in milli-ohms.

Cell diffusion equivalent capacitance, Cd (F / cell):

Enter the equivalent capacitance of the first order cell diffusion voltage model in Farads.

Second order equivalent circuit:

This selection will enable a second order equivalent circuit of the battery cell.

Cell diffusion equivalent resistance, Rd2 (mOhm / cell):

Enter the equivalent resistance of the second order cell diffusion voltage model in milli-ohms.

Cell diffusion equivalent capacitance, Cd2 (F / cell):

Enter the equivalent capacitance of the second order cell diffusion voltage model in Farads.

Initial state of charge:

Enter the initial state of charge (SOC) of the battery as a percentage.

Number of series-connected cells:

Enter the number of series-connected cells in the battery string.

Number of parallel-connected cells for each series element:

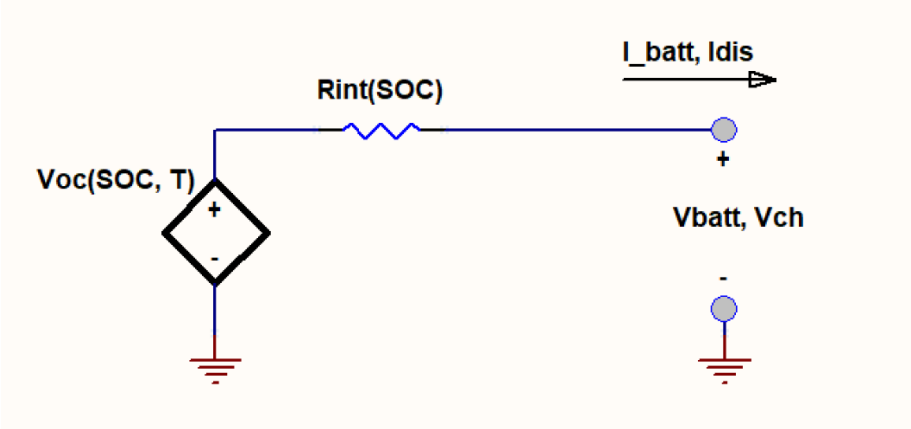
Enter the number of parallel-connected cells consisting of each series element.

Define discharging current as negative; charging current as positive:

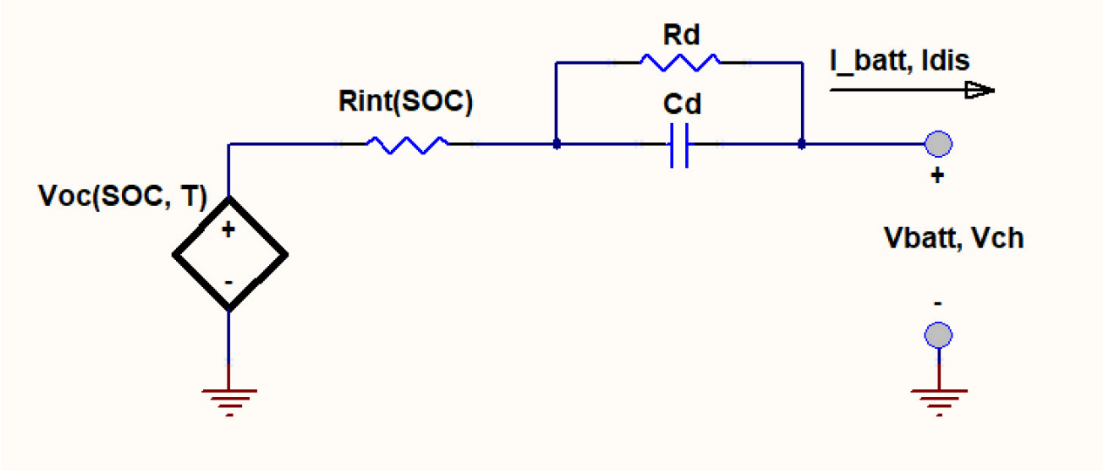
With this selection the polarity of the battery current can be exchanged (discharging current is negative, charging current is positive). As a default, the battery is considered a source and so the discharging current is positive while the charging current is negative.

If the effective SOC increases above 101% (beginning of over-charging), the block will turn red without a warning. If the effective SOC increases to 110% (output is limited at 105%), the simulation will be halted with a warning message. Likewise, if the SOC falls below 0%, the simulation will be halted with a warning message of a depleted battery.

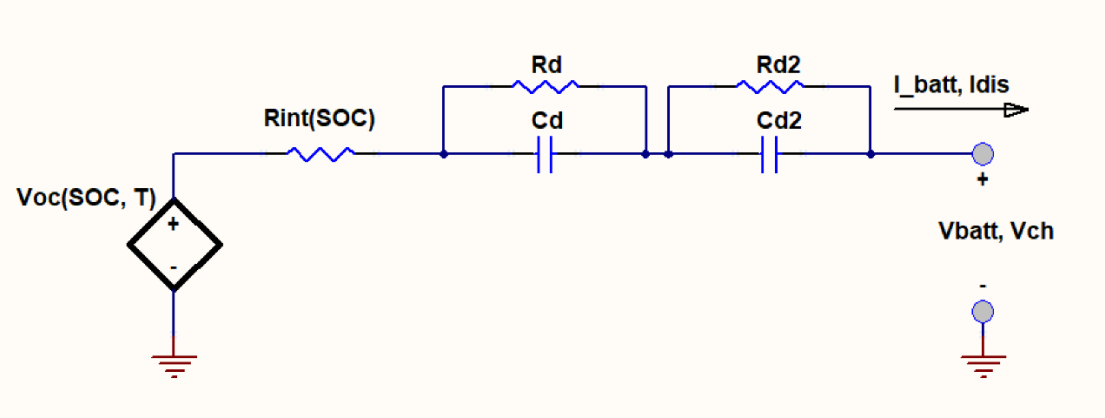
The equivalent circuits modelled by the various selections are shown in the following figures:



Zero order model



First order model

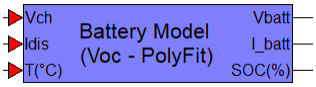


Second order model

The open-circuit voltage of the cell is mapped by the appropriate file. This is a 3-dimensional file which maps the open-circuit voltage with respect to the state-of-charge and the operating temperature of the battery.

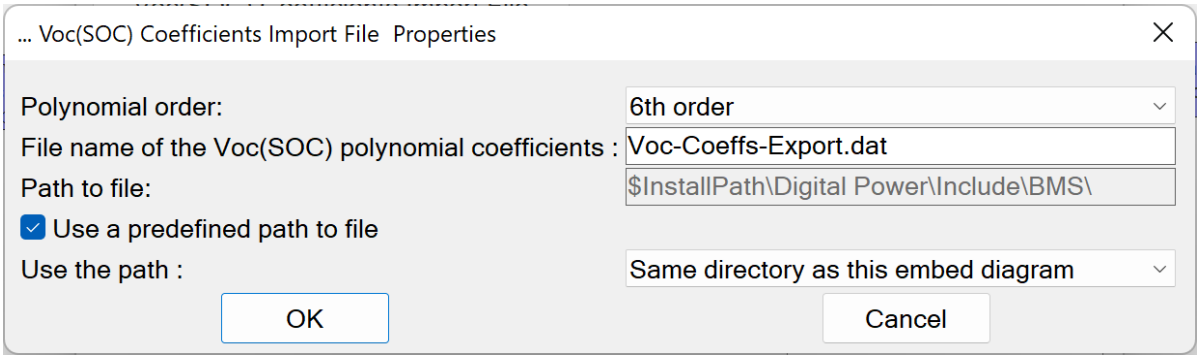
Series cells can be configured along with parallel -connected cells, however in this case the output equivalent circuit parameters are approximated for the series and parallel combinations.

The Thevenin equivalent circuit model is the most popular battery model found in the literature and further information of this model can be easily obtained.

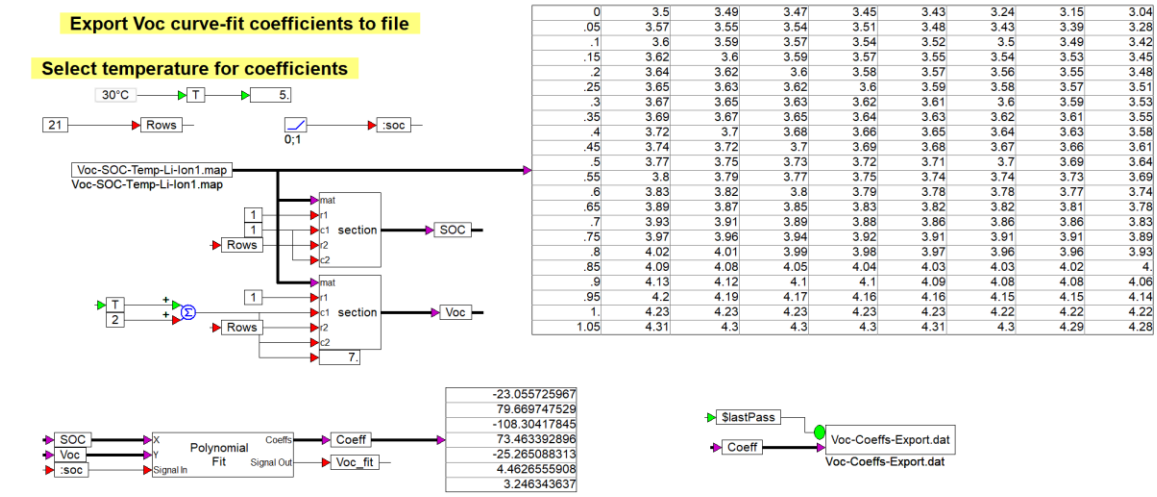


Battery - Thevenin Equivalent Circuit with PolyFit

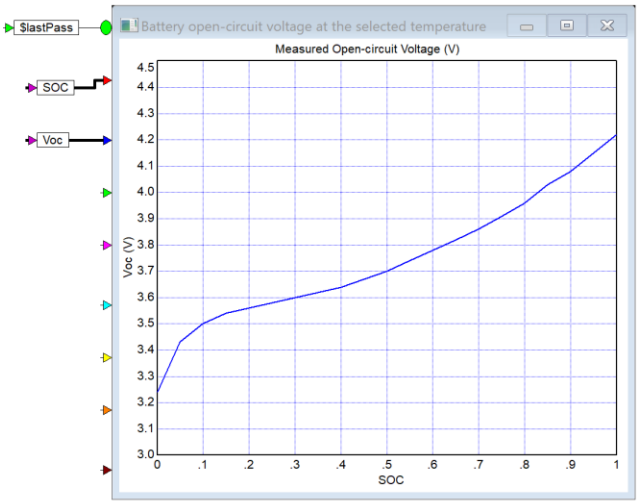
This block is identical to the battery model using look-up-tables except that in this case the open-circuit voltage, V_{oc}, is modelled using polynomial fitting equations. The polynomial can be selected from a 4^{th} to an 8^{th} order model and the coefficients imported as in the following dialog:

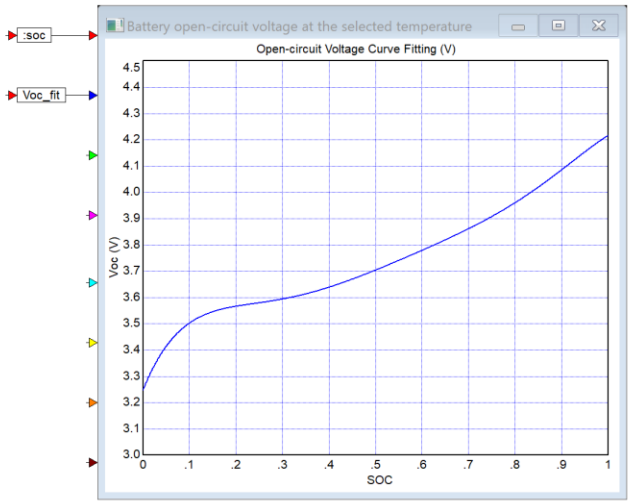


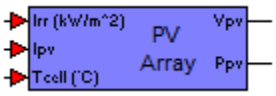
The curve-fitting and the subsequent determination of the necessary coefficients can be performed in Embed similar to the following example:



0	3.5	3.49	3.47	3.45	3.43	3.24	3.15	3.04
.05	3.57	3.55	3.54	3.51	3.48	3.43	3.39	3.28
.1	3.6	3.59	3.57	3.54	3.52	3.5	3.49	3.42
.15	3.62	3.6	3.59	3.57	3.55	3.54	3.53	3.45
.2	3.64	3.62	3.6	3.58	3.57	3.56	3.55	3.48
.25	3.65	3.63	3.62	3.6	3.59	3.58	3.57	3.51
.3	3.67	3.65	3.63	3.62	3.61	3.6	3.59	3.53
.35	3.69	3.67	3.65	3.64	3.63	3.62	3.61	3.55
.4	3.72	3.7	3.68	3.66	3.65	3.64	3.63	3.58
.45	3.74	3.72	3.7	3.69	3.68	3.67	3.66	3.61
.5	3.77	3.75	3.73	3.72	3.71	3.7	3.69	3.64
.55	3.8	3.79	3.77	3.75	3.74	3.74	3.73	3.69
.6	3.83	3.82	3.8	3.79	3.78	3.78	3.77	3.74
.65	3.89	3.87	3.85	3.83	3.82	3.82	3.81	3.78
.7	3.93	3.91	3.89	3.88	3.86	3.86	3.86	3.83
.75	3.97	3.96	3.94	3.92	3.91	3.91	3.91	3.89
.8	4.02	4.01	3.99	3.98	3.97	3.96	3.96	3.93
.85	4.09	4.08	4.05	4.04	4.03	4.03	4.02	4.
.9	4.13	4.12	4.1	4.1	4.09	4.08	4.08	4.06
.95	4.2	4.19	4.17	4.16	4.16	4.15	4.15	4.14
1.	4.23	4.23	4.23	4.23	4.23	4.22	4.22	4.22
1.05	4.31	4.3	4.3	4.3	4.31	4.3	4.29	4.28







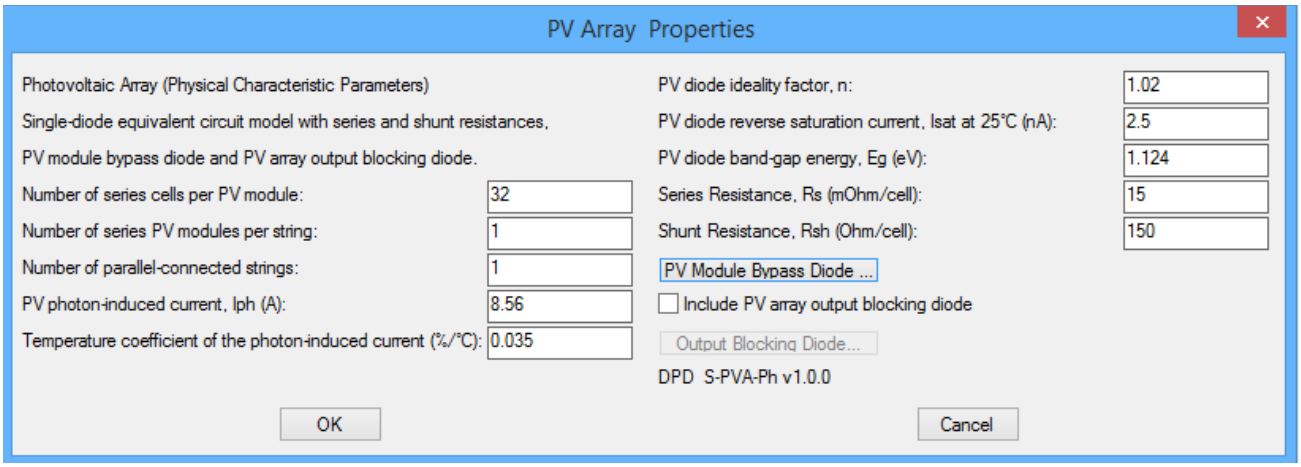
PV Array

A PV array can be configured by defining the physical PV cell characteristics and combining them into PV modules, strings and finally a PV array.

Input Pins:	**Irr**	Solar irradiation input in kW/m^2.
	Ipv	PV array current (A).
	Tcell	The cell temperature of the solar array in °C.
Output Pins:	**Vpv**	PV array output voltage (V).
	Ppv	PV array output power (W).

Dialog properties:

The PV Array properties menu is shown in the following box which appears when right-clicking on the block



Number of series cells per PV module:

Enter the number of series PV cells in each PV module.

Number of series PV modules per string:

Enter the number of series PV modules to form a PV string.

Number of parallel-connected strings:

Enter the number of parallel PV strings to form the PV array.

PV photon-induced current:

Enter the photo-voltaic photon induced current, Iph in nano-amps.

Temperature coefficient of the photon-induced current:

Enter the temperature coefficient of the photo-induced current.

PV diode ideality factor:

Enter the PV diode ideality factor.

PV diode reverse saturation current (nA):

Enter the reverse saturation current of the PV diode in nano-Amps.

PV diode band-gap energy (eV):

Enter the diode band-gap energy in electron-Volts.

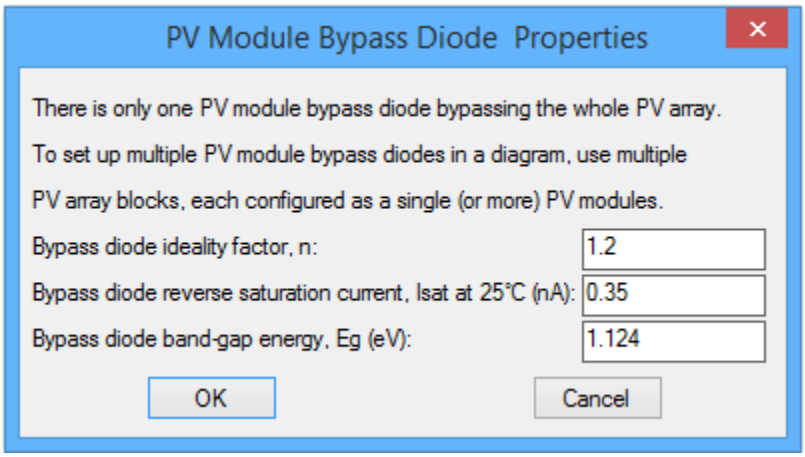
Series resistance, Rs:

Enter the series resistance of each PV cell according to the equivalent circuit in milli-ohms.

Shunt resistance, Rsh:

Enter the parallel resistance of each PV cell according to the equivalent circuit in ohms.

PV Module Bypass Diode:



Bypass diode ideality factor:

Enter the diode ideality factor.

Bypass diode reverse saturation current (nA):

Enter the reverse saturation current of the diode in nano-Amps.

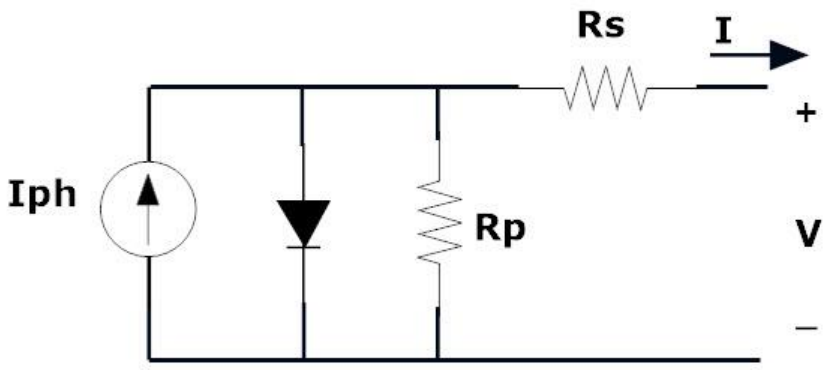
Bypass diode band-gap energy (eV):

Enter the diode band-gap energy in elevtron-Volts.

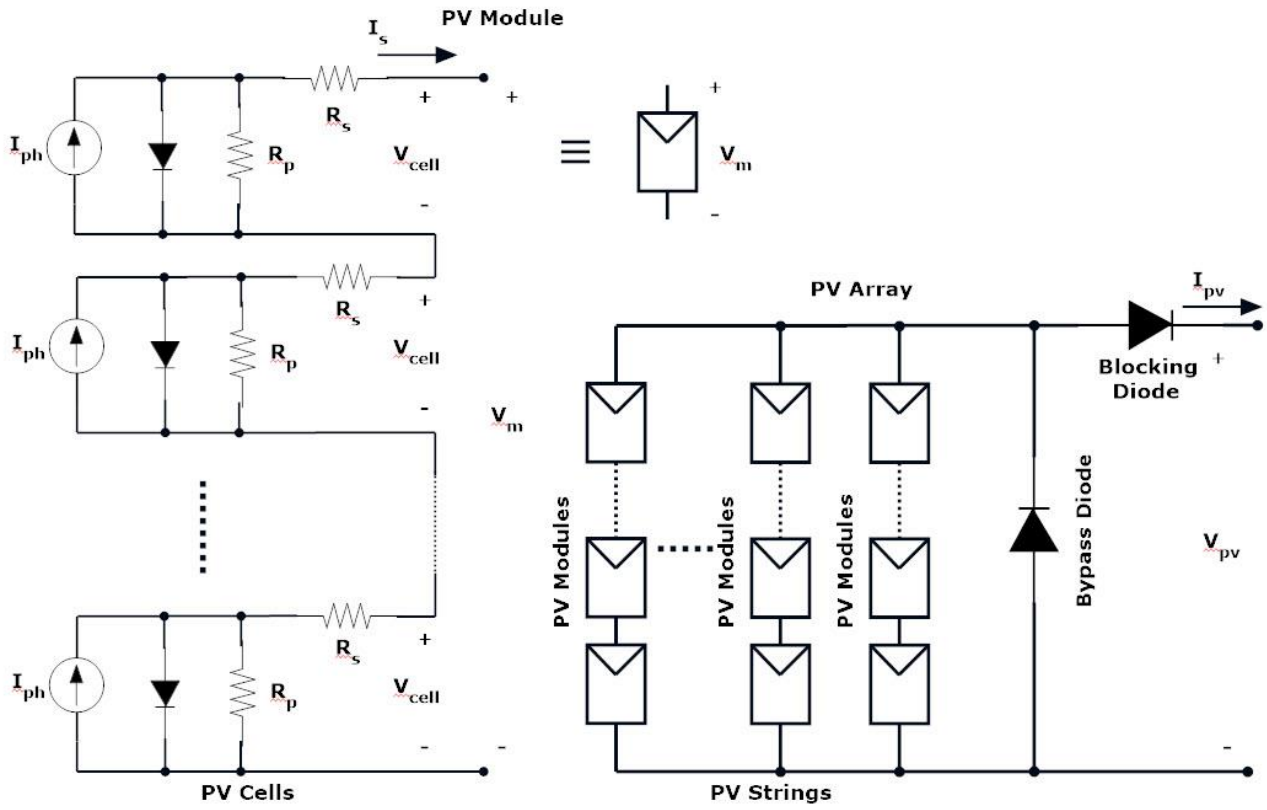
Include PV array output blocking diode:

Enabling the output blocking diode will configure a series diode in the PV array output. The configuration of this diode is similar to the bypass diode.

The model uses the 1-diode equivalent circuit model as follows:

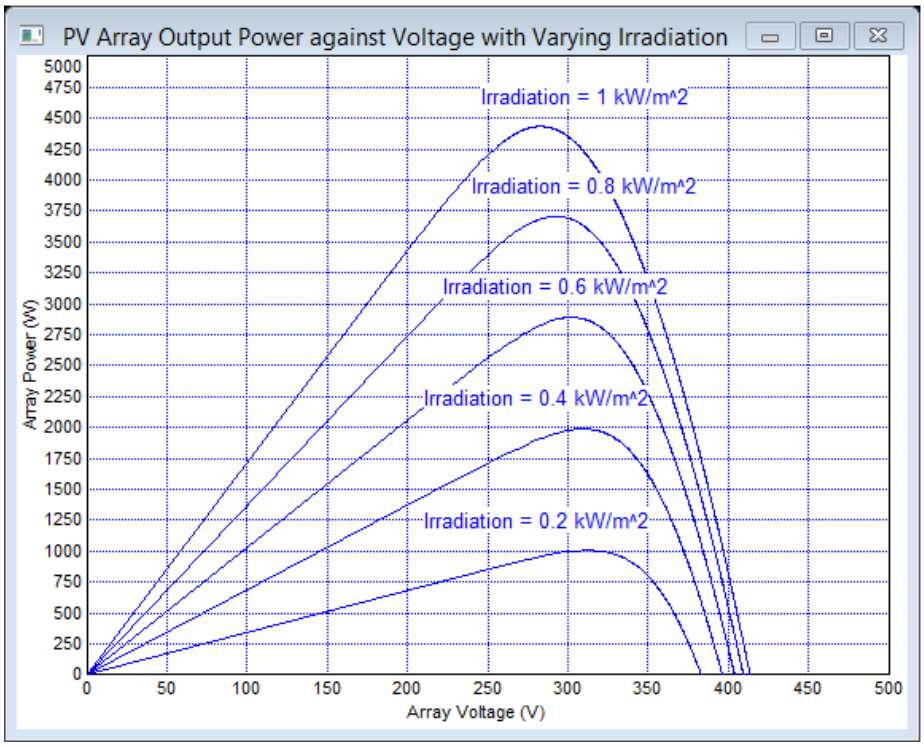


The PV array consists of series cells forming a PV module, series PV modules forming a PV string and parallel PV strings forming a PV array as in the following figure:

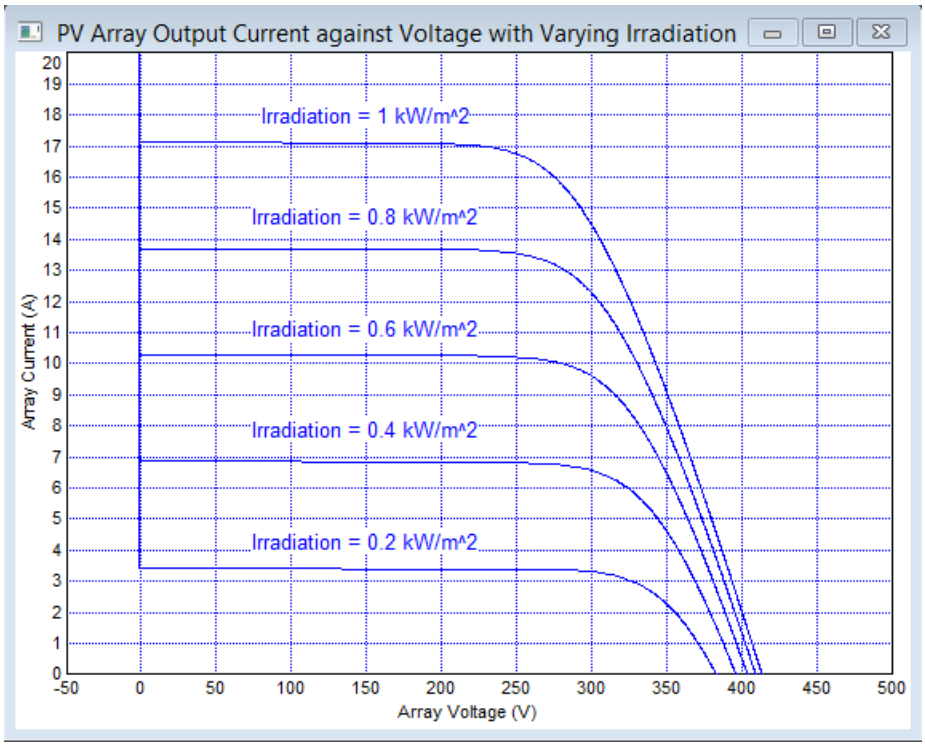


The PV array block can be used to configure a single PV cell, a single PV module, a PV string or an entire array. If the PV array block is used to configure a single PV module, many PV arrays blocks can also be connected together to form a PV array.

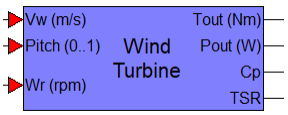
In this way, different solar irradiation and temperatures can be input into the individual PV modules and shading effects can be simulated.



PV array curves of output power against array voltage for varying solar irradiation levels.



PV array curves of array current against array voltage for varying solar irradiation levels.



Wind Turbine

The wind turbine can be configured by defining the physical PV cell characteristics and combining them into PV modules, strings and finally a PV array.

Input Pins:

Vw (m/s) The wind velocity in $m.s^{-1}$.

Pitch (0..1) Pitch controller input (0..1) in degrees divided by 90 and limited from 1 down to 0 where a value of 1 corresponds to 90° (against the wind) and the maximum output power would be set by a value of 0 at this pin. This input could also be used as a yaw control input in the case of a yaw control mechanism.

Wr (rpm) The rotor angular velocity in revolutions per minute.

Output Pins:

Tout Output torque (Nm).

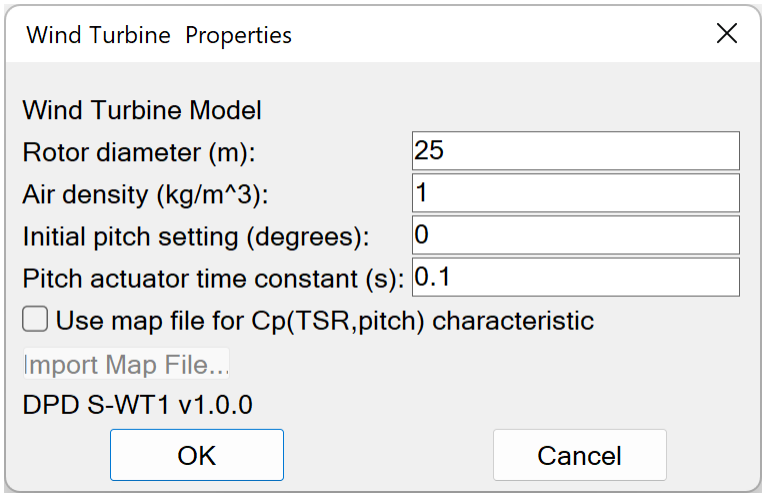
Pout Wind turbine output power (W).

Cp Power coefficient of the wind turbine

TSR Tip speed ratio output (λ).

Dialog properties:

The Wind Turbine properties menu is shown in the following box which appears when right-clicking on the block



Rotor diameter (m):

Enter the diameter of the turbine in meters.

Air density (kg/m^3):

Enter the air density in kg / m^3.

Initial pitch setting (degrees):

Enter the initial setting of the pitch control in degrees (0..90).

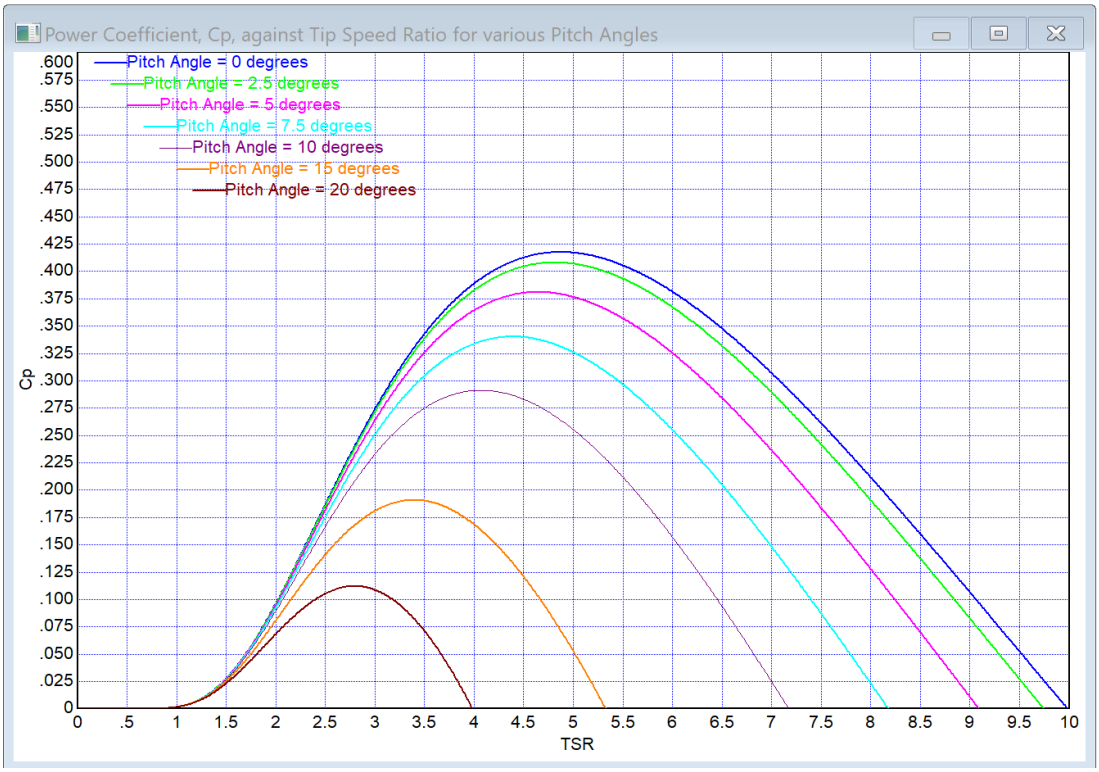
Pitch actuator time constant (s):

Enter the time constant of the mechanical pitch actuator in seconds.

Use map file for Cp(TSR, pitch) characteristic:

If checked, a 2-dimensional map file can be defined for the power coefficient characteristic to be used in the model as a function of tip speed ratio and pitch angle.

Typical power coefficient against tip speed ratio curves for various pitch angles are given below using the internal default characteristic:





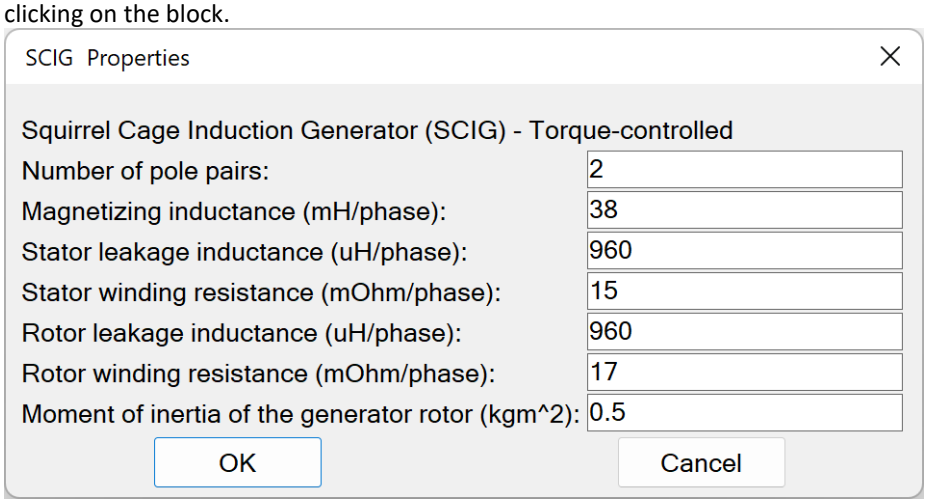
Squirrel Cage Induction Generator (SCIG)

The squirrel cage induction generator (SCIG) model is based on the two-phase equivalent circuit of the induction motor. This model can be used in the synchronous d-q reference frame or the rotating alpha-beta frame. This block models the generator using a Torque input.

Input pins:	**Tm (Nm)**	The mechanical input torque to the generator in Nm.
	Wm (rpm)	The mechanical angular velocity of the generator rotor in revolutions per minute.
	v[L12,L23,L31]	The stator (output) voltage input in volts.
Output pin:	**iS[L1,L2,L3]**	The stator (generator output) three-phase currents in amperes.
	Te (Nm)	The electromagnetic torque output in Nm.
	Wm (rpm)	The rotor angular velocity in revolutions per minute.

Dialog properties:

The SCIG block properties menu is shown in figure 5.69 which appears when right-clicking on the block.



Number of pole pairs:

The number of generator pole pairs.

Magnetising inductance:

Enter the magnetizing inductance of the equivalent model in milli-Henry per phase.

Stator leakage inductance:

Enter the stator leakage inductance in micro-Henry.

Stator winding resistance:

Enter the winding resistance of the stator in milli-Ohms.

Rotor leakage inductance:

Enter the rotor leakage inductance in micro-Henry.

Rotor winding resistance:

Enter the winding resistance of the rotor in milli-Ohms.

Moment of inertia of the generator rotor:

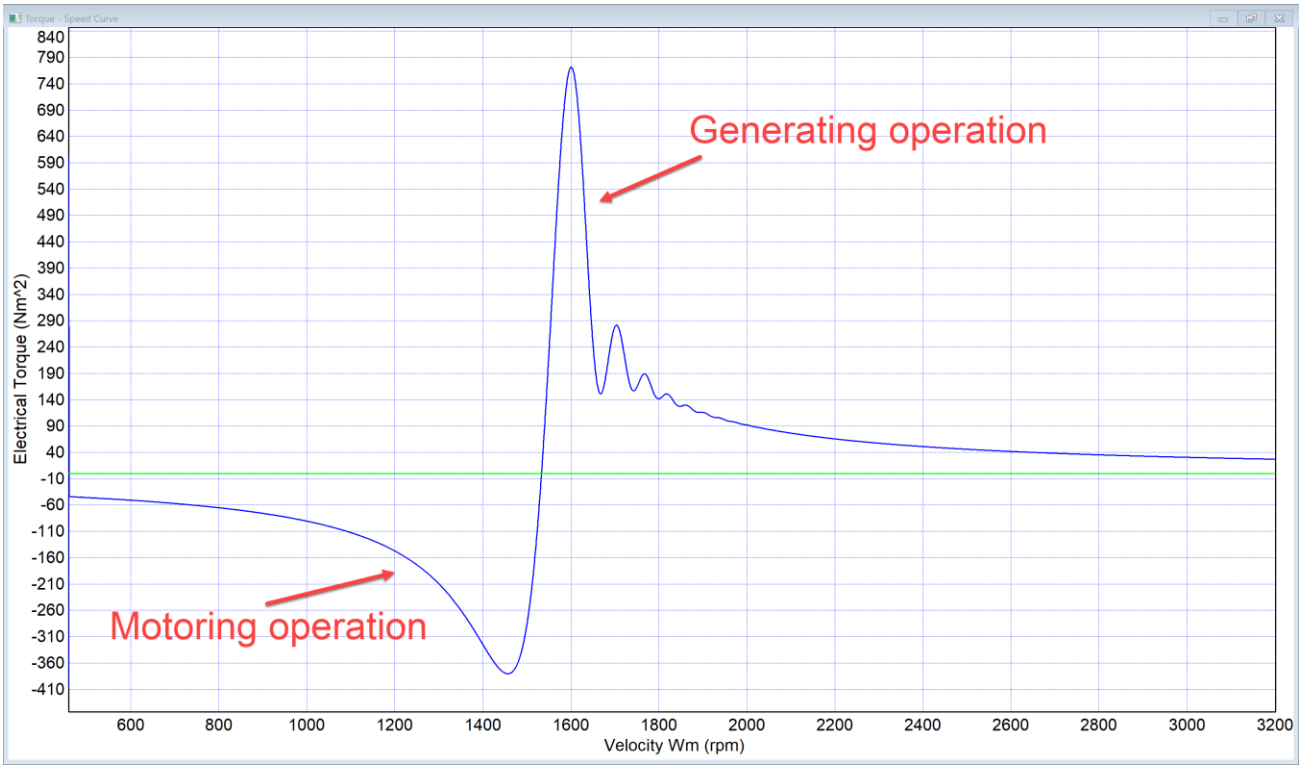
Enter the constant of moment of inertia of the generator rotor in kg.m.s^2.

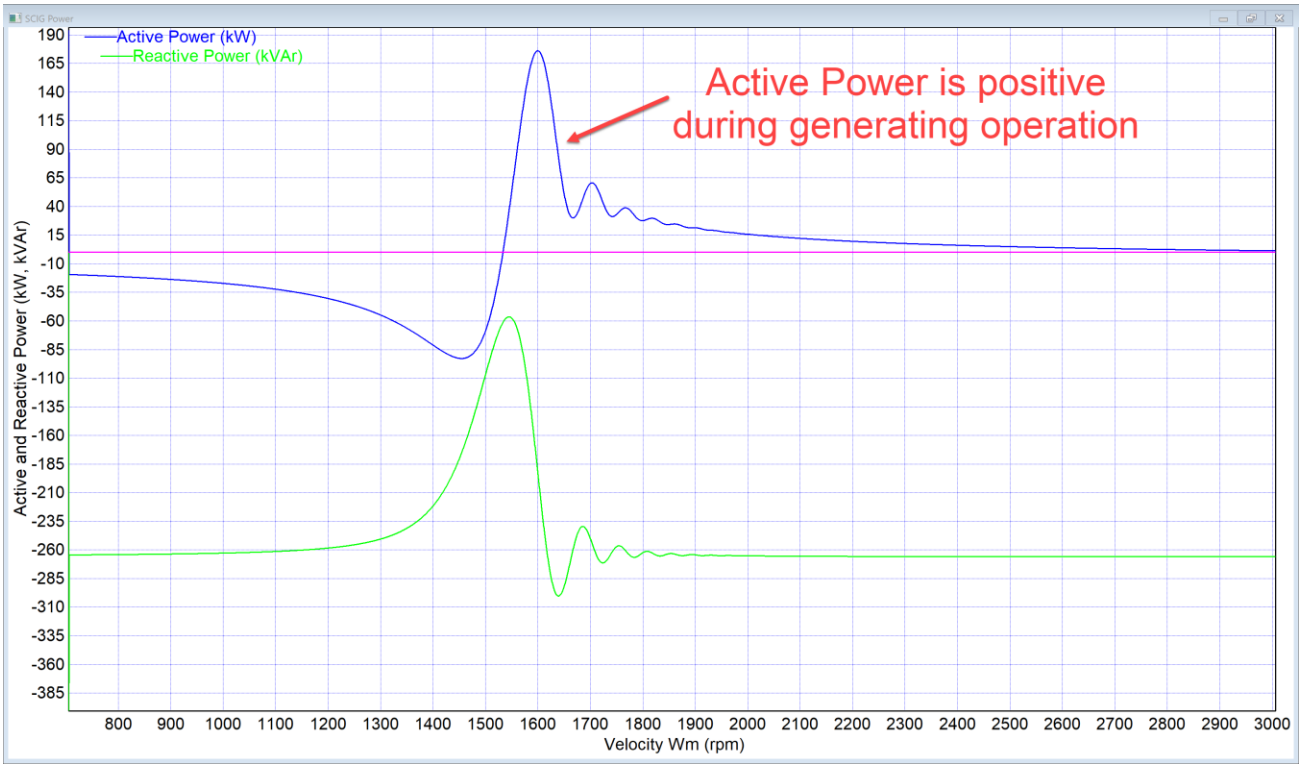


SCIG (Velocity input)

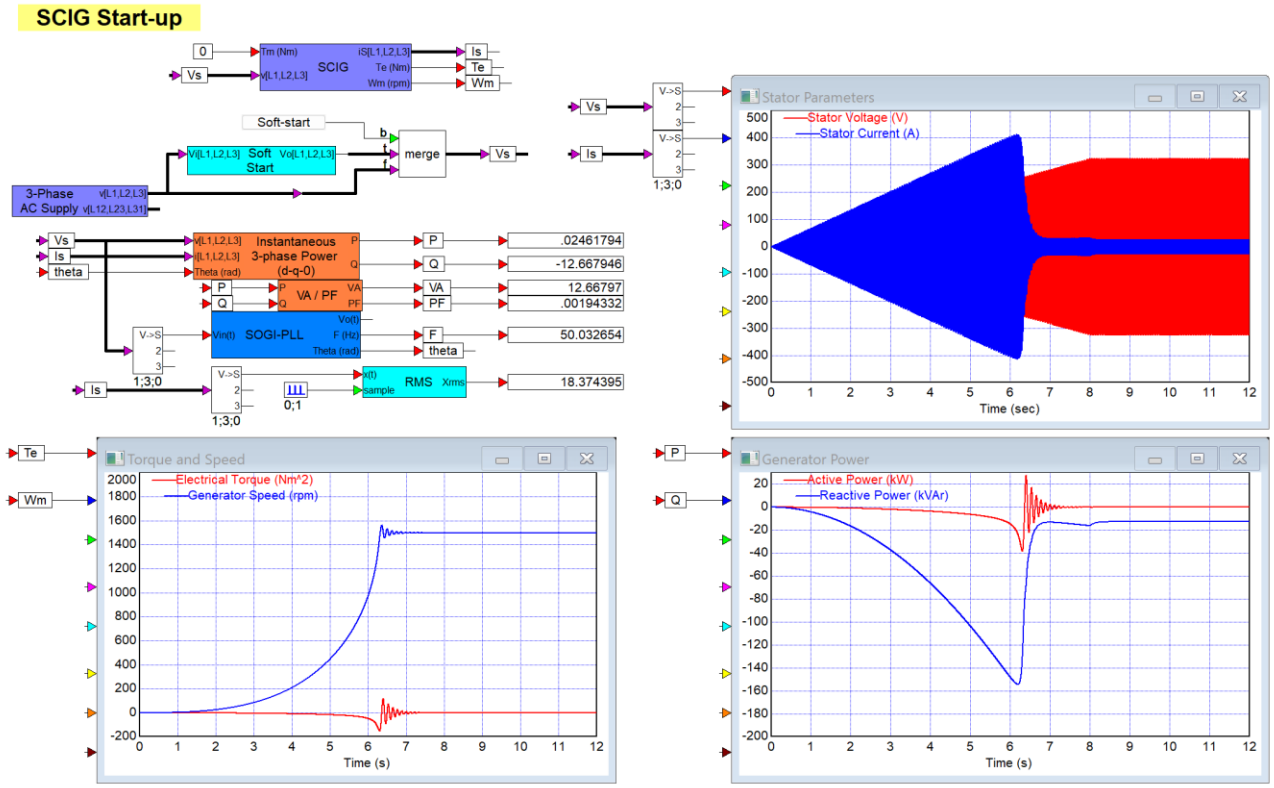
This block is identical to the previous SCIG model (Torque input) except that it has a mechanical velocity input (there is no mechanical torque output) in this case and is used more for generating torque-velocity curves and generator parameters.

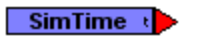
In simulations, generally the torque input model would be used.Note that the SCIG model is defined so that in generating mode, the power and torque are positive as shown in the following:


Torque - Speed Curve
Generating operation
Motoring operation
Electrical Torque (Nm^2)
Velocity Wm (rpm)


SCIG Power
Active Power (kW)
Reactive Power (kVAr)
Active Power is positive
during generating operation
Active and Reactive Power (kW, kVAr)
Velocity Wm (rpm)

The SCIG model during start-up is shown in the following.





Simulation time

This block outputs the current simulation time.

Output Pins: **t** The current simulation time in seconds.

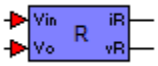
Contents - Simulation

Components

The components sub-section within the simulation section of the Digital Power Designer provides many blocks which will be expanded upon, in order to perform basic circuit simulations and form custom converter configurations used in digital power applications.

Some other components, such as transformers can be used completely independently for transformer design and simulation verification with transformers.

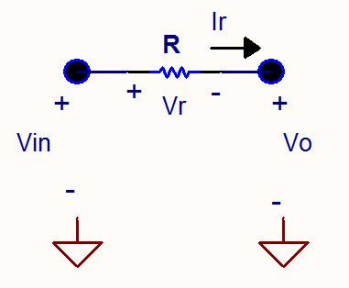
Passive Components



Resistor (series)

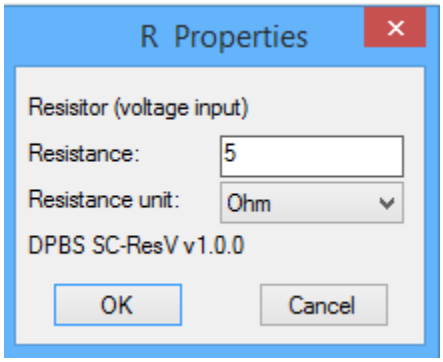
Input Pins:	**Vin**	Input voltage (V).
	Vo	Output voltage (V)
Output Pins:	**iR**	Current through the resistor (A)
	vR	Voltage across the resistor (V)

Circuit schematic:



Dialog properties:

The series resistor block properties menu is shown in the following box which appears when right-clicking on the block.

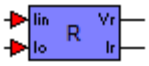


Resistance:

Enter the value of the resistor.

Resistance unit:

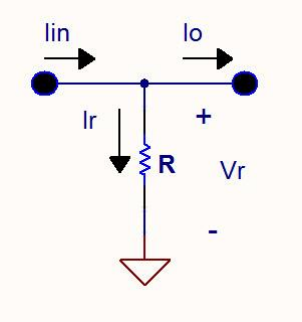
Select the units of the resistance here.



Resistor (shunt)

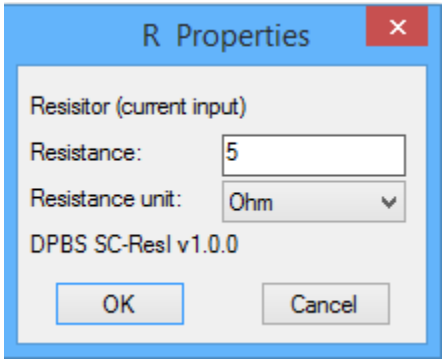
Input Pins:	**Iin**	Input current to the resistor (A).
	Io	Output current (A)
Output Pins:	**Vr**	Voltage across the resistor (to ground, V)
	Ir	The current through the resistor (A).

Circuit schematic:



Dialog properties:

The shunt resistor block properties menu is shown in the following box which appears when right-clicking on the block.

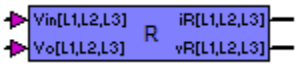


Resistance:

Enter the value of the resistor.

Resistance unit:

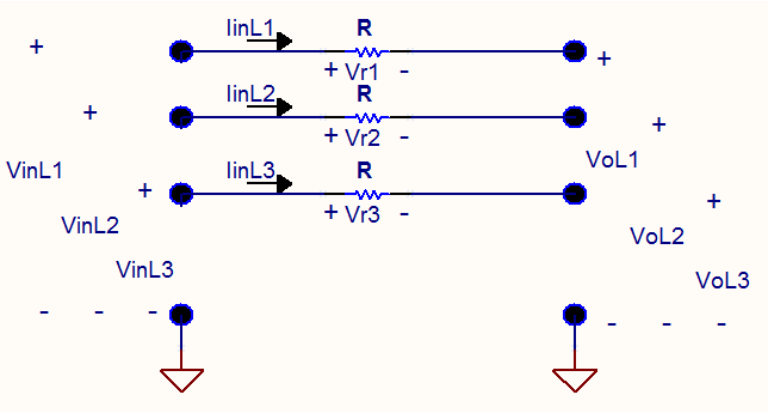
Select the units of the resistance here.



Resistor (3-phase, series)

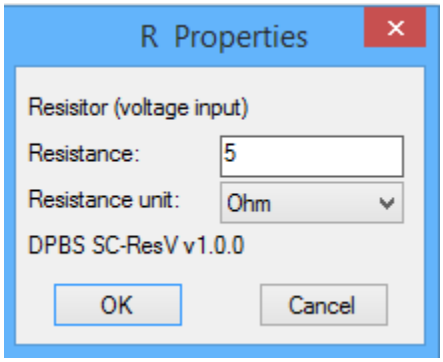
Input Pins:	**Vin[L1,L2,L3]**	Input 3-phase voltage (V).
	Vo[L1,L2,L3]	Output 3-phase voltage (V)
Output Pins:	**iR[L1,L2,L3]**	3-phase Current through the resistor (A)
	vR[L1,L2,L3]	3-phase Voltage across the resistor (V)

Circuit schematic:



Dialog properties:

The 3-phase series resistor block properties menu is shown in the following box which appears when right-clicking on the block.



Resistance:

Enter the value of the resistor.

Resistance unit:

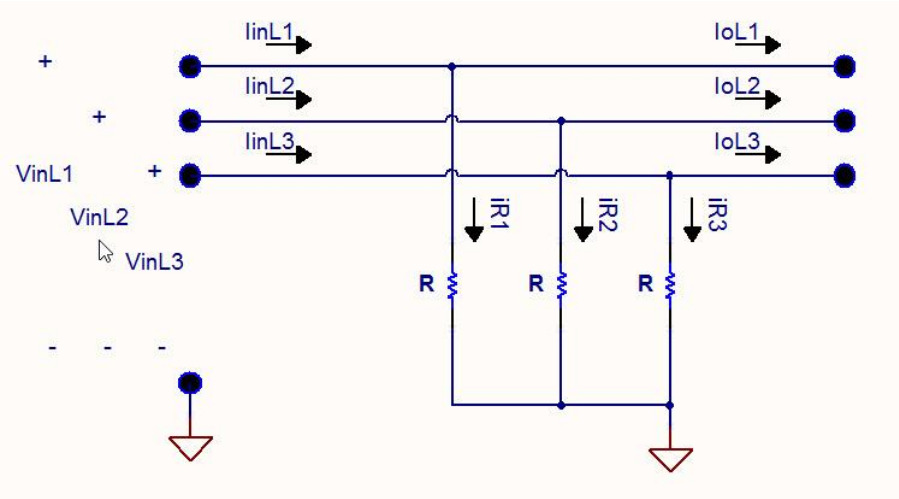
Select the units of the resistance here.



Resistor (3-phase, Y-connected, voltage input)

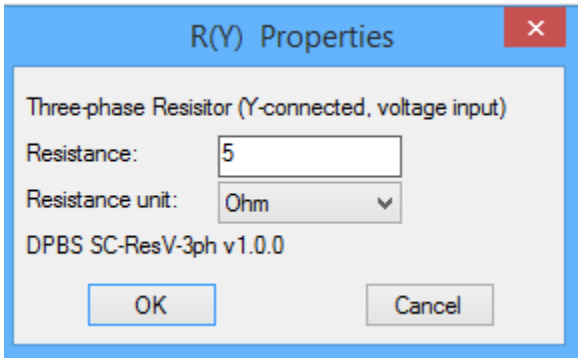
Input Pins:	**Vin[L1,L2,L3]**	Input three-phase voltage (V).
	vY	Star-point voltage (V)
Output Pins:	**iR[L1,L2,L3]**	Lines currents in the resistors (A)
	vR[L1,L2,L3]	Voltage across the 3-phase resistors (V)

Circuit schematic:



Dialog properties:

The three-phase resistive block properties menu is shown in the following box which appears when right-clicking on the block.



Resistance:

Enter the value of the resistor.

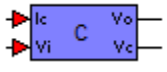
Resistance unit:

Select the units of the resistance here.



Resistor (3-phase, Y-connected, current input)

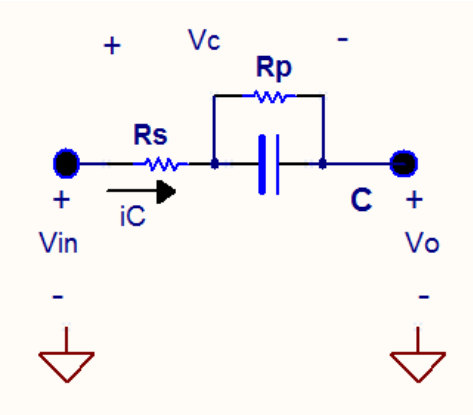
This block is similar to the voltage input 3-phase Y-connected resistor except that the inputs are the current into the three-phase resistance network.



Capacitor (series)

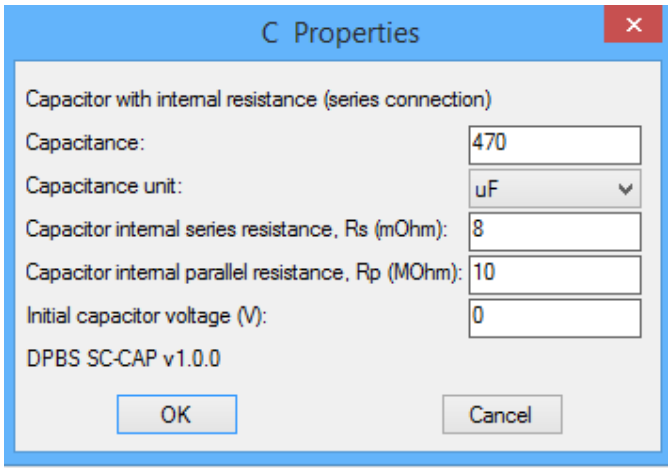
Input Pins:	**Ic**	Current through the capacitor (A)
	Vi	Input voltage (V).
Output Pins:	**Vo**	Output voltage (V)
	Vc	Voltage across the capacitor (V).

Circuit schematic:



Dialog properties:

The capacitor block properties menu is shown in the following box which appears when right-clicking on the block.



Capacitance:

Enter the value of the capacitor.

Capacitance unit:

Select the units of the capacitance value here.

Capacitor internal series resistance:

Enter the series resistance or ESR of the capacitor in milli-ohms.

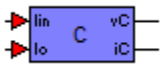
Capacitor internal parallel resistance:

Enter the equivalent parallel resistance (self-discharge) of the capacitor in Mega-ohms.

Initial capacitor voltage:

Enter the initial voltage on the capacitor in volts.

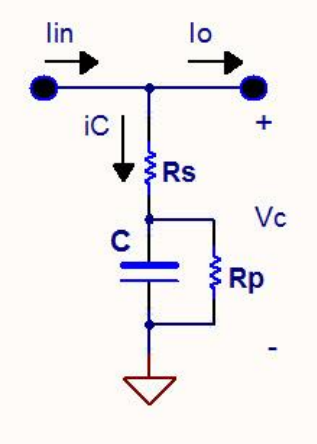
[Contents - Simulation]



Capacitor (shunt-connected)

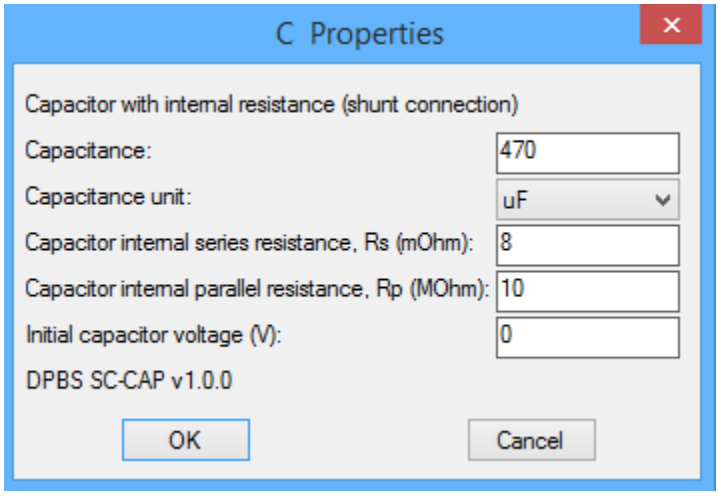
Input Pins:	**Iin**	The input current from a source connected to the capacitor (A).
	Io	The output current to loading on the capacitor (A)
Output Pins:	**vC**	The voltage across the capacitor (V)
	iC	The current through the capacitor (A)

Circuit schematic:



Dialog properties:

The shunt capacitor block properties menu is shown in the following box which appears when right-clicking on the block.



Capacitance:

Enter the value of the capacitor.

Capacitance unit:

Select the units of the capacitance value here.

Capacitor internal series resistance:

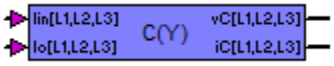
Enter the series resistance or ESR of the capacitor in milli-ohms.

Capacitor internal parallel resistance:

Enter the equivalent parallel resistance (self-discharge) of the capacitor in Mega-ohms.

Initial capacitor voltage:

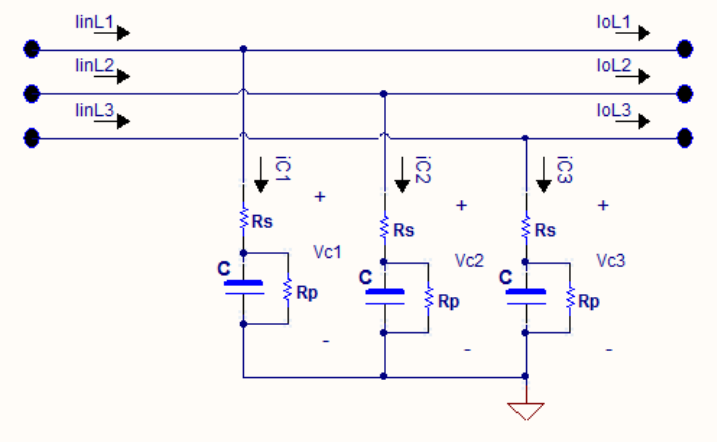
Enter the initial voltage on the capacitor in volts.



Capacitor (3-phase, Y-connected)

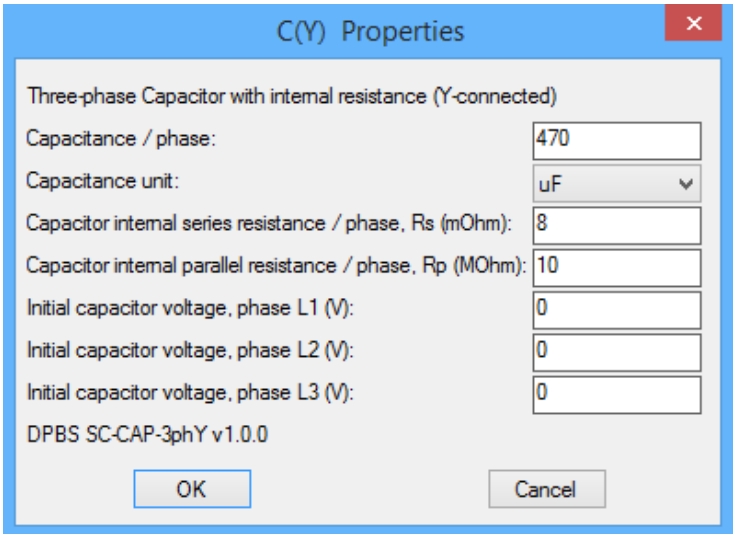
Input Pins:	**Iin[L1,L2,L3]**	3-phase Input current (A).
	Io[L1,L2,L3]	3-phase Output current input (A)
Output Pins:	**vC[L1,L2,L3]**	3-phase Voltage across the capacitor (V)
	iC[L1,L2,L3]	3-phase Current through the capacitor (A)

Circuit schematic:



Dialog properties:

The three-phase capacitor block properties menu is shown in the following box which appears when right-clicking on the block.



Capacitance:

Enter the value of the capacitor.

Capacitance unit:

Select the units of the capacitance value here.

Capacitor internal series resistance:

Enter the series resistance or ESR of the capacitor in milli-ohms.

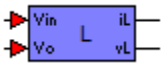
Capacitor internal parallel resistance:

Enter the equivalent parallel resistance (self-discharge) of the capacitor in Mega-ohms.

Initial capacitor voltage:

Enter the initial voltage on the capacitor in volts.

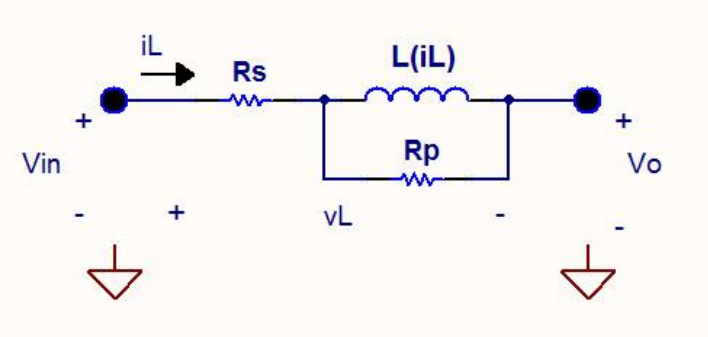
Contents - Simulation



Inductor (series)

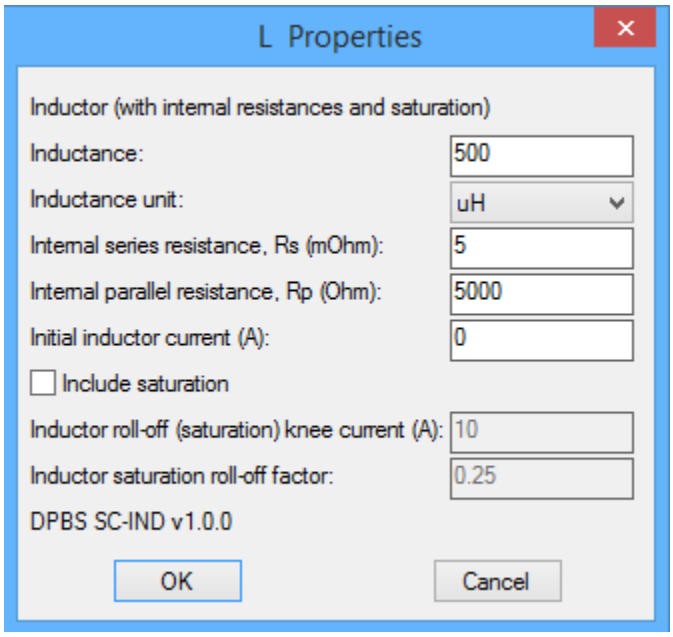
Input Pins:	**Vin**	Input voltage (V).
	Vo	Output voltage (V)
Output Pins:	**iR**	Current through the resistor (A)
	vR	Voltage across the resistor (V)

Circuit schematic:



Dialog properties:

The inductor block properties menu is shown in the following box which appears when right-clicking on the block.



Inductance:

Enter the value of the inductor.

Inductance unit:

Select the units of the inductance here.

Internal series resistance:

Enter the value of the internal series resistance in milli-ohms.

Internal parallel resistance:

The parallel resistance can model inductor core-loss. Enter a value in ohms.

Initial inductor current:

Enter the initial inductor current for each phase.

Include saturation:

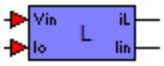
Select the units of the resistance here.

Inductor roll-off (saturation) knee current:

Enter the value of inductor current where the bend in the saturation curve characteristic begins.

Inductor saturation roll-off factor:

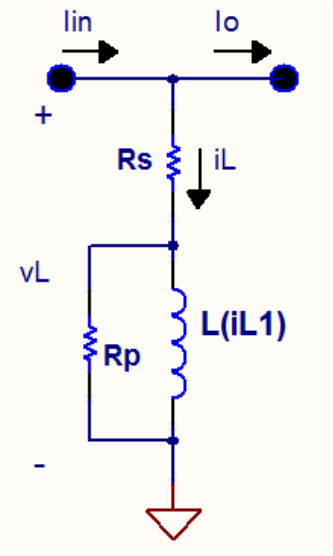
The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero.



Inductor (shunt-connected)

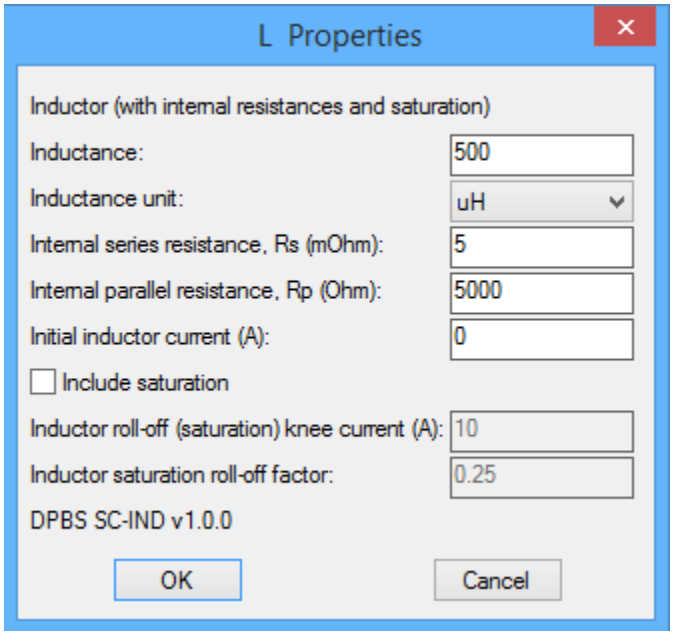
Input Pins:	**Vin**	Input voltage (V) across the inductor.
	Io	Output current input (A)
Output Pins:	**iL**	Current through the inductor (A).
	Iin	Input current (A).

Circuit schematic:



Dialog properties:

The shunt connected inductor block properties menu is shown in the following box which appears when right-clicking on the block.



Inductance:

Enter the value of the inductor.

Inductance unit:

Select the units of the inductance here.

Internal series resistance:

Enter the value of the internal series resistance in milli-ohms.

Internal parallel resistance:

The parallel resistance can model inductor core-loss. Enter a value in ohms.

Initial inductor current:

Enter the initial inductor current for each phase.

Include saturation:

Select the units of the resistance here.

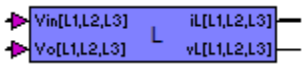
Inductor roll-off (saturation) knee current:

Enter the value of inductor current where the bend in the saturation curve characteristic begins.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero.

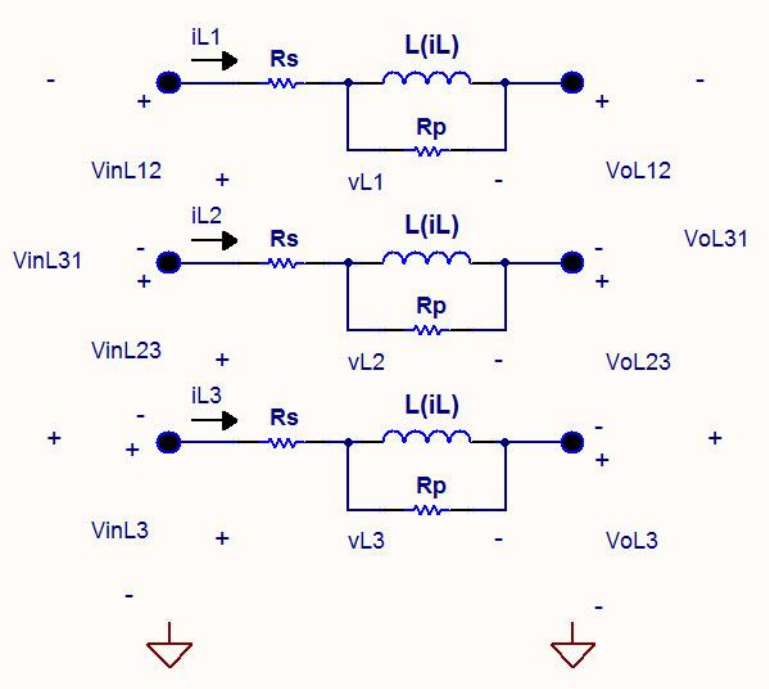
Contents - Simulation



Inductor (3-phase, series)

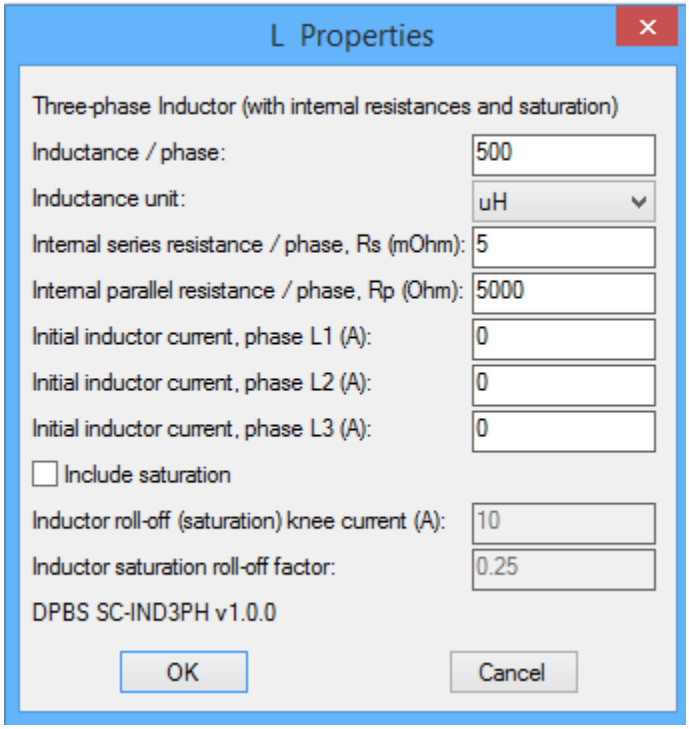
Input Pins:	**Vin[L1,L2,L3]**	Input line-neutral voltage (V).
	Vo[L1,L2,L3]	Output line-neutral voltage (V)
Output Pins:	**iL[L1,L2,L3]**	Current through the 3-phase inductors (A)
	vL[L1,L2,L3]	Voltage across the 3-phase inductor (V)

Circuit schematic:



Dialog properties:

The three-phase inductor block properties menu is shown in the following box which appears when right-clicking on the block.



Inductance:

Enter the value of the inductor.

Inductance unit:

Select the units of the inductance here.

Internal series resistance:

Enter the value of the internal series resistance in milli-ohms.

Internal parallel resistance:

The parallel resistance can model inductor core-loss. Enter a value in ohms.

Initial inductor current:

Enter the initial inductor current for each phase.

Include saturation:

Select the units of the resistance here.

Inductor roll-off (saturation) knee current:

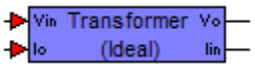
Enter the value of inductor current where the bend in the saturation curve characteristic begins.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero.

Contents - Simulation

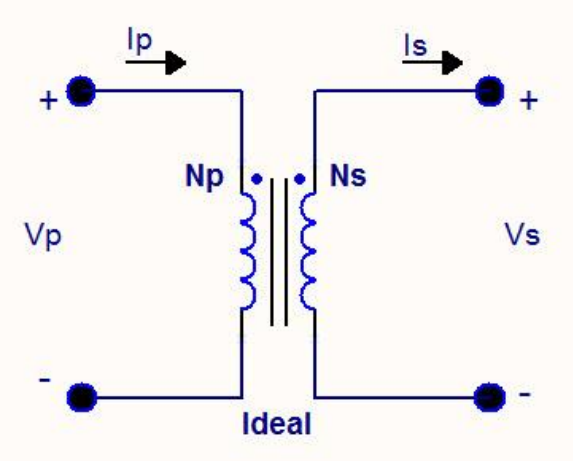
Transformers



Single-phase transformer (ideal)

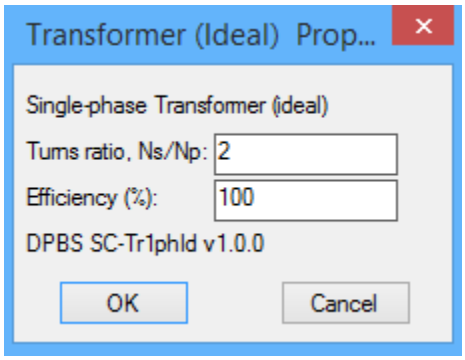
Input Pins:	**Vin**	Primary Input voltage (V).
	Io	Secondary Output current (A).
Output Pins:	**Vo**	Secondary Output voltage (V)
	Iin	Primary input current (A).

Circuit schematic:



Dialog properties:

The ideal transformer block properties menu is shown in the following box which appears when right-clicking on the block.

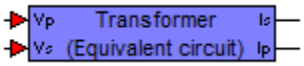


Turns ratio:

Enter the turns ratio of the transformer.

Efficiency:

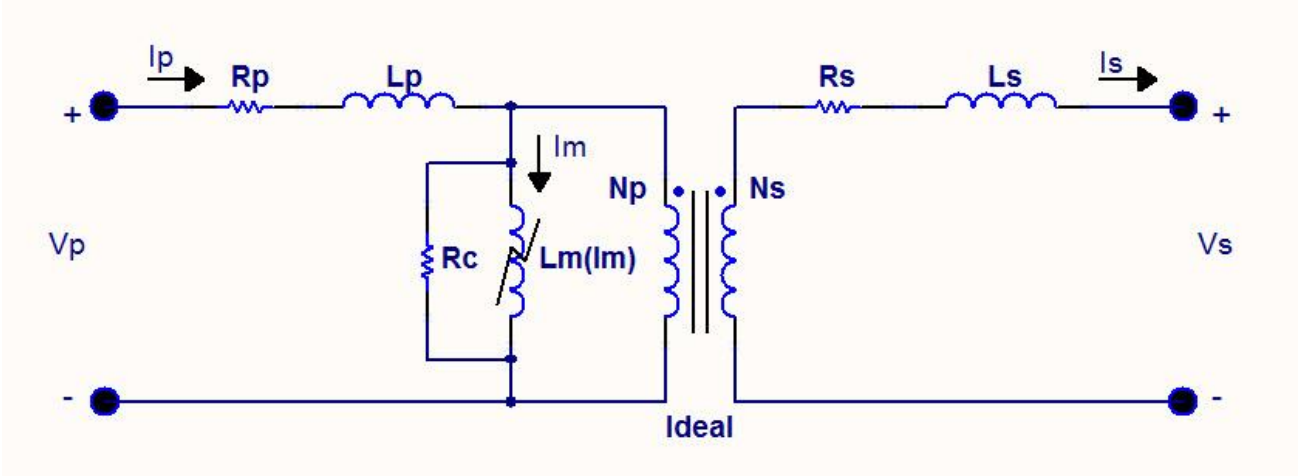
Enter the efficiency of the transformer as a percentage.



Single-phase transformer (equivalent circuit)

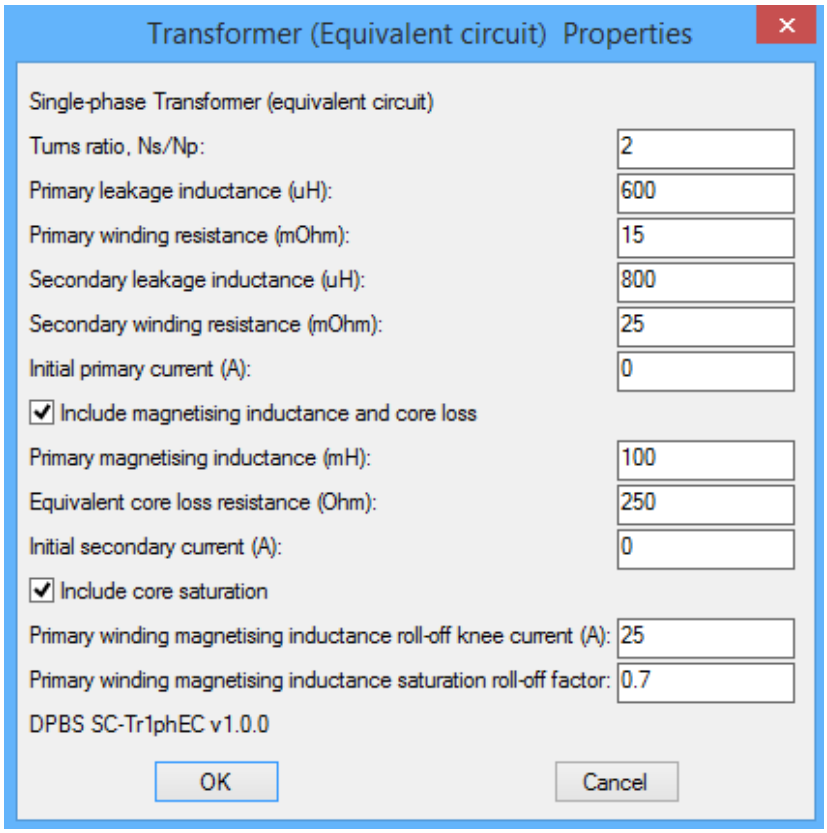
Input Pins:	**Vp**	Primary Input voltage (V).
	Vs	Secondary Output voltage (V).
Output Pins:	**Is**	Secondary output current (A)
	Ip	Primary input current (A).

Circuit schematic (including magnetising inductance, core-loss and core saturation):



Dialog properties:

The single-phase equivalent circuit model transformer block properties menu is shown in the following box which appears when right-clicking on the block.



Turns ratio:

Enter the turns ratio of the transformer.

Primary leakage inductance:

Enter the value of the leakage inductance of the primary winding in micro-Henrys.

Primary winding resistance:

Enter the value of the primary winding resistance in milli-ohms.

Secondary leakage inductance:

Enter the value of the leakage inductance of the secondary winding in micro-Henrys.

Secondary winding resistance:

Enter the value of the secondary winding resistance in milli-ohms.

Initial primary current:

Enter the initial current of the primary winding in amperes.

Include magnetising inductance and core loss:

Select to include the magnetising and core loss components in the transformer model (requires a higher simulation rate for modelling).

Primary magnetising inductance:

Enter the value of the magnetising inductance of the primary winding in milli-Henrys.

Equivalent core loss resistance:

Enter the value of the effective primary winding parallel resistance equivalent to core-loss in ohms.

Initial secondary current:

Enter the initial current of the secondary winding in amperes.

Include core saturation:

Select to include a linearized saturation model of the transformer core.

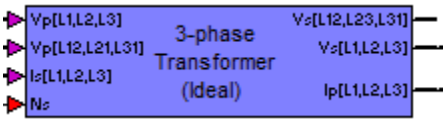
Primary winding magnetising inductance roll-off knee current:

Enter the value of inductor current where the bend in the curve begins.

Primary winding magnetising inductance saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero.

Contents - Simulation

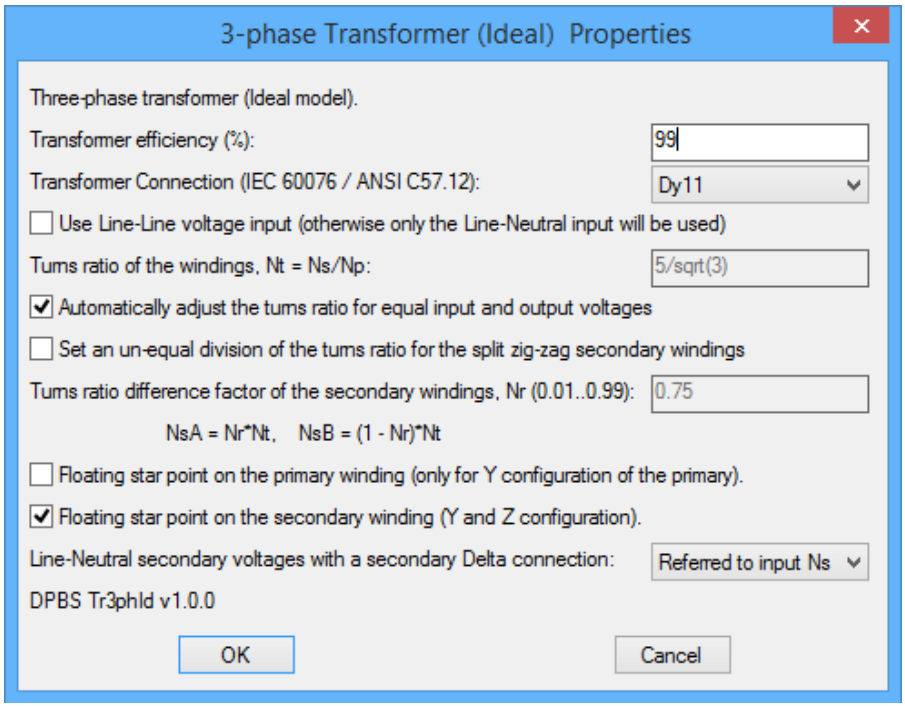


Three-phase transformer (ideal)

Input Pins:	**Vp[L1,L2,L3]**	Primary input line – neutral voltage (V).
	Vp[L12,L23,L31]	Primary input line – line voltage (V), if selected in the configuration.
	Is[L1,L2,L3]	Secondary line currents input (A).
	Ns	Secondary neutral connection (star-point), if used.
Output Pins:	**Vs[L12,L23,L31]**	Secondary line-line output voltage (V)
	Vs[L1,L2,L3]	Secondary line-neutral output voltage (V)
	Ip[L1,L2,L3]	Primary input line currents (A).

Dialog properties:

The ideal 3-phase transformer block properties menu is shown in the following box which appears when right-clicking on the block.

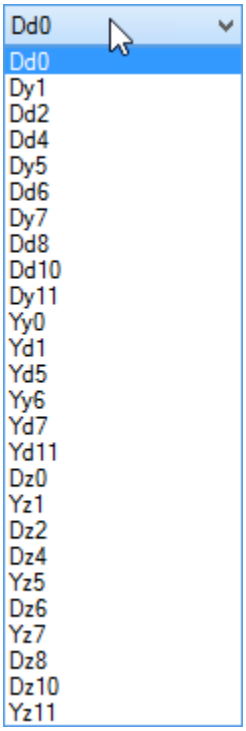


Efficiency:

Enter the efficiency of the transformer as a percentage.

Transformer connection:

Select the desired transformer connection according to IEC-60076 or ANSI C57.12. The choices are:



Use line-line voltage input:

Select to use the line-line voltage input pin, otherwise the line-neutral voltage will be used.

Turns ratio of the windings, Nt = Ns/Np:

Enter the turns ratio of the transformer as a fraction of the number of secondary turns divided by the number of primary turns.

Automatically adjust the turns ratio for equal input and output voltages:

Select this for a 1-to-1 voltage ratio between the primary and secondary windings.

Set an unequal division of the turns ratios for the split zig-zag secondary windings:

Select this to use different turns ratios for the two interconnected secondary windings of the zig-zag connection. This will allow constructing different phase shifts between the primary and secondary voltages.

Turns ratio difference factor of the secondary windings, Nr:

Enter the difference between the turns ratio of the secondary windings required, Nr, as a fraction from 0.01 to 0.99. The actual number of turns are then calculated as such:

$$NsA = Nr*Nt, \quad NsB = (1-Nr)*Nt$$

Floating star point on the primary (Y configuration):

Select this for a floating point star connection on the primary winding.

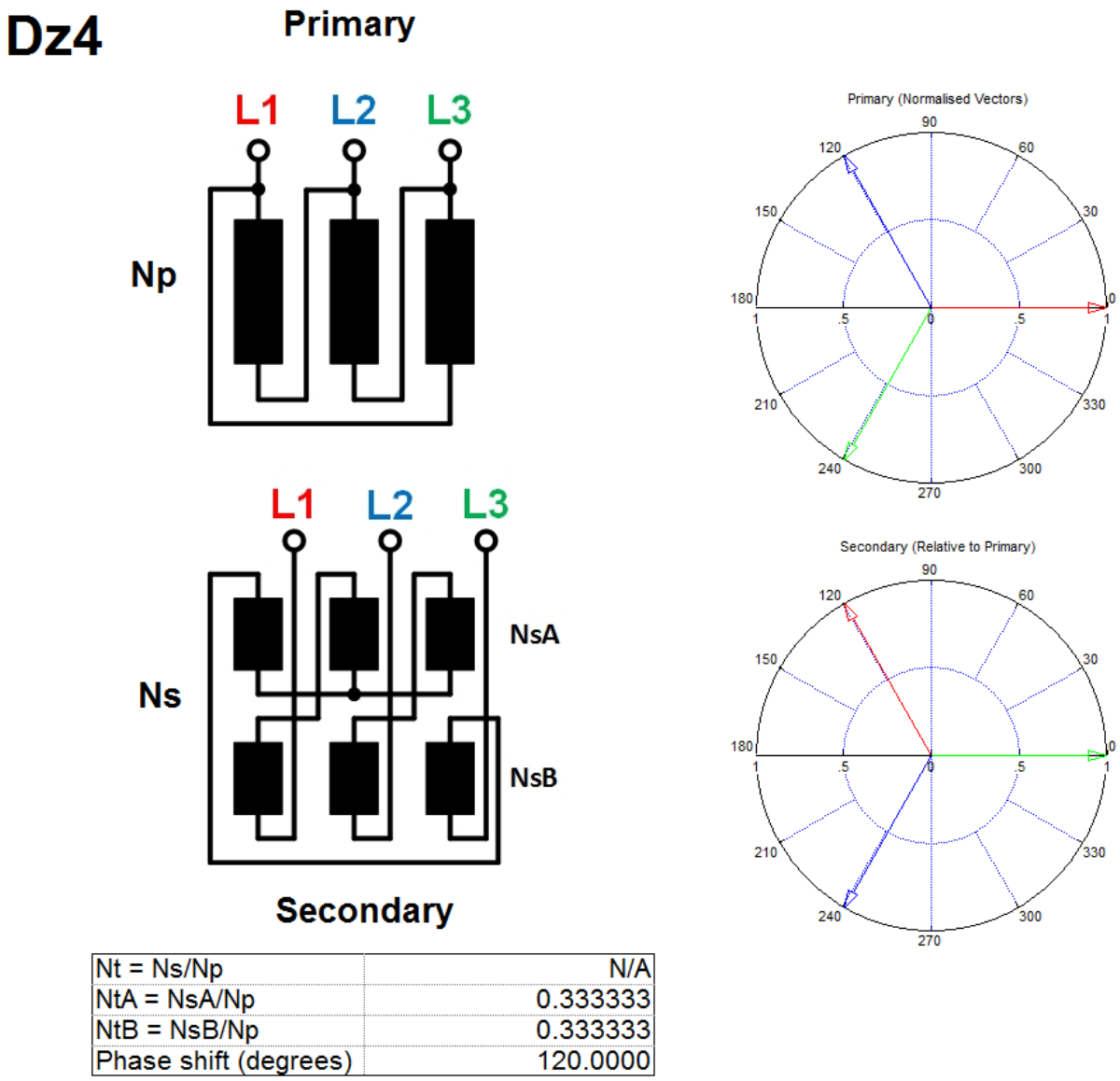
Floating star point on the secondary (Y and Z configurations):

Select this for a floating point star connection on the secondary winding.

Line-neutral secondary voltages with a secondary delta connection:

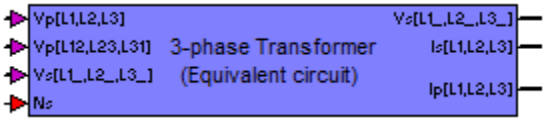
Choose to either approximate the line-neutral voltages with a secondary delta winding configuration or to reference them to the input pin Ns.

The circuit schematic is represented by the winding connections as given below for the Dz4 transformer. These connections can be found internally in the block and change interactively with the selected configuration of the transformer.



Nt = Ns/Np	N/A
NtA = NsA/Np	0.333333
NtB = NsB/Np	0.333333
Phase shift (degrees)	120.0000

Typical internal view of the 3-phase ideal transformer block showing the selected circuit configuration (connections), phasor diagrams of the three phases, the effective turns ratios and phase shift from primary to secondary.



Three-phase transformer (equivalent circuit)

Input Pins: **Vp[L1,L2,L3]** 3-phase primary line to neutral voltage input.

Vp[L12,L23,L31] 3-phase primary line to line voltage input. Select in the dialog which voltage to use.

Vs[L1_,L2_,L3_] 3-phase secondary voltage input. These will be line-line voltages if the line-to-line voltages are selected as the secondary voltage to this pin, otherwise line-neutral.

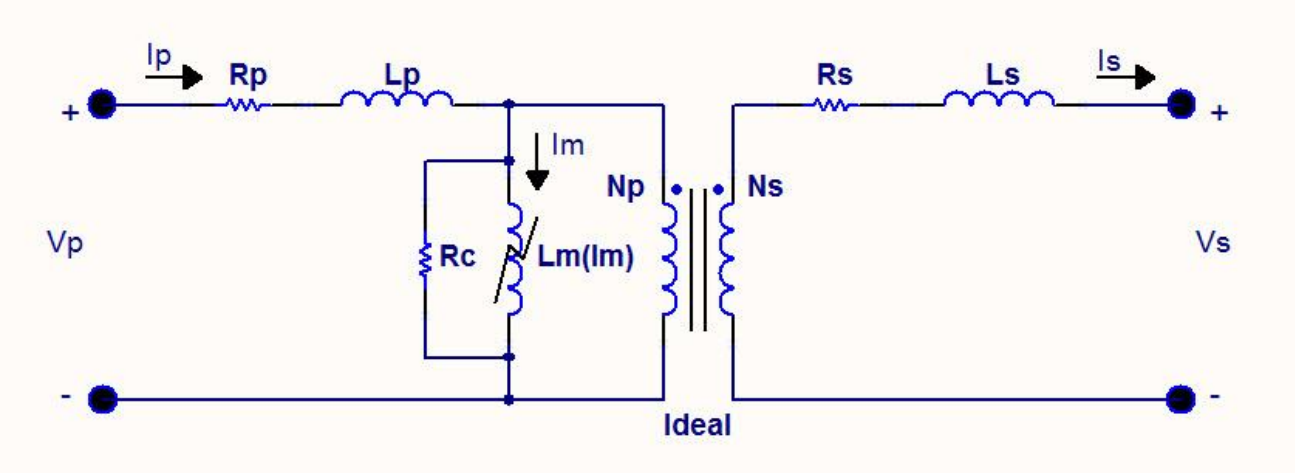
Ns Input for the secondary connection the neutral point

Output Pins: **Vs[L1_,L2_,L3_]** 3-phase secondary voltage output. These will be line-neutral voltages if the line-to-line voltages are selected as the secondary voltage at the input pin, otherwise line- line.

Is[L1,L2,L3] 3-phase secondary output line currents.

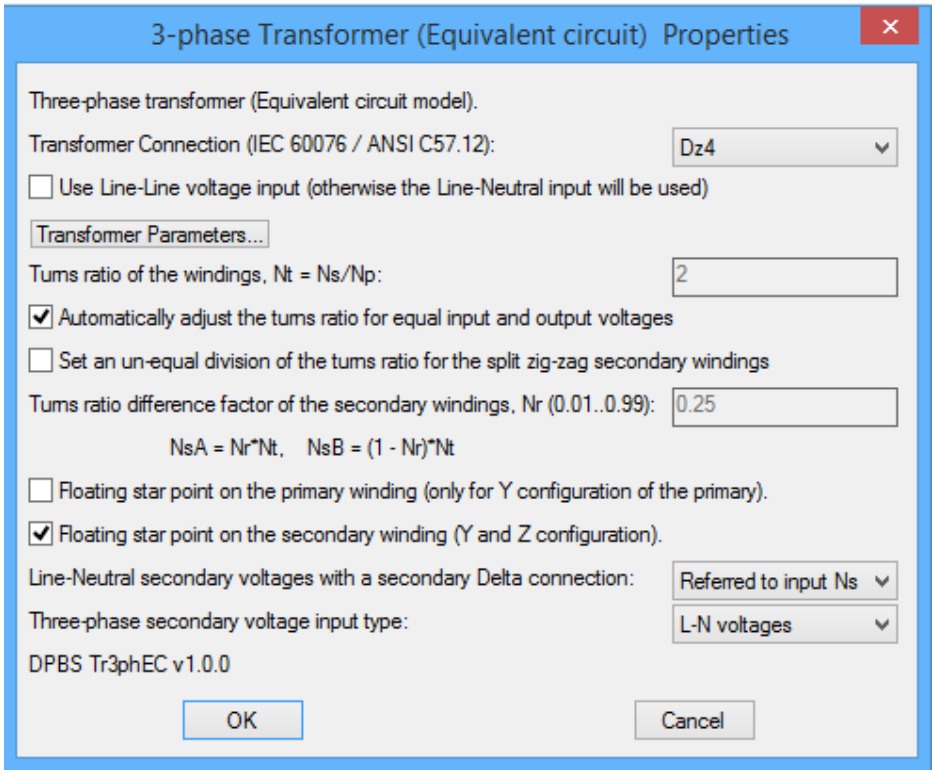
Ip[L1_,L2_,L3_] 3-phase primary input line currents.

Circuit schematic (per phase, including magnetising inductance, core-loss and core saturation):



Dialog properties:

The 3-phase transformer (equivalent circuit) properties menu is shown in the following box which appears when right-clicking on the block.

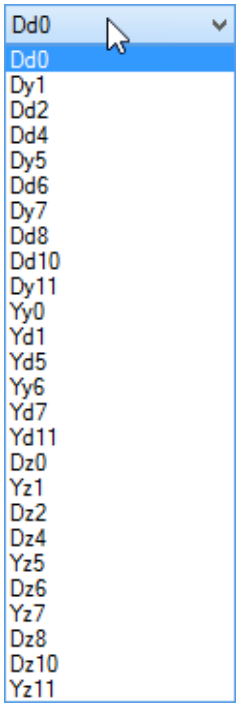


Efficiency:

Enter the efficiency of the transformer as a percentage.

Transformer connection:

Select the desired transformer connection according to IEC-60076 or ANSI C57.12. Again the choices are:



Use line-line voltage input:

Select to use the line-line voltage input pin, otherwise the line-neutral voltage will be used.

Turns ratio of the windings, Nt = Ns/Np:

Enter the turns ratio of the transformer as a fraction of the number of secondary turns divided by the number of primary turns.

Automatically adjust the turns ratio for equal input and output voltages:

Select this for a 1-to-1 voltage ratio between the primary and secondary windings.

Set an unequal division of the turns ratios for the split zig-zag secondary windings:

Select this to use different turns ratios for the two interconnected secondary windings of the zig-zag connection. This will allow constructing different phase shifts between the primary and secondary voltages.

Turns ratio difference factor of the secondary windings, Nr:

Enter the difference between the turns ratio of the secondary windings required, Nr, as a fraction from 0.01 to 0.99. The actual number of turns are then calculated as such:

$$NsA = Nr*Nt, \quad NsB = (1-Nr)*Nt$$

Floating star point on the primary (Y configuration):

Select this for a floating point star connection on the primary winding.

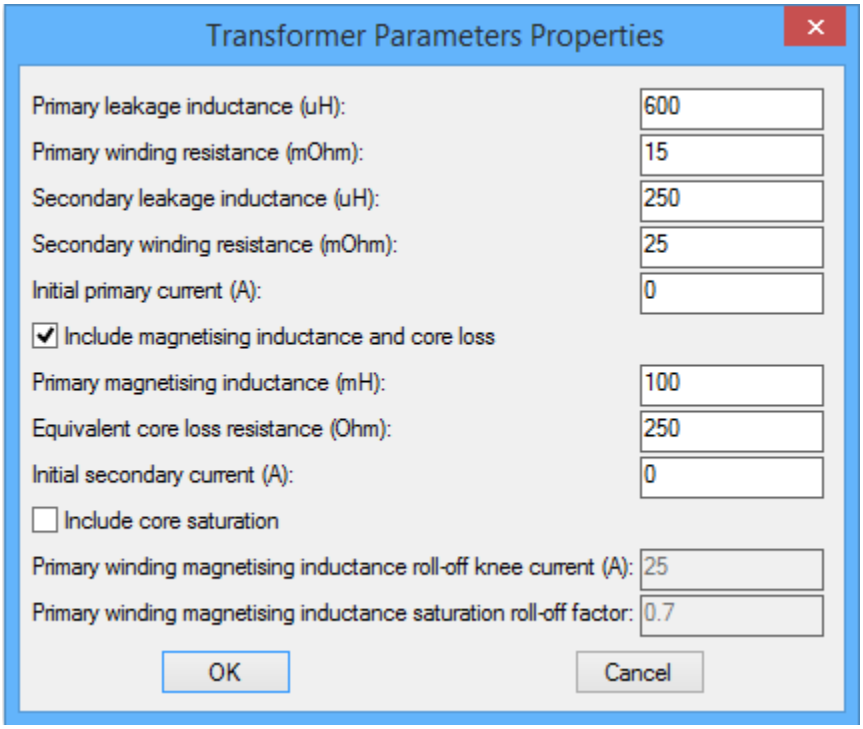
Floating star point on the secondary (Y and Z configurations):

Select this for a floating point star connection on the secondary winding.

Line-neutral secondary voltages with a secondary delta connection:

Choose to either approximate the line-neutral voltages with a secondary delta winding configuration or to reference them to the input pin Ns.

Transformer Parameters:



Primary leakage inductance:

Enter the value of the leakage inductance of the primary winding in micro-Henrys.

Primary winding resistance:

Enter the value of the primary winding resistance in milli-ohms.

Secondary leakage inductance:

Enter the value of the leakage inductance of the secondary winding in micro-Henrys.

Secondary winding resistance:

Enter the value of the secondary winding resistance in milli-ohms.

Initial primary current:

Enter the initial current of the primary winding in amperes.

Include magnetising inductance and core loss:

Select to include the magnetising and core loss components in the transformer model (requires a higher simulation rate for modelling).

Primary magnetising inductance:

Enter the value of the magnetising inductance of the primary winding in milli-Henrys.

Equivalent core loss resistance:

Enter the value of the effective primary winding parallel resistance equivalent to core-loss in ohms.

Initial secondary current:

Enter the initial current of the secondary winding in amperes.

Include core saturation:

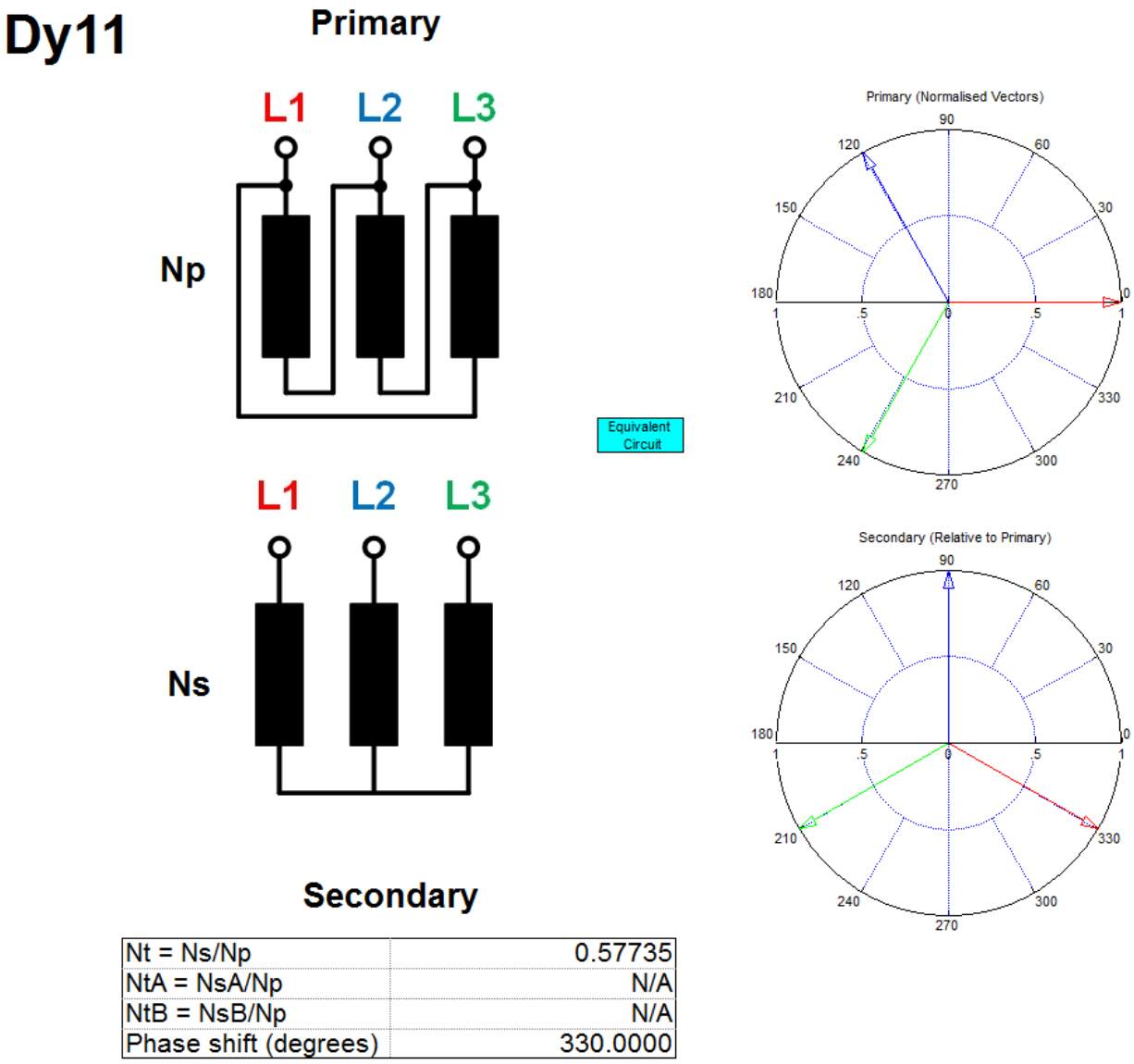
Select to include a linear saturation model of the primary core.

Primary winding magnetising inductance roll-off knee current:

Enter the value of primary winding current where the bend in the saturation curve characteristic begins.

Primary winding magnetising inductance saturation roll-off factor:

The roll-off factor of the primary winding permeability should be inserted here. For transformers modelled without saturation, enter a value of zero.



Nt = Ns/Np	0.57735
NtA = NsA/Np	N/A
NtB = NsB/Np	N/A
Phase shift (degrees)	330.0000

Similarly, the 3-phase transformer with equivalent circuit model shows the current configuration internally in the block.

Contents - Simulation

Active Components



Analog comparator

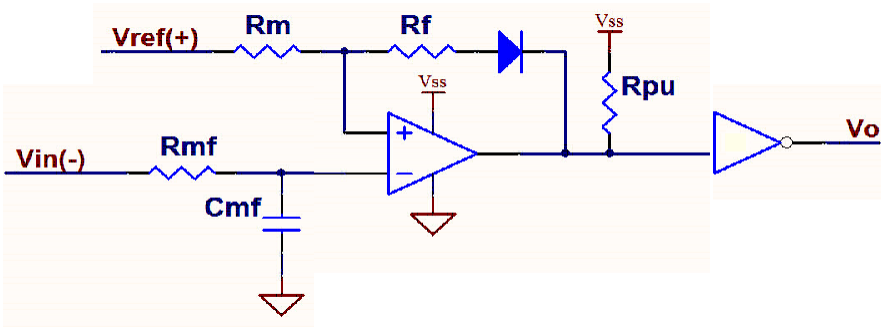
Models an analog comparator with its resistive network.

Input Pins: **Vin(-)** Input voltage (V), negative input to the comparator.

Vref(+) Input reference voltage, positive input to the comparator.

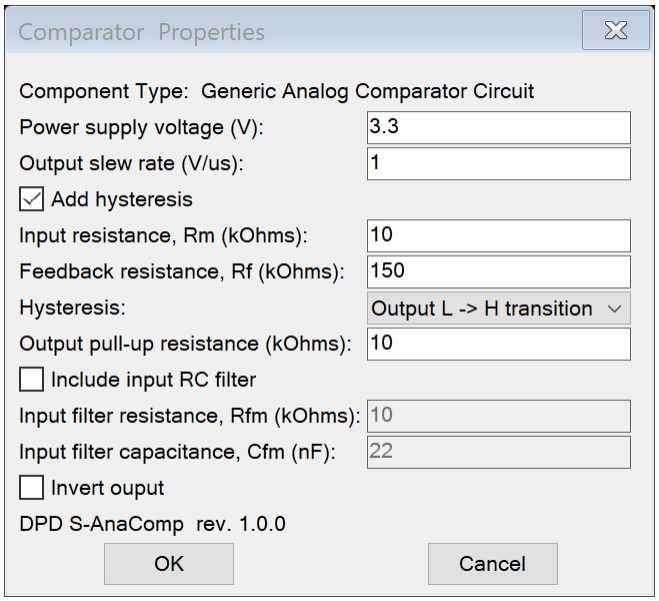
Output Pins: **Vo** Comparator output

Circuit schematic:



Dialog properties:

The analog comparator block properties menu is shown in the following box which appears when right-clicking on the block.



Power supply voltage (V):

Enter the power supply voltage in volts.

Output slew rate (V/us):

Enter the maximum slew rate of the output in volts / microsecond.

Add hysteresis:

Check this if hysteresis is desired.

Input resistance, Rm:

Enter the value of the input resistance in kilo-ohms in series with the negative comparator input.

Feedback resistance, Rf:

Enter the value of the feedback resistance in kilo-ohms from the output to the positive comparator input.

Hysteresis:

Select the type of hysteresis required, the circuit amd model will be adapted accordingly.

Output pull-up resistance, Rpu:

Enter the value of the pull-up resistance in kilo-ohms on the comparator output.

Include RC filter:

Select this option if an RC filter is desired on the input to the comparator.

Input filter resistance, Rfm:

Enter the value of the filter resistance in kilo-ohms for the RC filter at the comparator input.

Input capacitance, Cfm:

Enter the value of the filter capacitance in nano-farads in series for the RC filter at the comparator input.

Invert output:

Select this option to invert the output of the comparator.



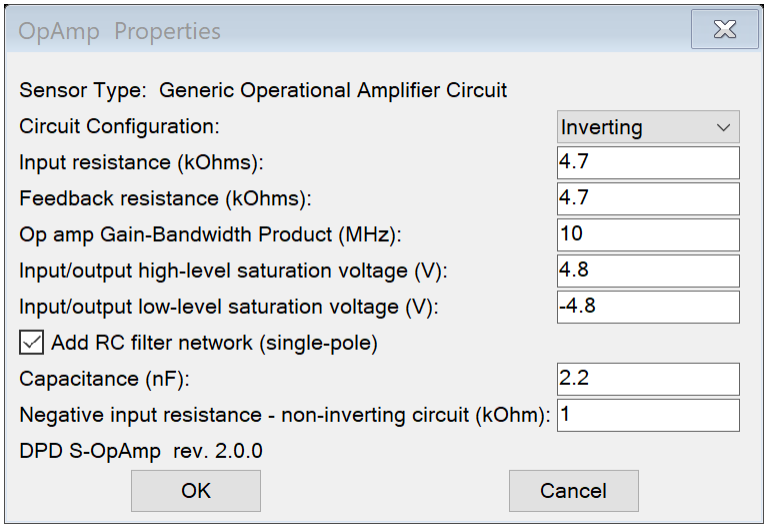
Operational amplifier

This block models a typical operational amplifier (op-amp) circuit including the input and feedback resistances to determine the closed-loop gain and optionally a capacitance to modify the closed-loop pole frequency.

Input Pins:	V**in**	Input voltage (V).
	F (Hz):	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output Pins:	**Vo**	Output voltage (V).
	S(s):	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

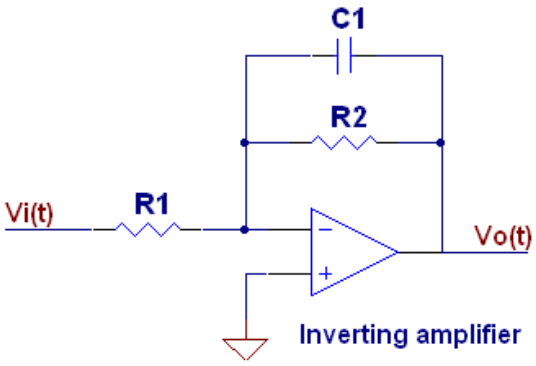
The op-amp block properties menu is shown in the following box which appears when right-clicking on the block.

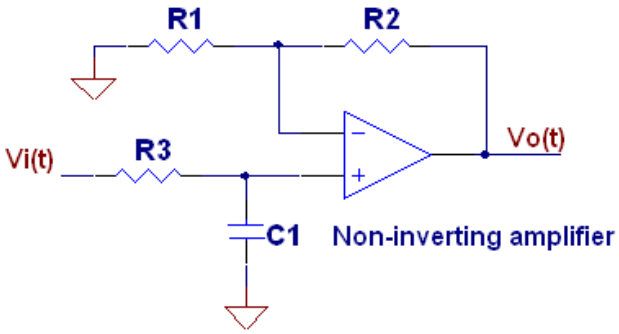


Circuit configuration:

The choices here are:

1. Inverting amplifier
2. Non-inverting amplifier





Input resistance:

This is the resistance R1in kilo-Ohms at the input pin which determines the opamp gain together with R2.

Feedback resistance:

This is the resistance in the feedback circuit R2 in kilo-Ohms.

Opamp Gain-bandwidth product:

This is a characteristic of the op-amp itself and is included in the transfer function of the amplifier. The value will be found in the data sheet of the op-amp.

Input/output high-level saturation voltage:

The upper saturation voltage of the op-amp and the upper voltage limit on the input pins of the op-amp.

Input/output low-level saturation voltage:

The lower saturation voltage of the op-amp and the lower voltage limit on the input pins of the op-amp.

Add RC filter:

The filter is added in the op-amp circuit as in the circuit schematics.

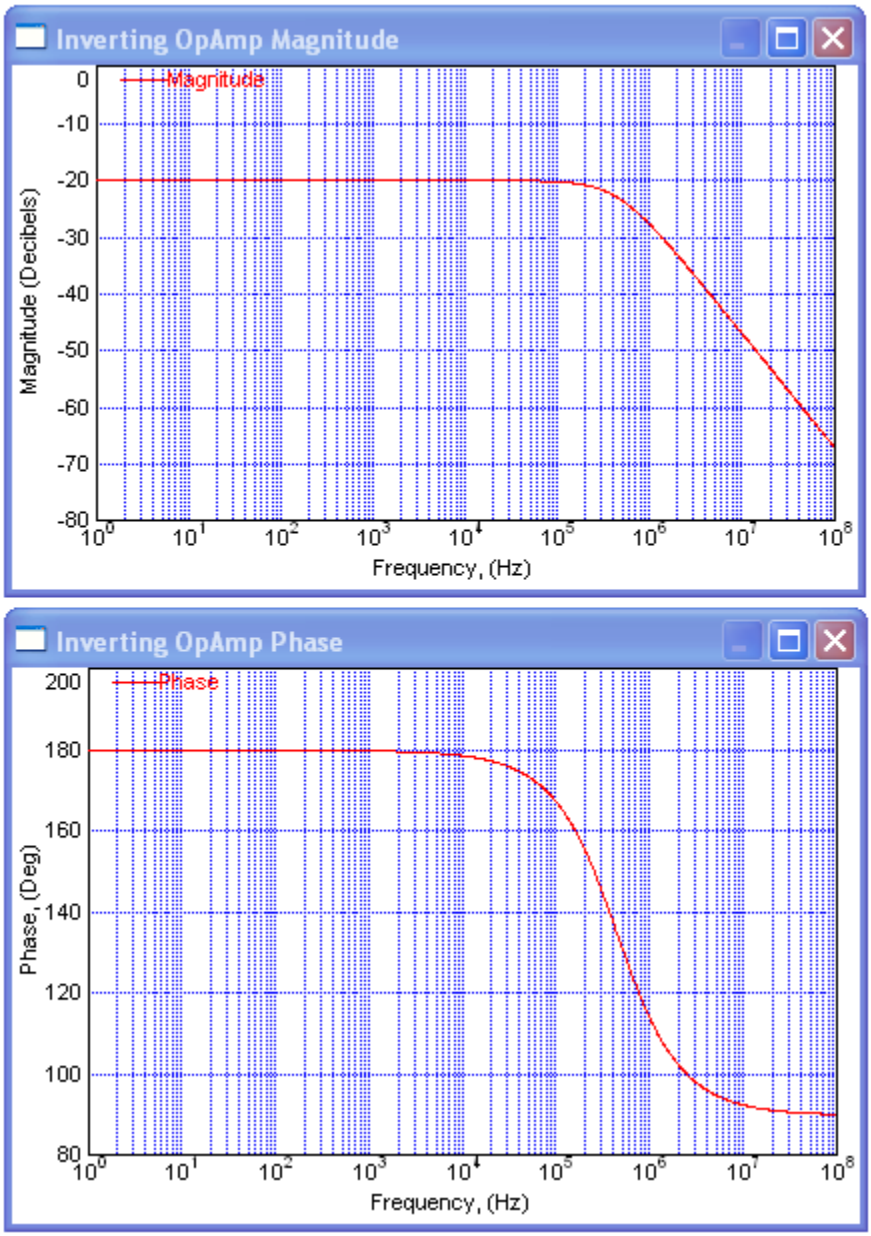
Capacitance (nF):

Enter the value of the filter capacitance C1 in nano-farads.

Negative input resistance – non-inverting circuit (kOhm):

Enter the value of the resistance of R3 in kilo-Ohms for the non-inverting amplifier circuit only. This value can vary from R1 and R2 in this case only.

The Op-amp is modelled as a single pole with a constant gain-bandwidth product. The op-amp open loop gain will therefore fall-off at -20 dB/decade after the cut-off frequency.



Contents - Simulation



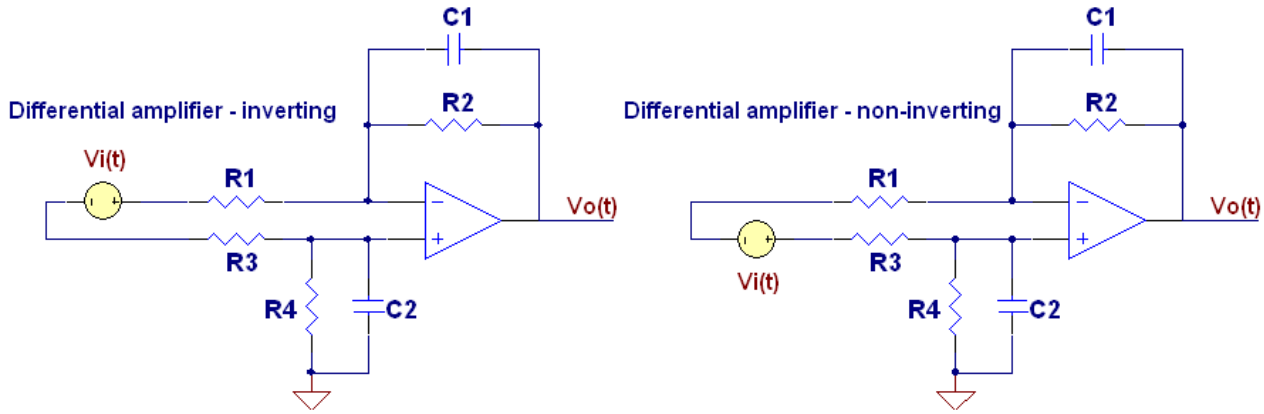
Difference Amplifier

The difference amplifier is similar to the operational amplifier block except that it models a closed-loop circuit where the output is equal to the difference of the two inputs times the closed-loop gain.

Input Pins:	**V+**	Positive input voltage (V).
	V-	Negative input voltage (V).
	F (Hz)	Frequency input for frequency response analysis.
Output Pins:	**Vo**	Output voltage (V).
	S(s)	Frequency response output.

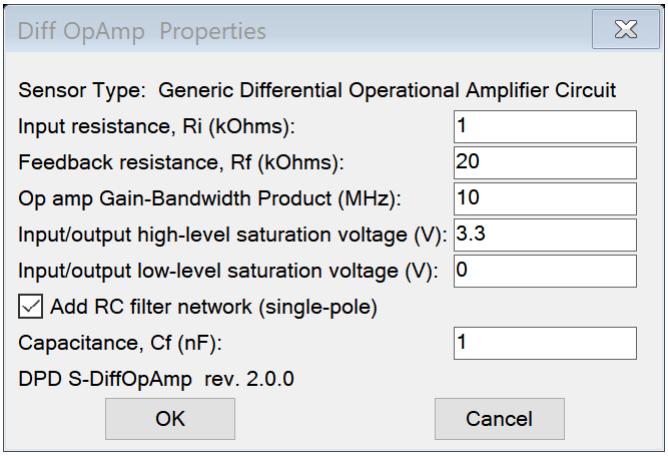
Schematic:

1. Differential amplifier - inverting
2. Differential amplifier – non-inverting.



Dialog properties:

The difference amplifier block properties menu is shown in the following box which appears when right-clicking on the block.



Input resistance:

This is the resistance R1(which equals R3) in kilo-Ohms at the input pin which determines the differential amp gain, together with R2 and R4.

Feedback resistance:

This is the resistance in the feedback circuit R2 (which equals R4) in kilo-Ohms.

Op-amp Gain-bandwidth product:

This is a characteristic of the op-amp itself and is included in the transfer function of the amplifier. The value will be found in the data sheet of the op-amp.

Input/output high-level saturation voltage:

The upper saturation voltage of the op-amp and the upper voltage limit on the input pins of the op-amp.

Input/output low-level saturation voltage:

The lower saturation voltage of the op-amp and the lower voltage limit on the input pins of the op-amp.

Note that, for simplicity, it is assumed that the op-amp input and output limits are identical and that the op-amp differential input voltage limit is twice that of each input limit. If different limiting values are needed to be applied for the input and output, they can be applied externally to the block. Note also that the input limit refers to the limit at the input pins at the op-amp itself and not the limit of the op-amp input circuit or the block input. High input voltages can be used at the input if large values of input resistance (with respect to the feedback resistance) are used.

Add RC filter network (single pole):

The filter is added in the differential amp circuit as in the circuit schematics.

Capacitance:

Enter the value of the filter capacitance C1 (which equals C2) in nano-farads.

The difference amplifier is modelled similarly to the op-amp block with differences due only to the external circuit configuration.

Contents - Simulation

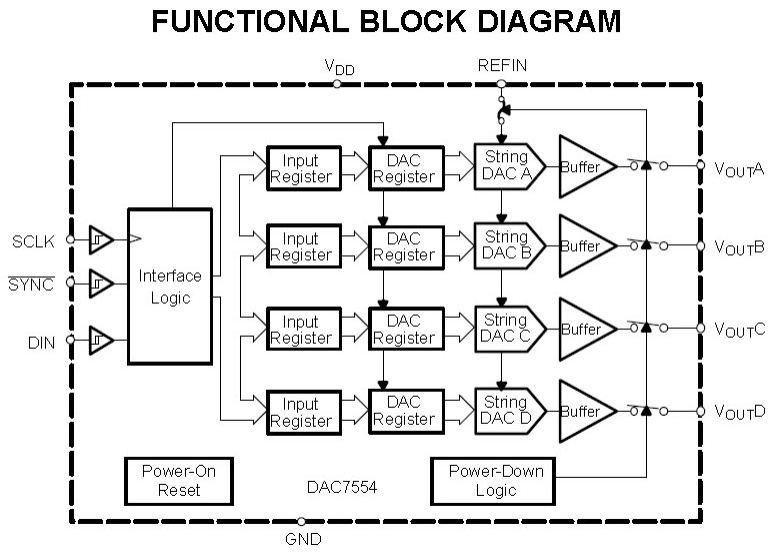


DAC7554

This block models a 4-channel, 12-bit digital to analog converter (DAC) and specifically the TI DAC7554. This block can be used together with the MCU peripherals emulators for the SPI interface (master).

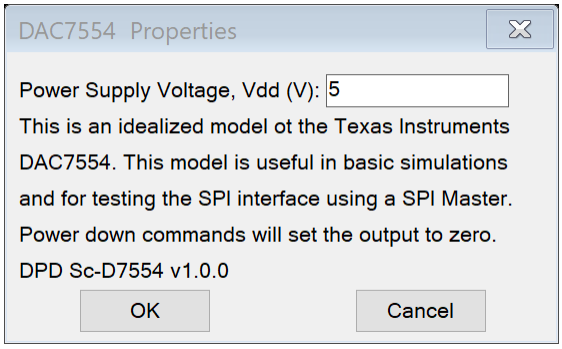
Input Pins:	**REFIN**	Input reference voltage (V).
	SCLK	Serial clock in from a SPI master.
	DIN	Serial data in from a SPI master.
	SYNC/	Sync input to accept data (STE output from SPI master).
Output Pins:	**VoutA**	Output of DACA
	VoutB	Output of DACB
	VoutC	Output of DACC
	VoutD	Output of DACD

Functional block diagram (from data sheet):



Dialog properties:

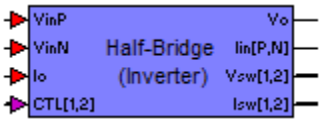
The DAC7554 block properties menu is shown in the following box which appears when right-clicking on the block.



Power Supply voltage, Vdd (V):

Enter the power supply voltage to be applied to the block in volts.

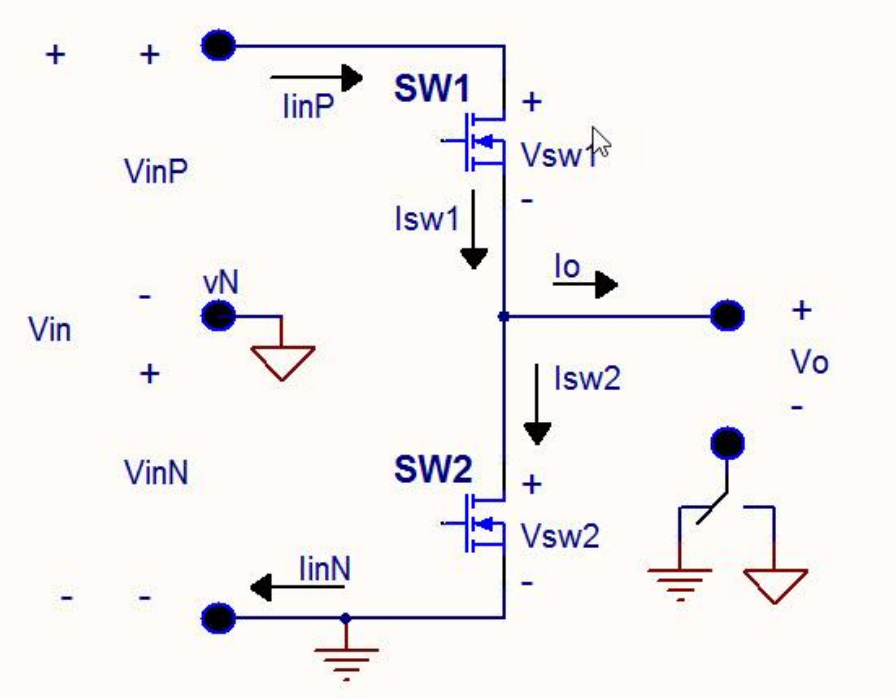
Power Switches (Bridges)



Inverter Half-bridge

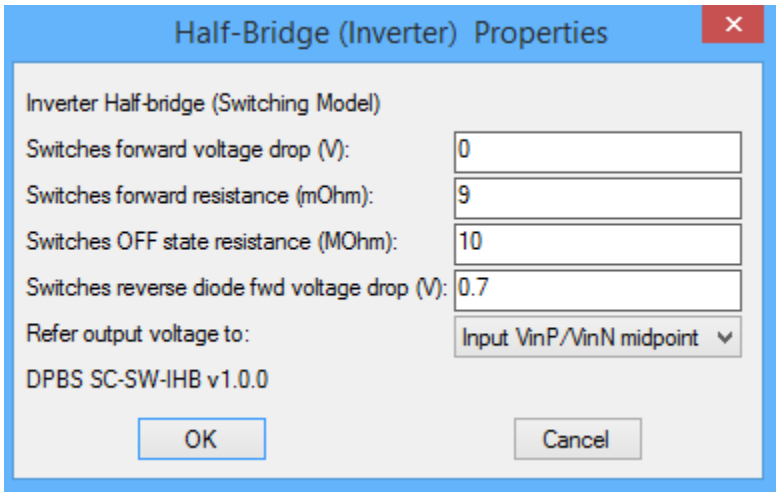
Input Pins:	**VinP**	Input positive DC source voltage (V).
	VinN	Input negative DC source voltage (V).
	Io	Output current on the bridge (A).
	CTL[1..2]	Input control signals SW1..2 for the switches.
Output Pins:	**Vo**	Output voltage of the bridge (V)
	Iin	Input current to the bridge (A).
	Vsw[1..2]	Voltage appearing across the switches.
	Isw[1..2]	Switch currents.

Circuit schematic:



Dialog properties:

The inverter half-bridge block properties menu is shown in the following box which appears when right-clicking on the block.



Switches forward voltage drop:

Enter the forward voltage drop of the switches in volts.

Switches forward resistance:

Enter the resistance of the switch in the ON state in milli-ohms.

Switches Off-state resistance:

Enter the off-state resistance of the switches in mega-ohms.

Switches reverse diode fwd voltage drop:

Enter the forward voltage drop of the switches integrated reverse diode in volts.

Refer output voltage to:

Choose either the midpoint of VinP / VinN (VinN if VinN = 0) or the negative rail.

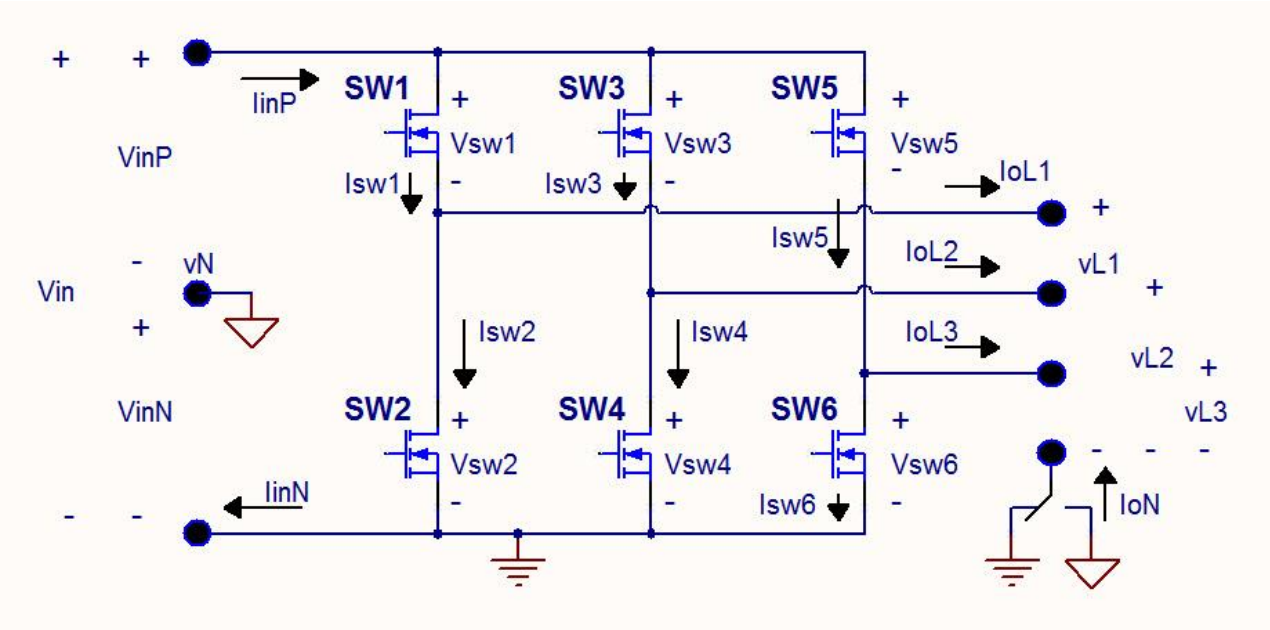


Inverter bridge, 3phase - 3leg

Models are three-phase, three-leg bridge in the inverter mode.

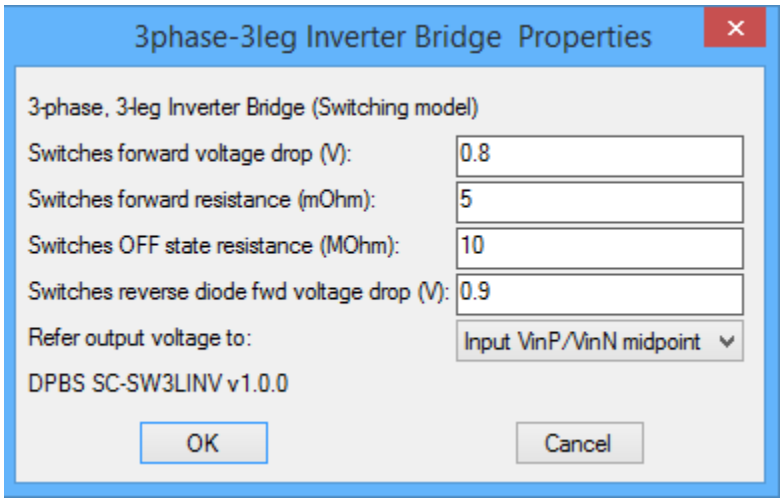
Input Pins:	**VinP**	Input positive DC source voltage (V).
	VinN	Input negative DC source voltage (V).
	Io[L1,L2,L3]	Output current on the bridge (A).
	CTL[1..6]	Input control signals SW1..6 for the switches.
Output Pins:	**Vo[L12,L23,L31]**	Output line-to-line voltage (V)
	Vo[L1,L2,L3]	Output line-to-neutral voltage (V).
	Iin	Input current to the bridge (A).
	Vsw[1..6]	Voltage appearing across the switches.
	Isw[1..6]	Switch currents.

Circuit schematic:



Dialog properties:

The inverter 3-phase, 3-leg bridge block properties menu is shown in the following box which appears when right-clicking on the block.



Switches forward voltage drop:

Enter the forward voltage drop of the switches in volts.

Switches forward resistance:

Enter the resistance of the switch in the ON state in milli-ohms.

Switches Off-state resistance:

Enter the off-state resistance of the switches in mega-ohms.

Switches reverse diode fwd voltage drop:

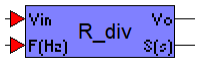
Enter the forward voltage drop of the switches integrated reverse diode in volts.

Refer output voltage to:

Choose either the midpoint of VinP / VinN (VinN if VinN = 0) or the negative rail.

Sensors

The sensors sub-section within the simulation section of the Digital Power Designer is designed to emulate many typical voltage and current sensors used in digital power applications.



Resistive divider (voltage sense)

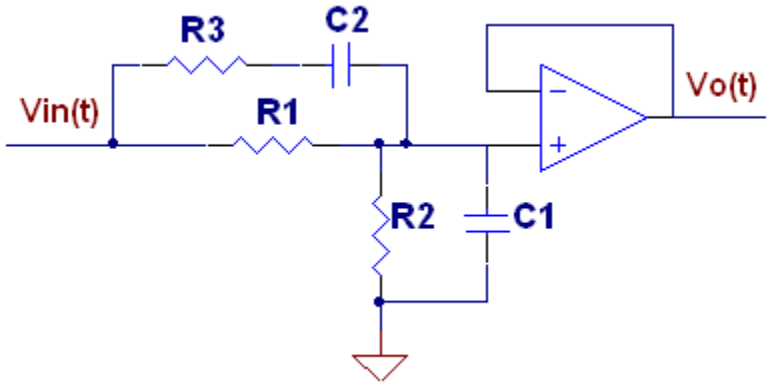
Input Pins: **Vin** Sensed input voltage (V).

F (Hz): Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.

Output Pins: **Vo** Sensor output voltage (V)

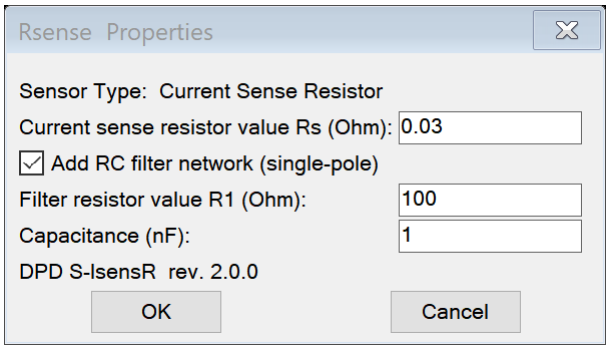
S(s): When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Circuit schematic:



Dialog properties:

The resistive divider block properties menu is shown in the following box which appears when right-clicking on the block.



Series resistor value R1:

Enter the value of the series resistor R1 in Ohms.

Parallel resistor R2:

Enter the value of the parallel resistor R2 in Ohms.

Add capacitor in parallel with R2:

Enables a single pole in the voltage measurement (for filtering noise or anti-aliasing).

Capacitance C1:

Enter the value of the capacitor C1 in nano-Farads.

Add RC network in parallel with R1:

Enables the addition of a zero in the loop transfer function.

Parallel resistor R3:

Enter the value of the resistor R3 in Ohms.

Capacitance C2:

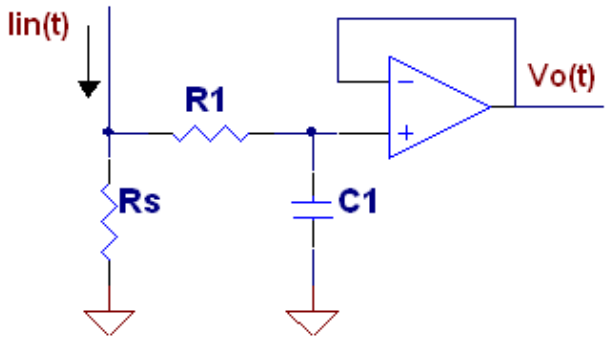
Enter the value of the capacitor C2 in nano-Farads.



Current sense resistor

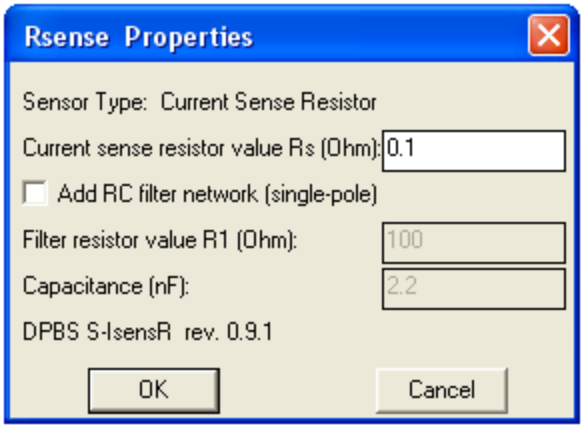
Input Pins:	**Iin**	Sensed input current (A).
	F (Hz):	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output Pins:	**Vo**	Sensor output voltage (V) – voltage across the sense resistor.
	S(s):	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Circuit schematic:



Dialog properties:

The current sense resistor block properties menu is shown in the following box which appears when right-clicking on the block.



Current sense resistor value:

Enter the value of the current sensing resistor Rs in Ohms.

Add RC filter network:

Check this box to add a first order filter to the current measurement.

Filter resistor value:

Enter the value of the filter resistance R1 in Ohms.

Capacitance:

Enter the value of the filter capacitance C1 in nano-farads.



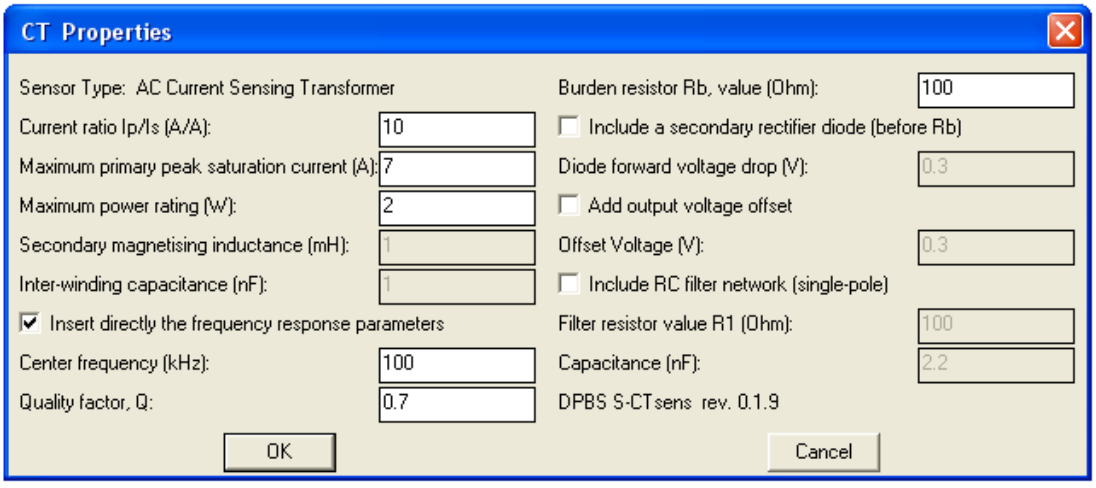
AC current transformer

Input Pins: **Iin** Sensed primary current (A).

Output Pins: **Vo** Sensor output voltage (V) – voltage across the burden resistor.

Dialog properties:

The AC current transformer block properties menu is shown in the following box which appears when right-clicking on the block.



Current ration Ip / Is:

Enter the current transformer primary to secondary current transfer ratio (A/A).

Maximum primary peak saturation current:

The saturation current referred to the primary winding – the secondary sense current will be limited at this value times the current ratio.

Maximum power rating:

The power rating of the current transformer – the average output power will be limited at this value.

Secondary magnetizing inductance:

The magnetizing inductance of the secondary winding in milli-Henries.

Inter-winding capacitance

The capacitance of the windings which together with the magnetizing inductance determines the frequency response of the current sensing transformer.

Insert directly the frequency response parameters:

If the current transformer parameters are not known, the frequency response parameters can be directly entered if this box is checked.

Centre frequency:

Enter the centre band frequency in kilohertz.

Quality factor:

Enter the quality factor, Q, of the current transformer response.

Burden resistor value:

Enter the value of the burden resistance (current transformer load) in Ohms.

Include secondary rectifier diode:

A diode can be included on the current transformer secondary to maintain positive values only (in practise, a current path will be required for the negative current in order to reset the winding and it is assumed that this has been correctly performed so that this effect is not accounted for here).

Diode forward voltage drop:

Enter the forward voltage drop of the rectifier diode in Volts.

Add output voltage offset:

Check this box to add a DC offset to the measurement (e.g. for measuring AC currents with a positive supply only).

Offset voltage:

Enter the offset voltage in Volts.

Include RC filter network:

Check this to include a first order filter on the voltage output.

Filter resistor value:

Enter the filter resistance value in Ohms.

Capacitance:

Enter the filter capacitance value in nano-farads.

Contents - Simulation



Isolated current sensor

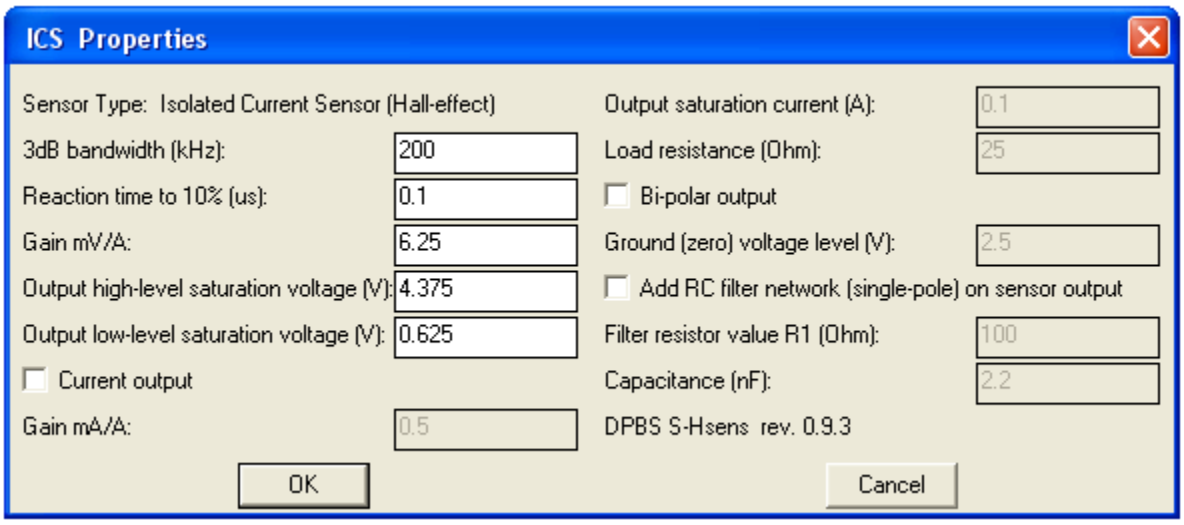
This sensor is designed to model a hall type of current sensor which is capable of measuring both DC and AC currents.

Input Pins: **Iin** Sensed input current (A).

Output Pins: **Vo** Sensor output voltage (V).

Dialog properties:

The isolated current sensor block properties menu is shown in the following box which appears when right-clicking on the block.



3dB cut-off frequency:

The cut-off frequency of the sensor or the bandwidth.

Reaction time to 10%:

This is the time it takes for the output to reach 10% of its final output on an input step and can be found in the datasheet of a particular device.

Gain:

This is the gain of the device in millivolts / amperes for a voltage output device.

Output high-level saturation voltage:

The maximum high-level output voltage for a voltage output device.

Output low-level saturation voltage:

The minimum low-level output voltage for a voltage output device.

Current output:

Current sensors can have either a voltage or a current output. For hall sensors, generally an open-loop device has a voltage output while a closed-loop, compensated device has a current output. Check this box for a current output device.

Gain:

This is the gain for a current output device in milli-amperes / amperes.

Output saturation current:

The output secondary saturation current in Amperes. It is assumed that the device is bi-polar in this case and the current saturation is dual polarity.

Load resistance:

The load resistance on the current output sensor in Ohms.

Bi-polar output:

Check this box for a bi-polar measurement (both sensors have a voltage output at this point since the current sensor has a load resistance converting it to voltage).

Ground (zero) voltage level:

Enter the ground voltage level required (this option can apply an offset to a bi-polar sensor centred at the ground or zero voltage in order to measure both positive and negative currents with a uni-polar ADC).

Add RC filter network:

A single pole RC filter can be added at the output of the sensor.

Filter resistor:

Enter the filter resistance value in Ohms.

Capacitance:

Enter the filter capacitance value in nano-farads.

Contents - Simulation



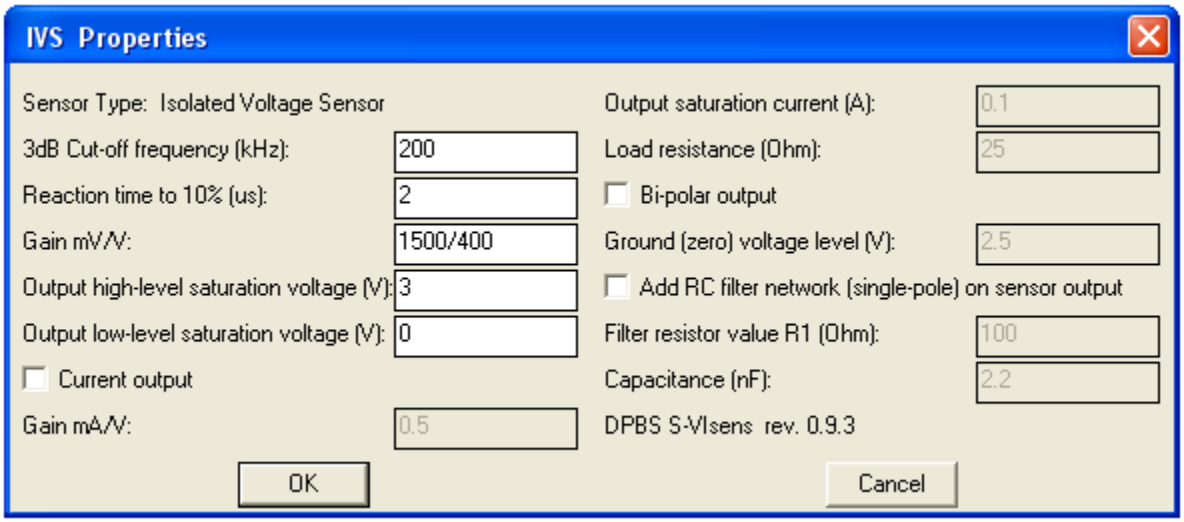
Isolated voltage sensor

This sensor is designed to model an isolated voltage sensor and can be either an opto-isolated type of sensor with amplifier or a hall type of voltage sensor. The sensor is capable of measuring both DC and AC voltages.

Input Pins:	**Vin**	Sensed input voltage (V).
Output Pins:	**Vo**	Sensor output voltage (V).

Dialog properties:

The isolated voltage sensor block properties menu is shown in the following box which appears when right-clicking on the block.



3dB cut-off frequency:

The cut-off frequency of the sensor or the bandwidth.

Reaction time to 10%:

This is the time it takes for the output to reach 10% of its final output on an input step and can be found in the datasheet of a particular device.

Gain:

This is the gain of the device in millivolts per volt for a voltage output device.

Output high-level saturation voltage:

The maximum high-level output voltage for a voltage output device.

Output low-level saturation voltage:

The minimum low-level output voltage for a voltage output device.

Current output:

Isolated voltage sensors can have either a voltage or a current output. Check this box for a current output device.

Gain:

This is the gain for a current output device in milli-amperes / volt.

Output saturation current:

The output secondary saturation current in Amperes. It is assumed that the device is bi-polar in this case and the current saturation is dual polarity.

Load resistance:

The load resistance on the current output sensor in Ohms.

Bi-polar output:

Check this box for a bi-polar measurement (both sensors have a voltage output at this point since the current sensor has a load resistance converting it to voltage).

Ground (zero) voltage level:

Enter the ground voltage level required (this option can apply an offset to a bi-polar sensor centred at the ground or zero voltage in order to measure both positive and negative AC voltages with a uni-polar ADC).

Add RC filter network:

A single pole RC filter can be added at the output of the sensor.

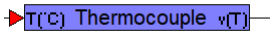
Filter resistor:

Enter the filter resistance value in Ohms.

Capacitance:

Enter the filter capacitance value in nano-farads.

Contents - Simulation



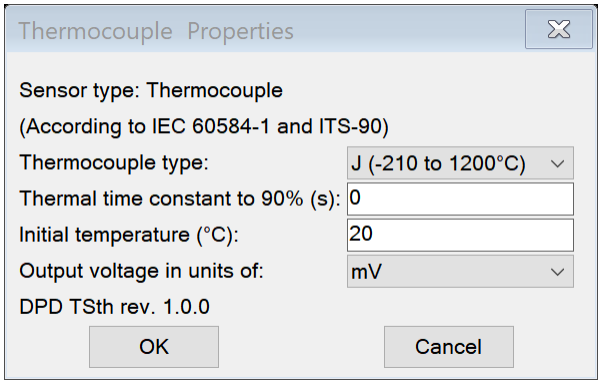
Thermocouple

Input Pins: **T(°C)** The temperature measured by the thermocouple (°C).

Output Pins: **v(T)** The thermal voltage produced by the thermocouple in the selected units.

Dialog properties:

The Thermocouple block properties menu is shown in the following box which appears when right-clicking on the block.



Thermocouple type:

Select the type of thermocouple to model. The choices and valid temperature range are:

1. J (-210 to 1200°C)
2. K (-270 to 1372°C)
3. T (-270 to 400°C)
4. E (-270 to 1000°C)
5. N (-270 to 1300°C)
6. B (0 to 1820°C)
7. R (-50 to 1786.1°C)
8. S (-50 to 1786.1°C)

Thermal time constant to 90%:

Enter a time constant in seconds for any temperature variation. A value of zero here will have no time constant.

Initial temperature (°C):

Enter the initial temperature of the thermocouple in °C. This is relevant when the thermal time constant is > 0.

Output voltage in units of:

Select the desired units for the thermal output voltage. The choices are:

1. µV
2. mV
3. V

Contents - Simulation



Temperature sensor (RTD)

Input Pins: **T(°C)** The currently measured temperature in °C.

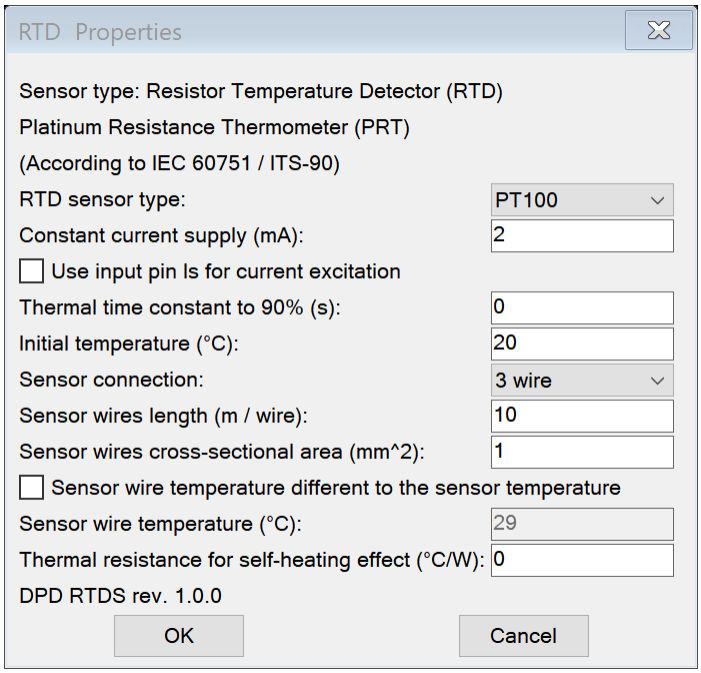
Is (A) If enabled, the current excitation input to the RTD device in Amperes.

Output Pins: **Vs(t)** The RTD sensor output voltage (V).

Vp(t) The RTD sensor output voltage (V).

Dialog properties:

The RTD temperature sensor block properties menu is shown in the following box which appears when right-clicking on the block.



RTD sensor type:

Select the type of RTD sensor to model. The choices are:

1. PT100
2. PT200
3. PT500
4. PT1000
5. PT2000

Constant current supply (mA):

Enter the excitation current of the RTD in milliamperes.

Use input pin Is for current excitation:

Select this if the excitation current to the RTD is to be determined at the input pin Is in Amperes.

Sensor connection:

Select the type of connection to the sensor. The choices are:

1. 2 wire
2. 3 wire
3. 4 wire

Sensor wires length (m / wire):

Enter the length of each wire to the RTD in meters.

Sensor wires cross-sectional area (mm^2):

Enter the cross-sectional area of the wires connected to the sensor.

Sensor wire temperature different to the sensor temperature:

Enter the

Sensor wire temperature (°C):

Enter the

Thermal resistance for self-heating effect (°C/W):

Enter the

Contents - Simulation

Filters

The filters in the digital power block vary from sensing circuit type hardware filters, to power circuit filters to filters which can be implemented in software. The filters selected are typically used in digital power applications.



Anti-aliasing filter

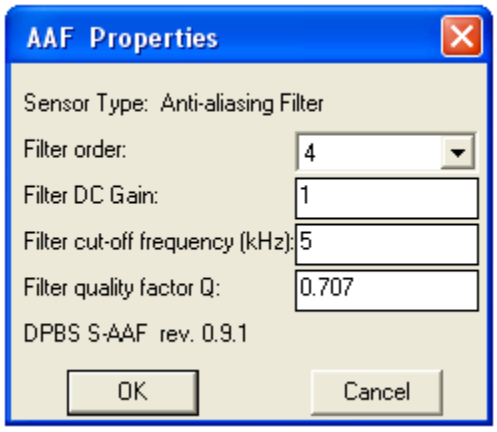
The anti-aliasing filter block is intended to model a hardware pre-filter before connecting to an ADC block. The details of aliasing are out of the scope of this document and can be found throughout the literature. The filter here is a low pass filter of 1 to 4 orders with a programmable quality factor.

Input Pins: **Vin** Input voltage (V).

Output Pins: **Vo** Filter output voltage (V)

Dialog properties:

The anti-aliasing filter block properties menu is shown in the following box which appears when right-clicking on the block.



Filter order:

Select the required filter order

Filter DC gain:

Enter the required filter DC / low frequency gain.

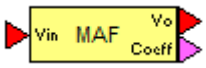
Filter cut-off frequency:

Enter the desired cut-off frequency of the low-pass filter.

Filter quality factor:

For filters of order 2 or higher, the quality factor can be set.

Contents - Simulation



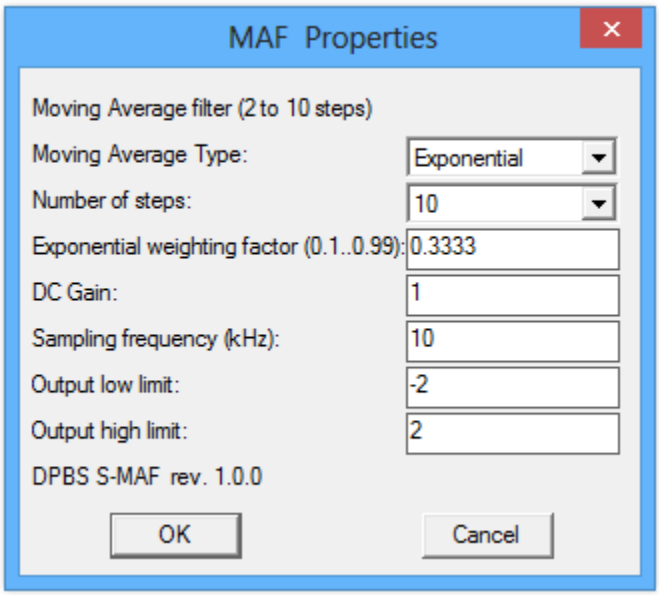
Moving average filter

The moving average filter is a filter applied to firmware and does not have a hardware equivalent. It would then normally be placed in a simulation after an ADC to simulate a digital control algorithm to be interfaced with the hardware component models. Three types of moving average can be emulated with this block from 2 to 10 steps. The output is updated at each sample determined by the sampling frequency, each sample being pushed through the filter similar to a FIFO; the newest sample having the highest weighting and the oldest sample being pushed out of the window.

Input Pins:	**Vin**	Input voltage (V).
Output Pins:	**Vo**	Filter output voltage (V)
	Coeff	Display of the filter coefficients (struct).

Dialog properties:

The moving average filter block properties menu is shown in the following box which appears when right-clicking on the block.



Moving average type:

The choices here are:

1. simple (each step has equal weighting)
2. linearly weighted (each past time step has an equal, decreasing difference in weighting)
3. exponential (each past time step is weighted in an exponentially decreasing rate)

Number of steps:

From 2 to 10 steps may be selected.

Exponential weighting factor:

Enter a value from 0.1 to 0.99 which will correspond to the weighting of the most recent step (sample); the remaining coefficients will be correspondingly exponentially weighted. This value is only relevant if an exponentially weighted filter is selected.

DC gain:

A gain coefficient will be determined in order to set the required DC filter gain.

Sampling frequency:

Enter the required sampling frequency in kHz. The coefficients are not dependent upon the sampling frequency.

Output high / low limit:

Enter the output high and low limits of the filter.

Contents - Simulation



Second-order Filter

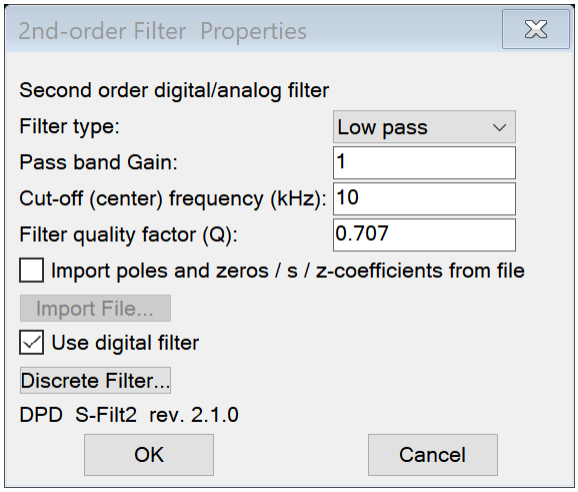
The second order filter emulates either a filter implemented in hardware or in software. It is a generalised filter based on the cut-off frequency and quality factor only. For further implementation options, one should use the transfer function block within the Embed basic block set.

For higher order filters, one can connect filter blocks in series.

Input Pins:	**Vi(t)**	Input signal, usually a voltage.
	Sin	Optional input pin to sample the filter (if enabled and if a discrete filter is selected).
	F(Hz)	Frequency input (optional) for frequency response analysis.
Output Pins:	**Vo(t)**	Filtered output, depending upon the input and filter type.
	So	Optional output pin to further sample components in a diagram after the internal computational delay.
	G(s)	Output frequency response (if a frequency input is present).

Dialog properties:

The 2nd order filter properties menu is shown in the following box which appears when right-clicking on the block



Filter type:

The choices are:

1. Low-pass
2. High-pass
3. Band-pass
4. Band-reject
5. All-pass

Pass band gain:

Enter the pass-band gain K in V/V.

Cut-off (center) frequency:

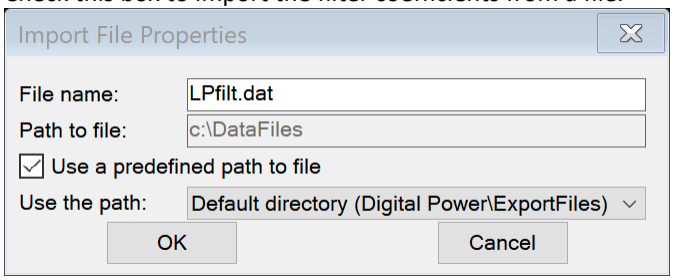
Enter the desired cut-off frequency (center frequency for band-pass and band-reject filters) in kilohertz ($\omega_o/2\pi$).

Filter Quality Factor:

Enter the desired quality factor Q of the second order filter.

Import poles and zeros / s / z-coefficients from file:

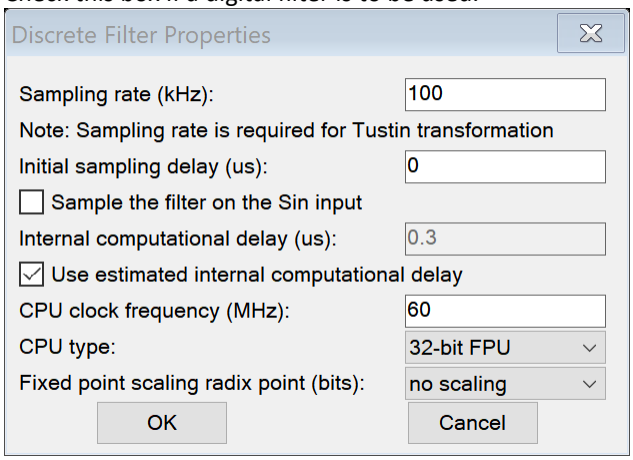
Check this box to import the filter coefficients from a file.



The file name should be given and the path to the file selected.
The type of coefficients will be automatically detected.

Use digital filter:

Check this box if a digital filter is to be used.



Sampling rate:

Enter the sampling frequency in kHz of the digital filter.

NOTE: If an external file is used for the discrete coefficients, the sampling rate used to generate those coefficients must be equal to the value entered here. The discrete filter coefficients will be generated for the entered sample rate using the Tustin transformation. For this reason, the sample rate is necessary even if the filter is sampled at the Sin input pin. If the sample rate at the Sin input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (if any prior process is to be computed). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the Sin input pin:

When enabled, the filter will be sampled on the rising edge of the Sin input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the filter internal computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz required to calculate the internal computational delay.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16.bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

The characteristic equation and the coefficients currently in use (during a simulation run) is displayed inside the block.

Transfer functions

The second order filters have the transfer functions:

Low-pass Filter.

$$H_{LP}(s) = K \cdot \frac{(\omega_0)^2}{s^2 + \frac{\omega_0}{Q} \cdot s + (\omega_0)^2}$$

High-pass filter:

$$H_{HP}(s) = K \cdot \frac{s^2}{s^2 + \frac{\omega_0}{Q} \cdot s + (\omega_0)^2}$$

Band-pass filter:

$$H_{BP}(s) = K \cdot \frac{\frac{\omega_0}{Q} \cdot s}{s^2 + \frac{\omega_0}{Q} \cdot s + (\omega_0)^2}$$

Band-reject filter:

$$H_{BR}(s) = K \cdot \frac{s^2 + (\omega_0)^2}{s^2 + \frac{\omega_0}{Q} \cdot s + (\omega_0)^2}$$

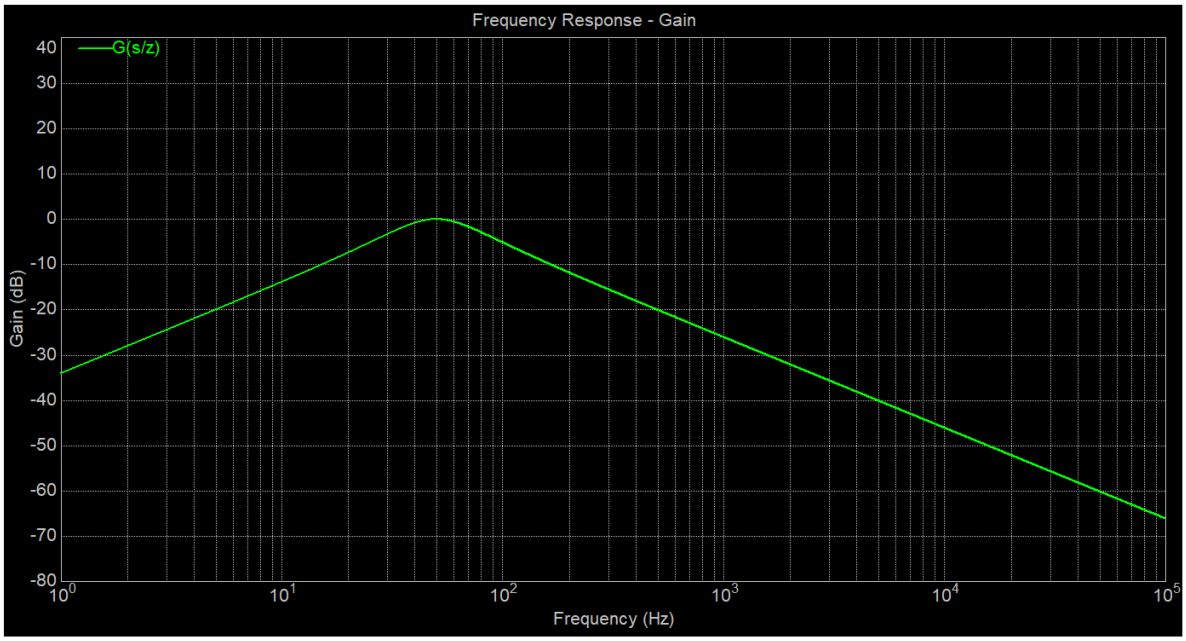
All-pass filter:

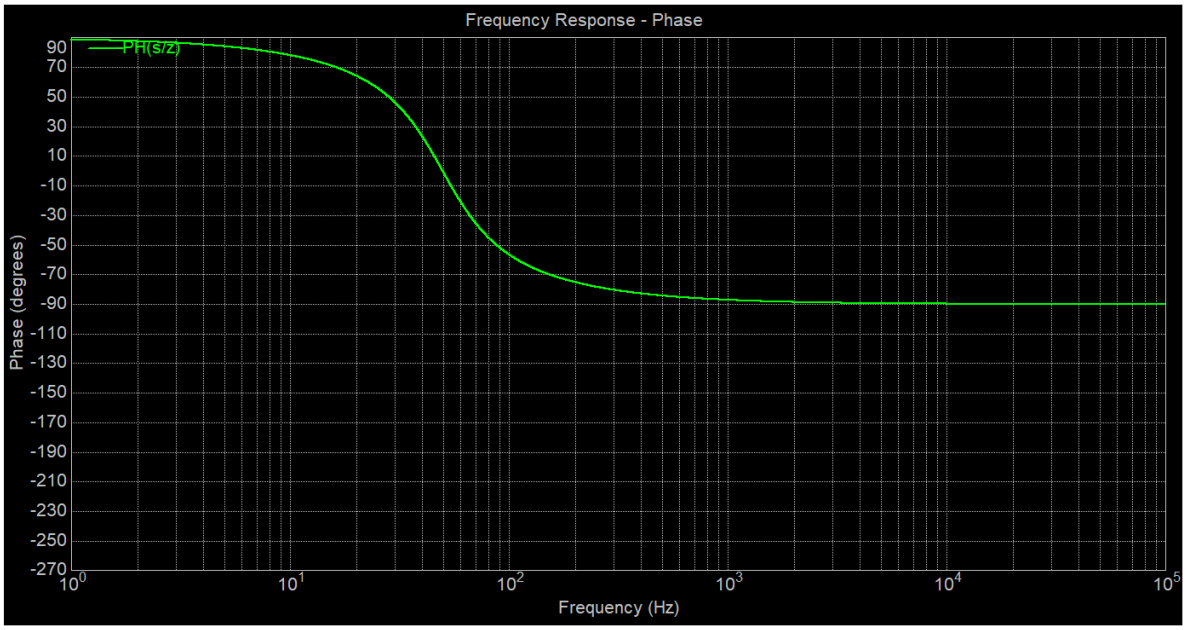
$$H_{AP}(s) = K \cdot \frac{s^2 - \frac{\omega_0}{Q} \cdot s + (\omega_0)^2}{s^2 + \frac{\omega_0}{Q} \cdot s + (\omega_0)^2}$$

The filters, when realized as digital filters (converted internally in the block using the bi-linear or Tustin transform), have the form:

$$H_F(z) = K_z \cdot \frac{z^2 + B_1 \cdot z + B_0}{z^2 + A_1 \cdot z + A_0}$$

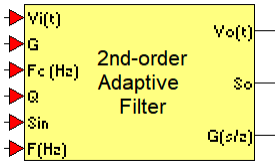
Second-order Filter





The frequency response of the second order filter can be viewed internally within the block. A model-based frequency response analysis block is required in the diagram in order to generate the frequency response.

Contents - Simulation



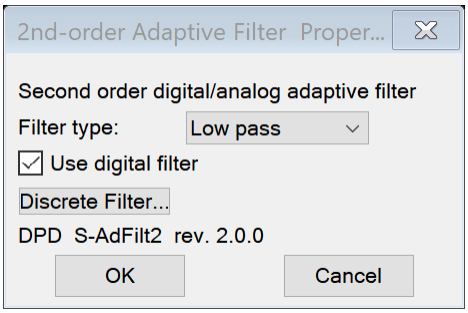
Second-order Adaptive Filter

The second order adaptive filter is based upon the second order filter block except that in this case, the filter parameters are determined at the input pins. This means that the filter parameters can be changed during a simulation and the filter response adapted as necessary.

Input Pins:	**Vi(t)**	Input signal, usually a voltage.
	G	Filter gain input.
	Fc	Cut-off (center) frequency input in Hz.
	Q	Quality factor input.
	Sin	Optional input pin to sample the filter (if enabled and if a discrete filter is selected).
	F(Hz)	Frequency input (optional) for frequency response analysis.
Output Pins:	**Vo(t)**	Filtered output, depending upon the input and filter type.
	So	Optional output pin to further sample components in a diagram after the internal computational delay.
	G(s)	Output frequency response (if a frequency input is present).

Dialog properties:

The 2nd order adaptive filter properties menu is shown in the following box which appears when right-clicking on the block

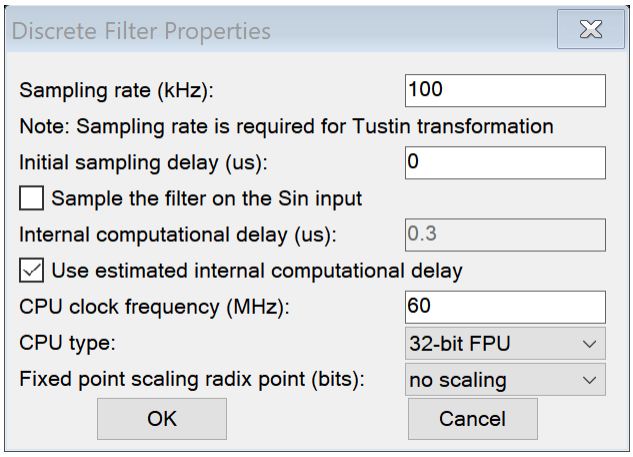


The dialog is similar to the second order filter except that the filter parameters are not input in the dialog.
Again, the types of second-order adaptive filters which can be modelled with this block are:

1. Low-pass
2. High-pass
3. Band-pass
4. Band-reject
5. All-pass

Use Digital Filter:

Select this if a digitally sampled filter is required. The following dialog will become available:



Sampling rate:

Enter the sampling frequency in kHz of the adaptive digital filter.

NOTE: If an external file is used for the discrete coefficients, the sampling rate used to generate those coefficients must be equal to the value entered here. The discrete filter coefficients will be generated for the entered sample rate using the Tustin transformation. For this reason, the sample rate is necessary even if the filter is sampled at the Sin input pin. If the sample rate at the Sin input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (if any prior process is computed). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the Sin input pin:

When enabled, the filter will be sampled on the rising edge of the Sin input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the filter internal computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz required to calculate the internal computational delay.

CPU type:

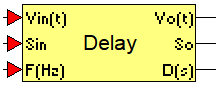
Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16.bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.



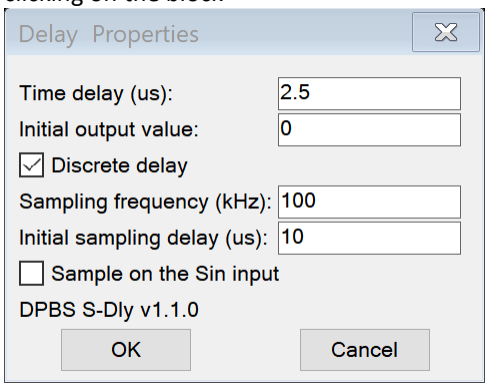
Delay

The delay block models a time delay in continuous time, discrete sampled time and in the frequency domain.

Input Pins:	**Vin(t)**	Input signal, usually a voltage.
	Sin	Optional input pin to sample the delay block (if enabled and if a discrete delay).
	F(Hz)	Frequency input to the delay block for frequency response analysis.
Output Pins:	**Vo(t)**	Delayed output signal.
	So	Optional output pin for further sequential sampling after the delay.
	D(s)	Frequency response output.

Dialog properties:

The delay properties menu is shown in the following box which appears when right-clicking on the block



Time Delay:

Enter the required time delay in micro-seconds.

Initial output value:

Enter the initial output value at the Vo(t) pin.

Discrete sampling:

Select for a discretely sampled delay stage

Sampling frequency:

Enter the sampling frequency in kHz.

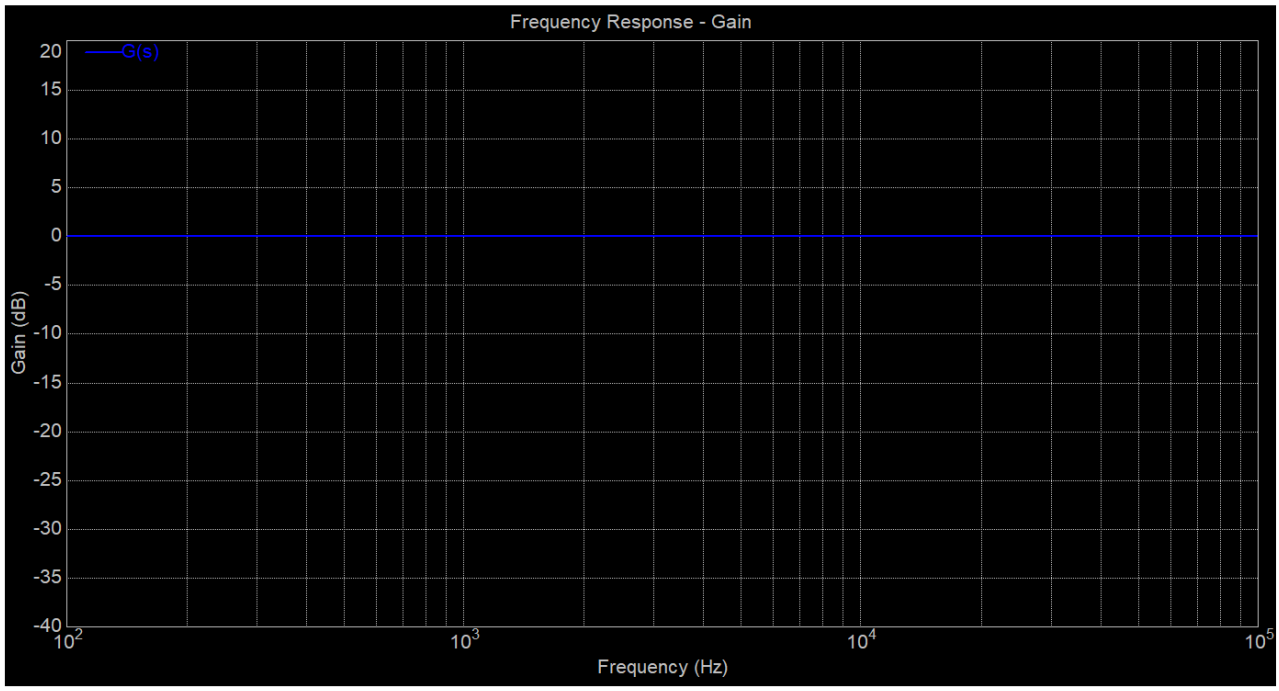
Initial Sampling Delay:

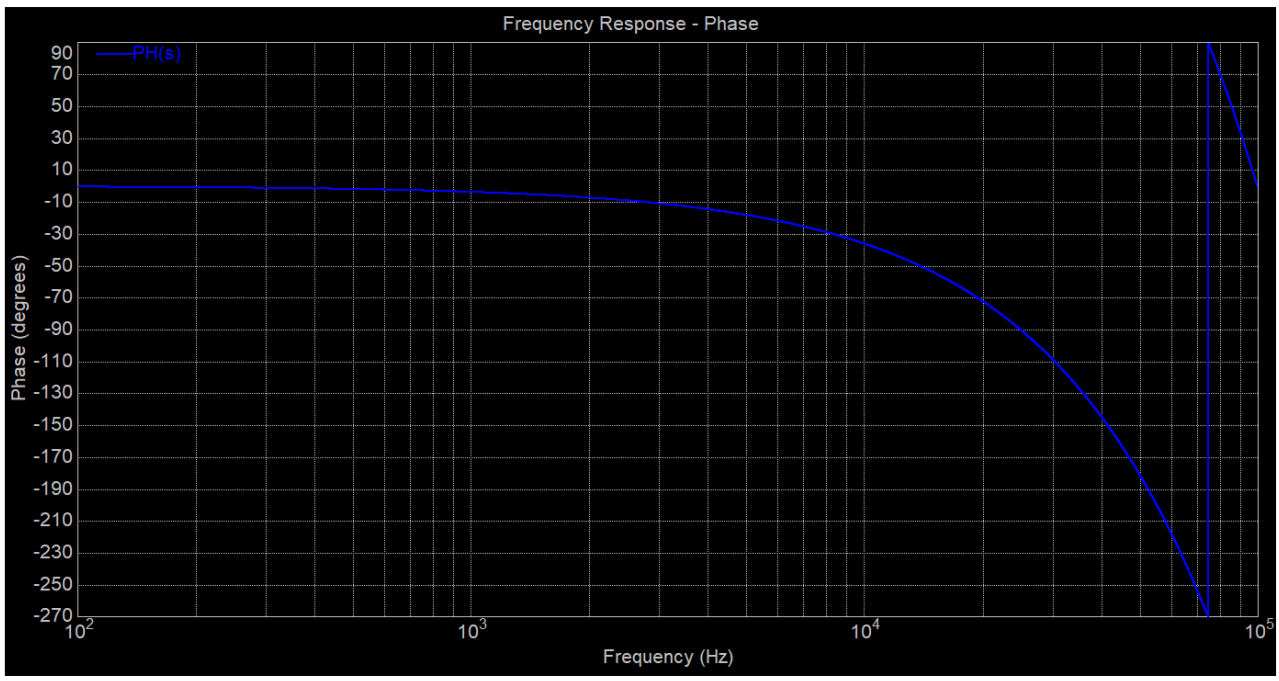
Enter the required initial delay before sampling starts.

Sample on the Sin input:

Select this option if the delay is to be digitally sampled on the rising edge of the input pin Sin.

Time Delay





The frequency response of the delay and gain blocks can be viewed internally within the block. A model-based frequency response analysis block is required in the diagram in order to generate the frequency response.



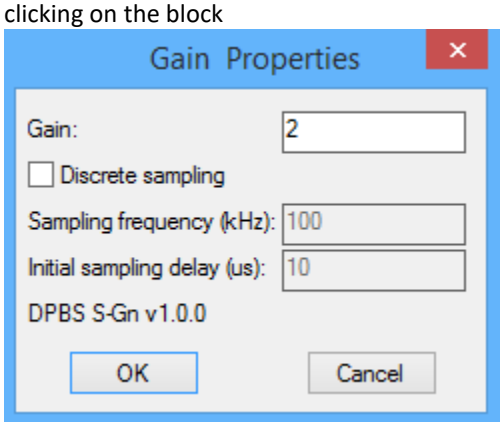
Gain

The gain block models gain in continuous time, discrete sampled time and in the frequency domain.

Input Pins:	**Vin(t)**	Input signal, usually a voltage.
	F(Hz)	Frequency input to the delay block for frequency response analysis.
Output Pins:	**Vo(t)**	Output signal multiplied by the gain.
	D(s)	Frequency response output.

Dialog properties:

The gain properties menu is shown in the following box which appears when right-clicking on the block



Gain:

Enter the required gain.

Discrete sampling:

Select for a discretely sampled gain stage

Sampling frequency:

Enter the sampling frequency in kHz.

Initial Sampling Delay:

Enter the required initial delay before sampling starts.



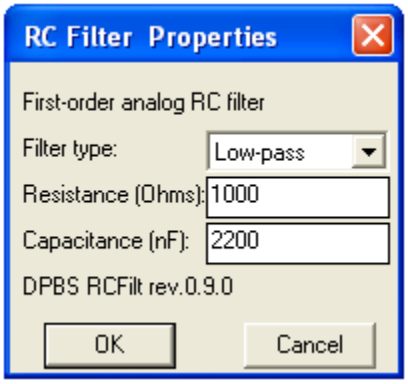
RC Filter

The RC filter emulates a first order hardware filter using a single resistor and a single capacitor. This filter is intended for use as a sense filter on any sensing circuits but can be applied as a general first order filter.

Input pin:	**Vi**	Unfiltered input voltage (V).
	F(Hz)	Frequency input (optional) for frequency response analysis.
Output Pin:	**Vo**	Filtered output voltage (V).
	G(s)	Output frequency response (if a frequency input is present).

Dialog properties:

The RC filter properties menu is shown in the following box which appears when right-clicking on the block



Filter type:

The choices are:

1. Low-pass
2. High-pass

Resistance:

Enter the series (low-pass) or parallel (high-pass) resistance value in Ohms.

Capacitance:

Enter the filter capacitance value in nano-Farads.

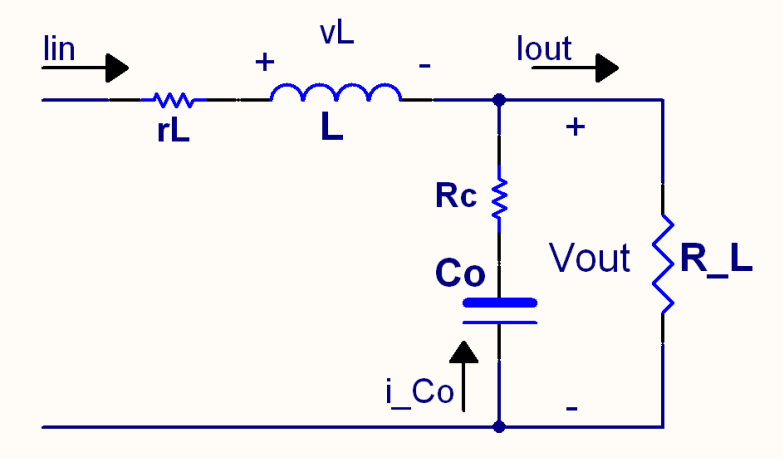
Contents - Simulation



Power LC Filter

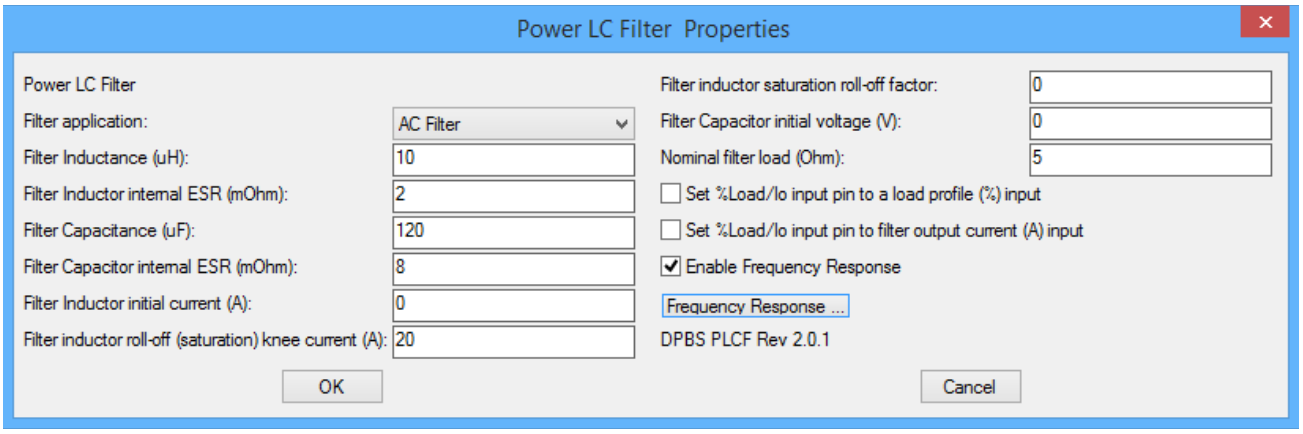
The power LC filter is a second order hardware filter using an inductor and a capacitor. This filter is intended for use in the power stage of circuits and not as a sensing filter. The filter can be applied as a converter input or output filter. If damping is required, the internal inductor and / or capacitor resistances can be increased to emulate series resistances. The filter can be applied with DC or AC voltages.

Input Pins:	**Vin**	Unfiltered input voltage (V).
	%Load/Io	Input which can be selected as a percentage load input or as the filter load current input.
	F(Hz)	Frequency input (optional) for frequency response analysis.
Output pins:	**Vo**	Filtered output voltage (V).
	Io	Filtered output current (A).
	Iin	Unfiltered input current (A).
	vL	The voltage across the filter inductor (V).
	iC	The current in the filter capacitance (A).
	G(s)	Output frequency response if used.
Circuit schematic:		Power LC filter (AC Filter).



Dialog properties:

The power LC filter properties menu is shown in the following box which appears when right-clicking on the block



Filter application:

The choices here are:

1. DC Filter (non-regenerative)
2. DC Filter (regenerative)
3. AC Filter

For a non-regenerative filter it is intended that the filter inductor current cannot go negative and therefore cannot return power to the source. Such a supply source would be an AC-DC diode rectifier or a DC-DC converter with a blocking diode.

Filter inductance (uH):

Enter the filter inductance in micro-henrys.

Filter inductor internal ESR (mOhm):

Enter the value of the internal inductor resistance in milli-ohms.

Filter capacitance (uF):

Enter the filter capacitance in micro-farads.

Filter capacitor internal ESR (mOhm):

Enter the value of the internal capacitor resistance (ESR) in milli-ohms.

Filter inductor initial current (A):

Enter the initial current (at simulation start) of the filter inductor in amps.

Filter capacitor initial voltage (V):

Enter the initial voltage (at simulation start) of the filter capacitor in volts.

Nominal filter load (Ohm):

Enter the nominal load on the filter in Ohms.

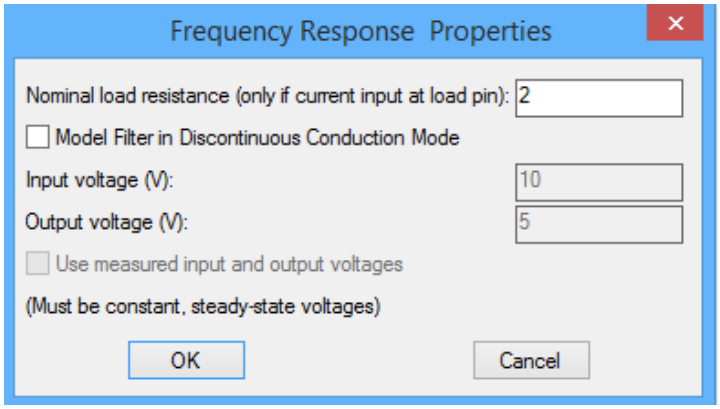
Set %Load/Io input pin to a load profile (%) input:

Set the input pin as a load profile control as a percent of the nominal load.

Set %Load/Io input pin to a filter output current input:

In this case the nominal load is ignored and the filter is directly loaded by this pin, determining its output current.

Frequency Response:

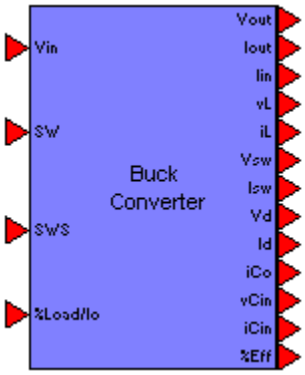


The frequency response dialog assists in the set-up of the LC Filter frequency response calculation.

Contents - Simulation

Power Converter Blocks (DC-DC)

The power converter blocks model various power converters as switching models.



Buck Converter

The buck converter is, in its basic form, a second order converter with a positive output for a positive input (non-inverting). It is a step-down converter because the output voltage is always lower than the input voltage.

Input Pins:	**Vin**	Input voltage (V). This is usually connected from a source block or it can be the output of another converter.
	SW	Main switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	SWS	Synchronous switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V).
	Iout	Converter output current (A).
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered switch current for the case of the buck converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vL	Voltage across the inductor (V)
	iL	Current flowing through the inductor (A)
	Vsw	Switch Voltage (V) – Positive for forward voltages.
	Isw	Switch Current (A) – Positive for forward current.
	Vd	Diode Voltage (V) - Positive for reverse voltages. The voltage across the re-circulating diode / synchronous switch.
	Id	Diode Current (A) – Positive for forward current. The current through the re-circulating diode / synchronous switch.
	iCo	Output Capacitor Current (A)

vCin Input capacitor Voltage (V)

This will be the voltage charge on input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.

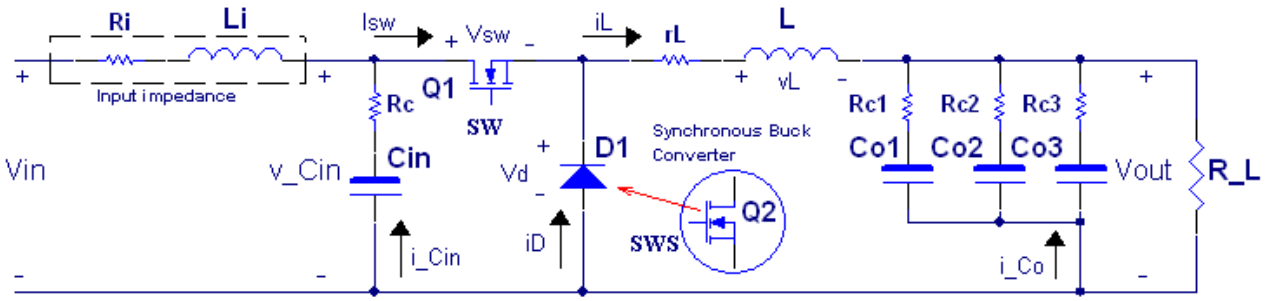
iCin Input capacitor current (A)

%Eff Converter Efficiency (%), averaged over a switching cycle.

The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switch and diode / synchronous switch conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR).

The switching losses and diode reverse recovery losses along with the inductor core losses are not included in the model.

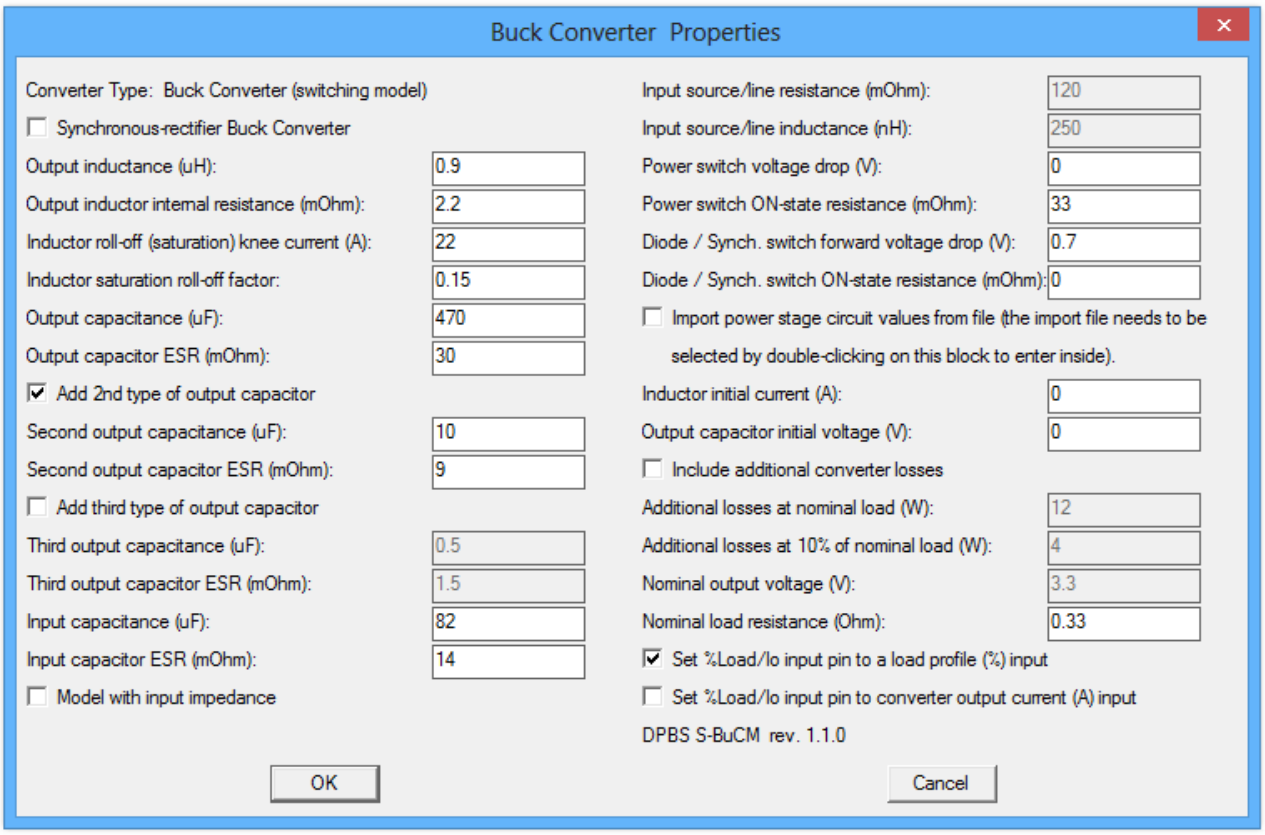
Circuit schematic: Buck Converter.



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. Refer to below.

Dialog properties:

The buck converter properties menu is shown in the following box which appears when right-clicking on the buck converter block.



Synchronous-rectifier Buck Converter:

When this check box is activated the output diode of the buck converter will be modelled as a controllable switch (usually a MOSFET). This will activate the SWS input pin.

Output inductance:

Insert the value of the buck converter output inductance in micro-Henrys.

Output inductor internal resistance:

The winding resistance of the buck inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if "Model with input impedance" is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to model the buck converter with input impedance. This can also be used to model the effects of an input filter on the buck converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switch voltage drop:

The forward voltage drop, in Volts, across the main switch of the buck converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch. For a synchronous converter, if the current through the inductor is negative and both the switches are in the OFF state, this value will be used as the forward voltage drop of the integrated reverse diode of the main switch.

Power switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diode / Synch. Switch forward voltage drop:

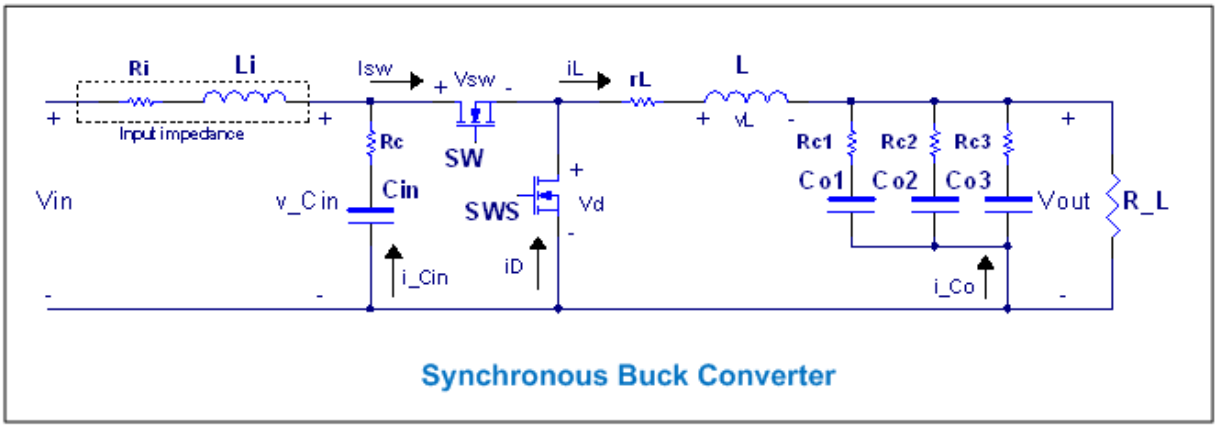
The forward voltage drop, in Volts, across the diode / synchronous switch (in the case of a synchronous-rectifier converter) of the buck converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

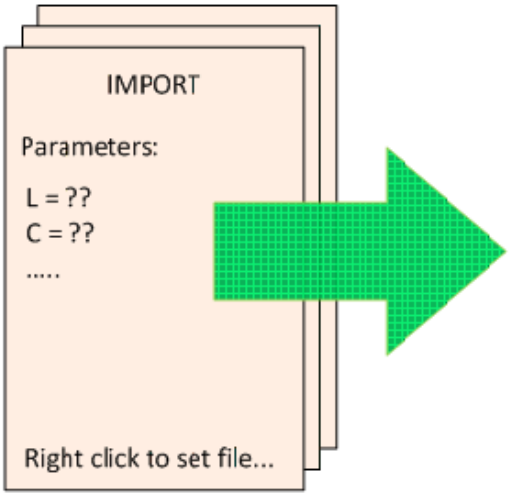
Diode / Synch. Switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file.
The file can be entered and viewed by double-left clicking on the main block:



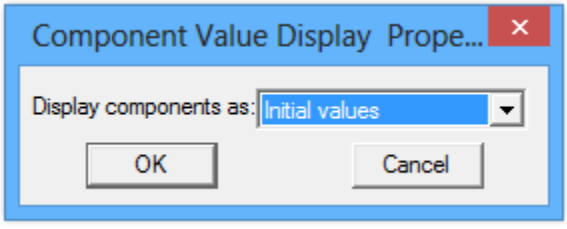


Component Value Display

Component	Value
File	Dialog values
Ri (mOhm)	N/A
Li (uH)	N/A
Cin (uF)	82.0000
Rc (mOhm)	14.0000
Co1 (uF)	470.0000
Rc1 (mOhm)	30.0000
Co2 (uF)	10
Rc2 (mOhm)	9
Co3 (uF)	N/A
Rc3 (mOhm)	N/A
L (uH)	.9000
rL (mOhm)	2.2000
VswON (V)	.0000
RswON (mOhm)	33.0000
VdON (V)	.7000
RdON (mOhm)	20.0000
R_L (Ohm)	.3300

The circuit schematic and the corresponding components currently in use (during a simulation run) is dispalyed and the import file can be set-up by right clicking on the import image.

The component values displayed can be configured by right-clicking on the Component Value Display box.



The choices are:

1. Initial values
2. Time-varying values

Initial inductor current:

The initial inductor current (at simulation start) can be entered here in Amperes.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

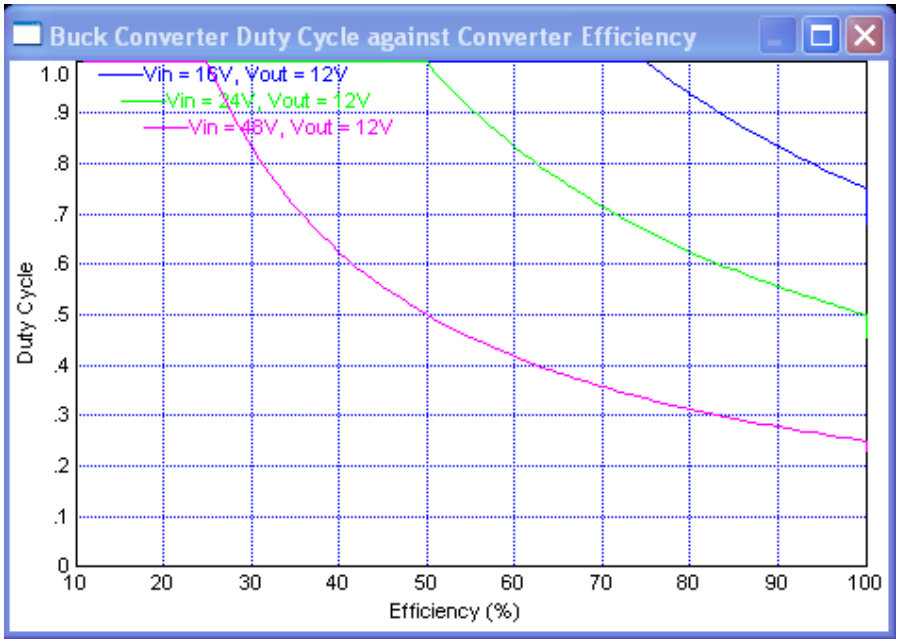
Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Since the converter duty cycle is inversely proportional to the efficiency as:

$$D = \frac{Vo}{\eta \cdot Vi} \qquad Vi > Vo \qquad \text{(Buck converter, in CCM)}$$

the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced when this box is checked.

The figure below shows the variation of duty cycle against efficiency in Continuous Current Mode (CCM) for different input to output voltage ratios.



Additional losses at nominal load:

Insert the additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load.

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses included in the model in this case will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

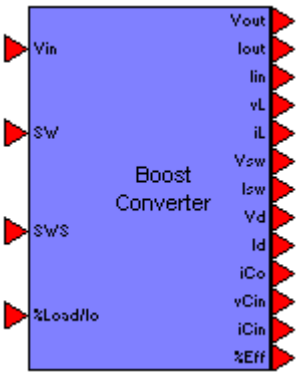
Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

Contents - Simulation



Boost Converter

The boost converter is, in its basic form, a second order converter with a non-inverting output. It is a step-up converter because the output voltage is always higher than the input voltage when switching.

Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW	Main switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	SWS	Synchronous switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V)
	Iout	Converter output current (A)
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered inductor current for the case of the boost converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vL	Voltage across the inductor (V)
	iL	Current flowing through the inductor (A)
	Vsw	Switch Voltage (V) – Positive for forward voltages.
	Isw	Switch Current (A) – Positive for forward current.

Vd Diode Voltage (V) - Positive for reverse voltages.

The voltage across the output diode / synchronous switch.

Id Diode Current (A) – Positive for forward current.

The current through the output diode / synchronous switch.

iCo Output Capacitor Current (A)

vCin Input capacitor Voltage (V)

This will be the voltage charge on input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.

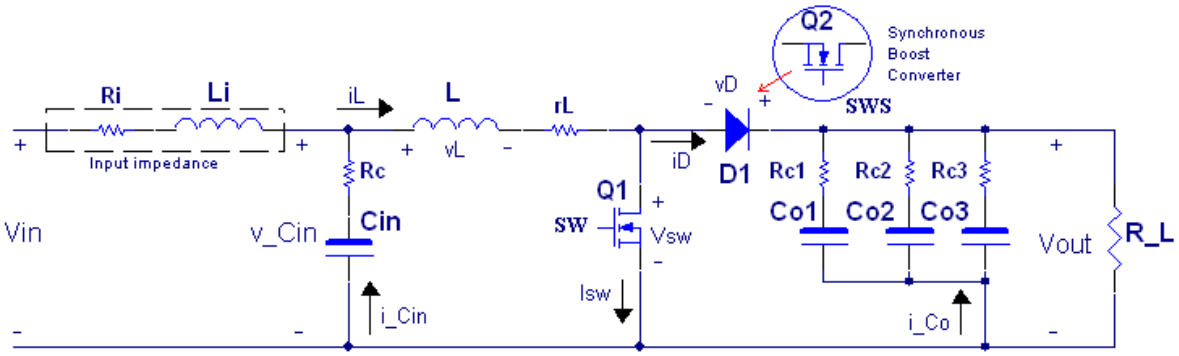
iCin Input capacitor current (A)

%Eff Converter Efficiency (%), averaged over a switching cycle.

The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switch and diode / synchronous switch conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR).

The switching losses and diode reverse recovery losses along with the inductor core losses are not included in the model.

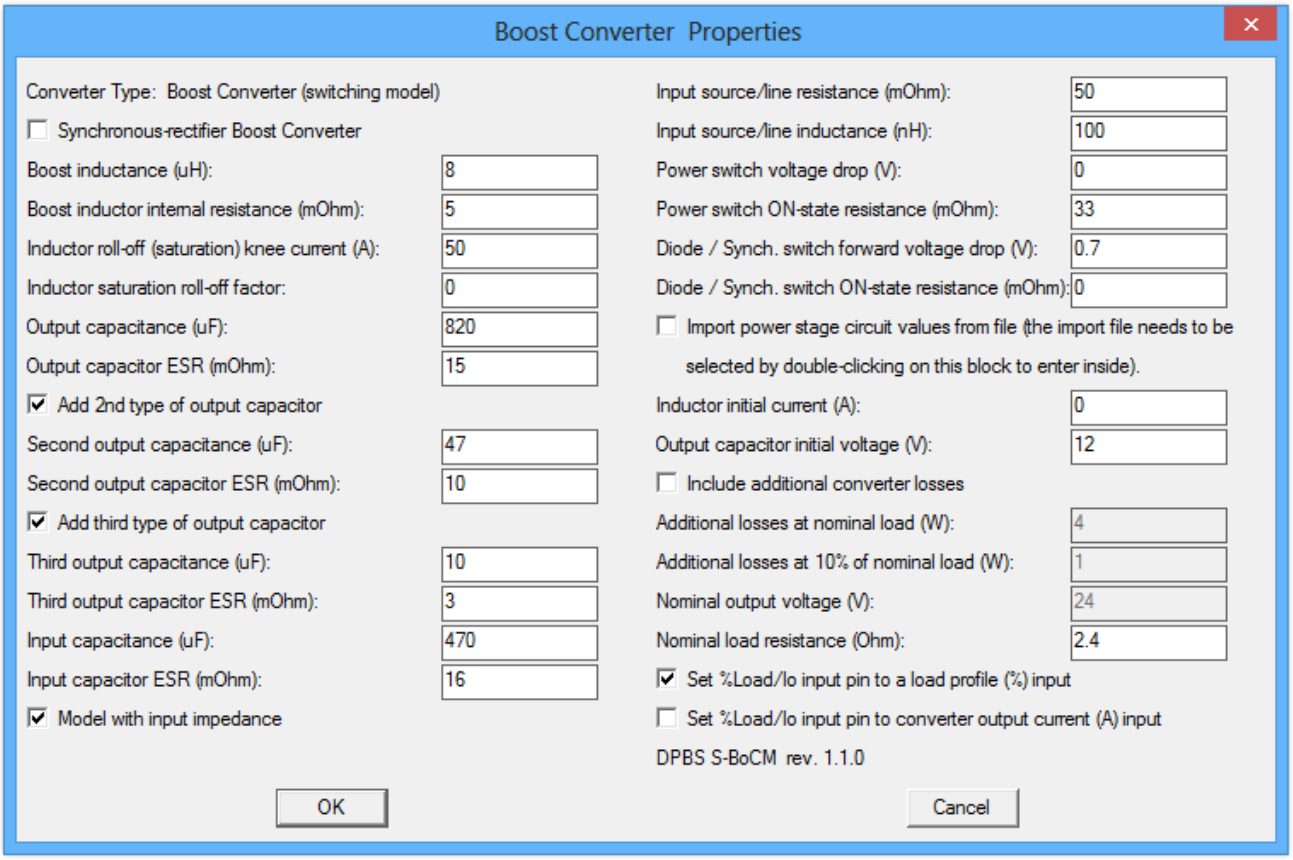
Circuit schematic: Boost Converter



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The boost converter properties menu is shown in the following box which appears when right-clicking on the boost converter block.



Synchronous-rectifier Boost Converter:

When this check box is activated the output diode of the boost converter will be modelled as a controllable switch (usually a MOSFET). This will activate the SWS input pin.

Input inductance:

Insert the value of the boost converter input inductance in micro-Henrys.

Input inductor internal resistance:

The winding resistance of the boost inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if "Model with input impedance" is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to include the input impedance in the boost converter model. This can also be used to model the effects of an input filter in the boost converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switch voltage drop:

The forward voltage drop, in Volts, across the main switch of the boost converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch. For a synchronous converter, if the current through the inductor is negative and both the switches are in the OFF state, this value will be used as the forward voltage drop of the integrated reverse diode of the main switch.

Power switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diode / Synch. Switch forward voltage drop:

The forward voltage drop, in Volts, across the diode / synchronous switch (in the case of a synchronous-rectifier converter) of the boost converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

Diode / Synch. Switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file. This file is typically generated by the Power Stage Design Tool within the Digital Power Design Suite.

The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Initial inductor current:

The initial inductor current (at simulation start) can be entered here in Amperes.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

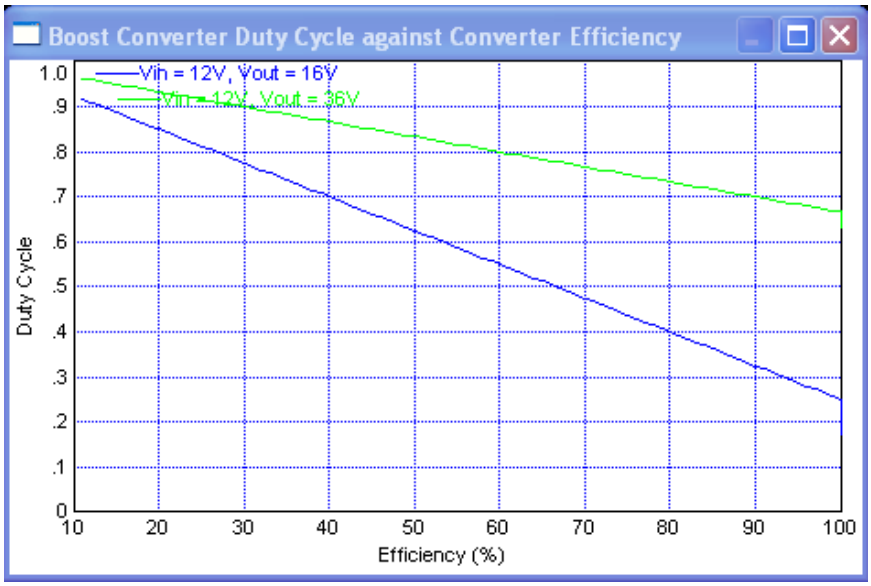
Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Since the converter duty cycle is a function of the efficiency as:

$$D = \frac{Vo - \eta \cdot Vi}{Vo} \qquad Vi < Vo \qquad \text{(Boost converter in CCM)}$$

the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced .

The figure below shows the variation of duty cycle against efficiency in CCM for two different input to output voltage ratios.



Additional losses at nominal load:

Insert the required additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load..

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

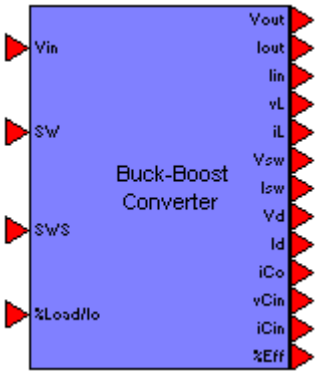
Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

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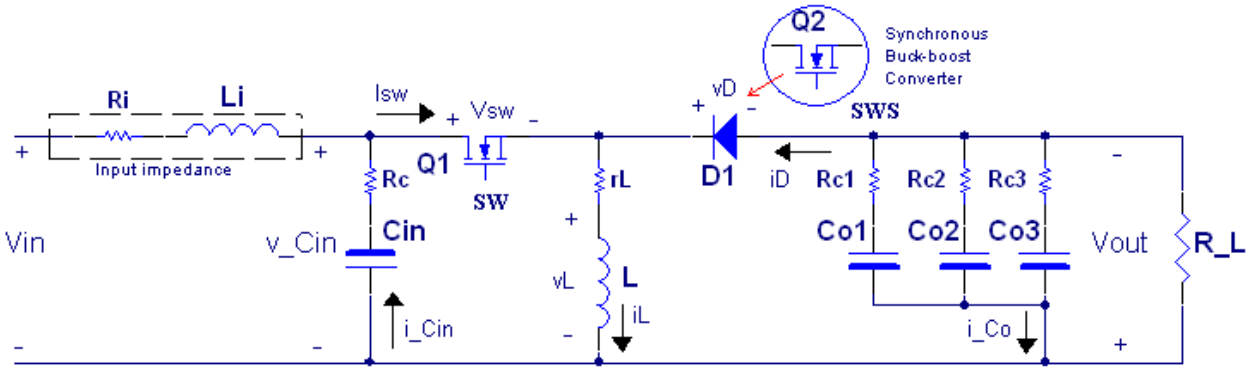
Buck-boost Converter

The buck-boost converter is, in its basic form, a second order converter with an inverting output. This converter accepts a positive input voltage and produces a negative output voltage. It is a step-up / step-down converter and the absolute value of the output voltage can be higher or lower than (or equal to) the input voltage.

Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW	Main switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	SWS	Synchronous switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V). Since the buck-boost converter is an inverting configuration, the voltage will be negative.
	Iout	Converter output current (A), again the output current is negative.
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered switch current for the case of the buck-boost converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vL	Voltage across the inductor (V)

iL	Current flowing through the inductor (A)
Vsw	Switch Voltage (V) – Positive for forward voltages.
Isw	Switch Current (A) – Positive for forward current.
Vd	Diode Voltage (V) - Positive for reverse voltages. The voltage across the buck-boost output diode / synchronous switch.
Id	Diode Current (A) – Positive for forward current. The current through the buck-boost output diode / synchronous switch.
iCo	Output Capacitor Current (A)
vCin	Input capacitor Voltage (V) This will be the voltage charge on input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.
iCin	Input capacitor current (A)
%Eff	Converter Efficiency (%), averaged over a switching cycle. The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switch and diode / synchronous switch conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR). The switching losses and diode reverse recovery losses along with the inductor core losses are not included in the model.

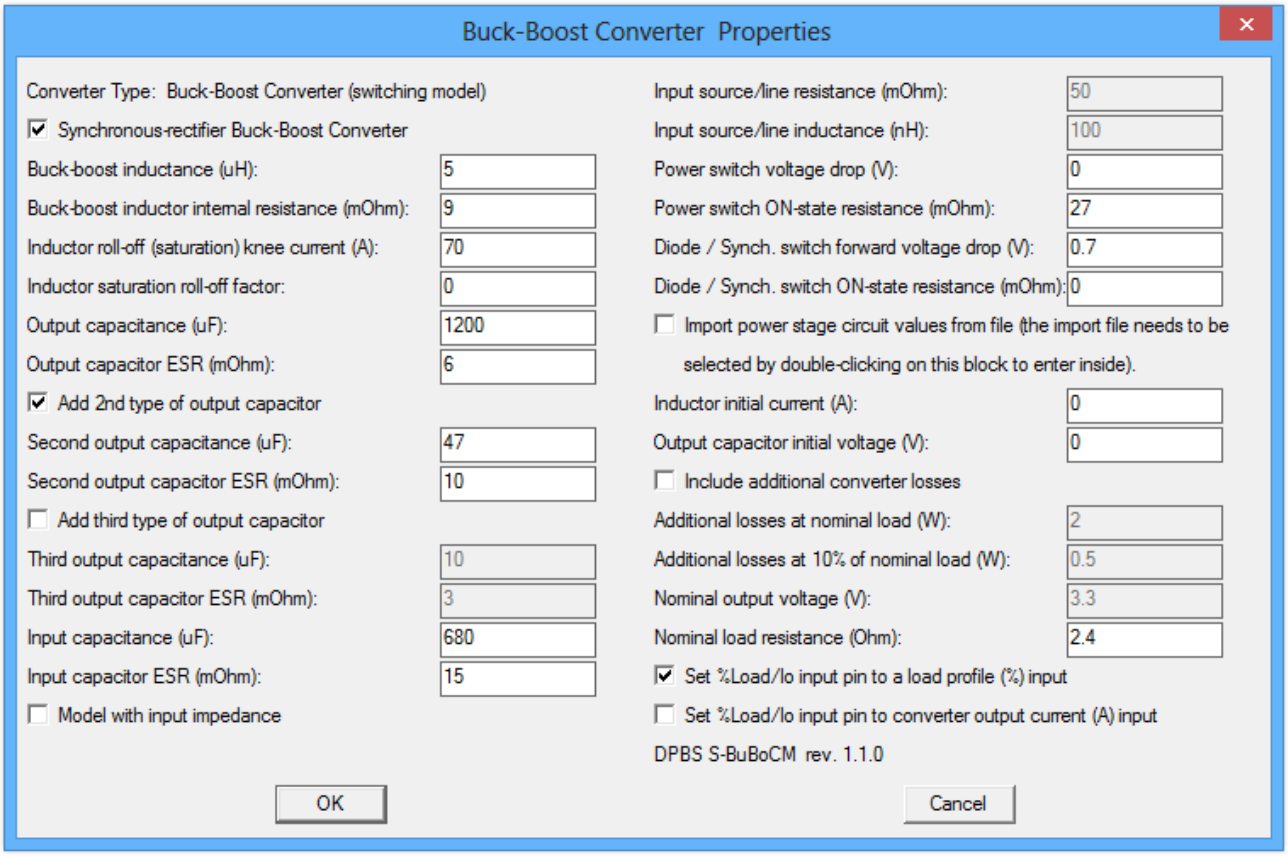
Circuit schematic: Buck-boost Converter



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The buck-boost converter properties menu is shown in the following box which appears when right-clicking on the buck-boost converter block.



Synchronous-rectifier Buck-boost Converter:

When this check box is activated the output diode of the buck-boost converter will be modelled as a controllable switch (usually a MOSFET). This will activate the SWS input pin.

Input inductance:

Insert the value of the buck-boost converter input inductance in micro-Henrys.

Output inductor internal resistance:

The winding resistance of the buck-boost inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the current flowing through the inductor.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if "Model with input impedance" is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to include the input impedance in the buck-boost converter model. This can also be used to model the effects of an input filter in the buck-boost converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switch voltage drop:

The forward voltage drop, in Volts, across the main switch of the buck-boost converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch. For a synchronous converter, if the current through the inductor is negative and both the switches are in the OFF state, this value will be used as the forward voltage drop of the integrated reverse diode of the main switch.

Power switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diode / Synch. Switch forward voltage drop:

The forward voltage drop, in Volts, across the diode / synchronous switch (in the case of a synchronous-rectifier converter) of the buck-boost converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

Diode / Synch. Switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file. This file is typically generated by the Power Stage Design Tool within the Digital Power Designer Suite. The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Initial inductor current:

The initial inductor current (at simulation start) can be entered here in Amperes.

Output capacitor initial voltage:

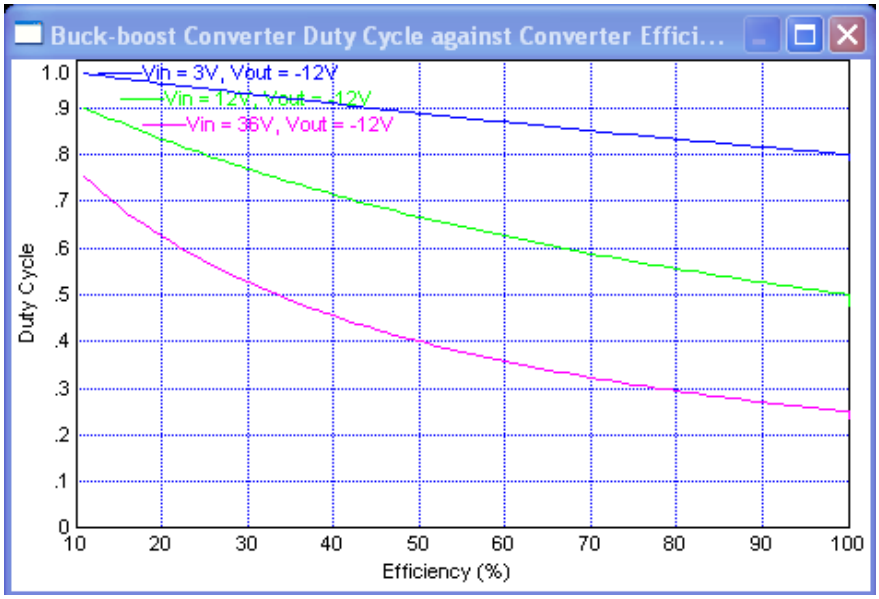
The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Since the converter duty cycle is a function of the efficiency as:

$$D = \frac{Vo}{\eta \cdot Vi + Vo}$$ (Buck-boost converter in CCM)

the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced . The figure below shows the variation of duty cycle against efficiency in CCM for different input to output voltage ratios for the buck-boost converter.



Additional losses at nominal load:

Insert the required additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load..

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

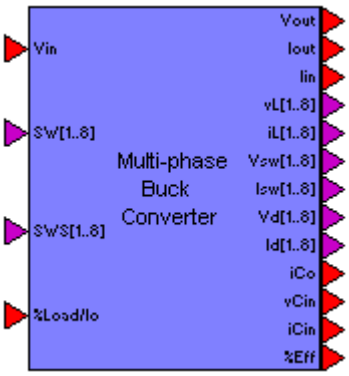
Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

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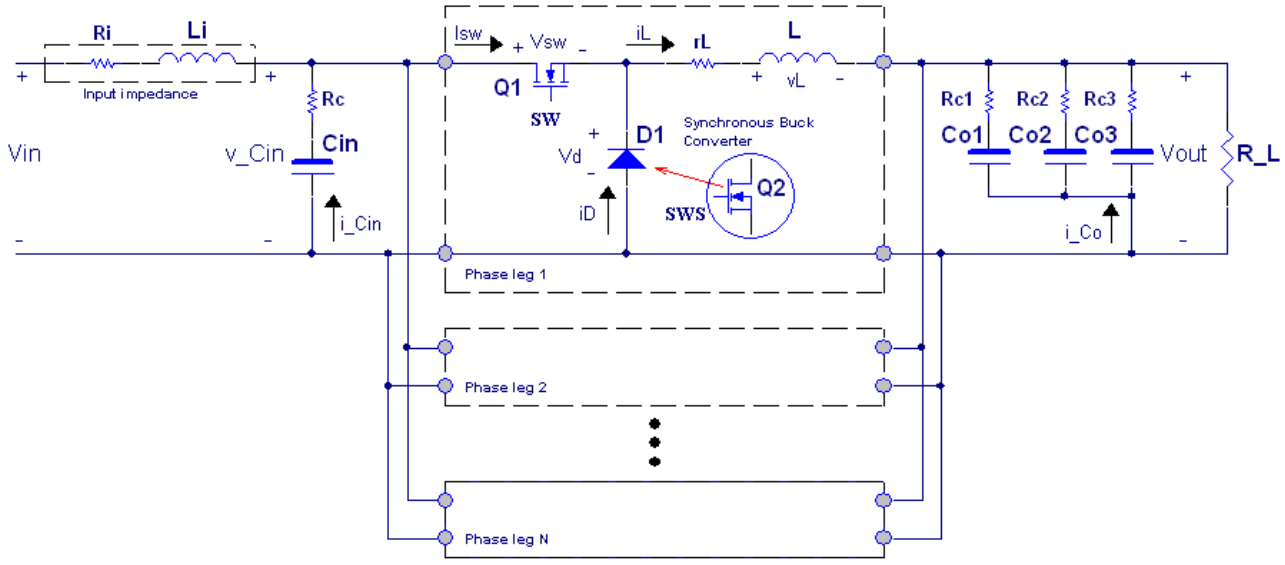
Multi-phase Buck Converter

The multi-phase buck converter is an 8 leg buck converter with a common input and output capacitor.

Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW[1..8]	Main switches control (SW < 1 = OFF, SW ≥ 1 = ON) – vector; rows = 1, columns = 8.
	SWS[1..8]	Synchronous switches control (SW < 1 = OFF, SW ≥ 1 = ON) – vector; rows = 1, columns = 8.
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V).
	Iout	Converter output current (A).
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered switch current for the case of the buck converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.

vL[1..8]	Voltage across the inductors – vector rows = 1, columns = 8 (V)
iL[1..8]	Current flowing through the inductors – vector rows = 1, columns = 8 (A)
Vsw[1..8]	Main switches Voltage (V) – Positive for forward voltages – vector.
Isw[1..8]	Main switches Current (A) – Positive for forward current– vector.
Vd[1..8]	Diodes / synch switches voltage (V) - Positive for reverse voltages – vector. The voltage across the re-circulating diode / synchronous switches.
Id[1..8]	Diode / synch switches current (A) – Positive for forward current – vector. The current through the re-circulating diode / synchronous switches.
iCo	Output Capacitor Current (A)
vCin	Input capacitor Voltage (V) This will be the voltage charge on input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.
iCin	Input capacitor current (A)
%Eff	Converter Efficiency (%), averaged over a switching cycle. The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switch and diode / synchronous switch conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR). The switching losses and diode reverse recovery losses along with the inductor core losses are not included in the model.

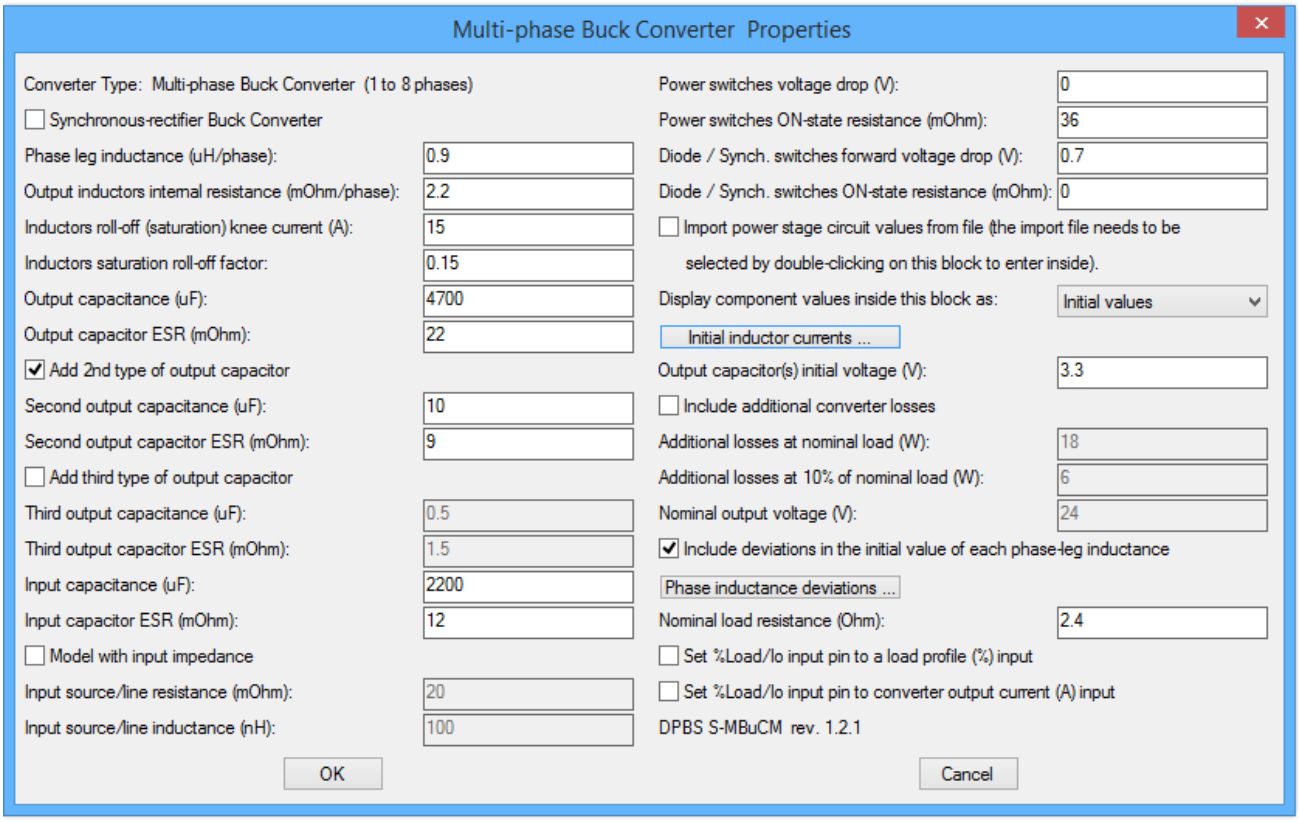
Circuit schematic: Multi-phase buck converter



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The multi-phase buck converter properties menu is shown in the following box which appears when right-clicking on the buck converter block.



Synchronous-rectifier multi-phase buck converter:

When this check box is activated the output diode of each leg of the buck converter will be modelled as a controllable switch (usually a MOSFET). This will activate the SWS input vector pin.

Phase leg inductance:

Enter the value of the buck converter output inductance for each leg of the multi-phase buck converter in micro-Henrys.

Output inductors internal resistance:

The winding resistance of the buck inductor should be given here in milli-Ohms per phase leg. The resistance of any connections can be summed into the given value.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads. This capacitor is one common capacitor for all phase legs.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if “Model with input impedance” is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to model the multi-phase buck converter with input impedance. This can also be used to model the effects of an input filter on the converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henrys.

Power switch voltage drop:

The forward voltage drop, in Volts, across the main switch of each leg of the buck converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch. For a synchronous converter, if the current through the inductor is negative and both the switches are in the OFF state, this value will be used as the forward voltage drop of the integrated reverse diode of the main switch.

Power switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diode / Synch. Switch forward voltage drop:

The forward voltage drop, in Volts, across the diode / synchronous switch (in the case of a synchronous-rectifier converter) of each leg of the multi-phase buck converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

Diode / Synch. Switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET

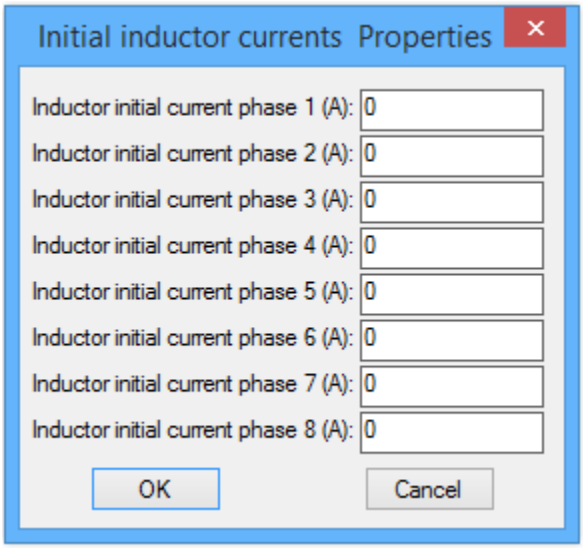
switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file. This file is typically generated by the Power Stage Design Tool within the Digital Power Design Suite. The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Initial inductor currents:

The initial inductor current (at simulation start) can be entered here in Amperes.



Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Since the converter duty cycle is inversely proportional to the efficiency as:

$$D = \frac{Vo}{\eta \cdot Vi} \qquad Vi > Vo \qquad \text{(Buck converter in CCM)}$$

the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced when this box is checked.

Additional losses at nominal load:

Insert the additional full-load losses in Watts.

Additional losses at 10% load:

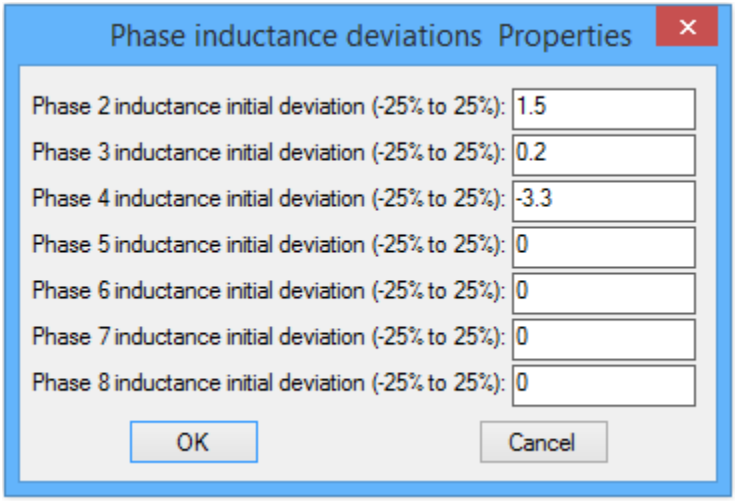
Insert the additional losses in Watts at 10% of full-load.

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Include deviations in the initial value of each phase leg inductance:

The value of the inductor of each phase leg will never be identical in practise and deviations of the initial inductance can be accounted for by checking this box.



Phase x inductance initial deviation:

For each phase, enter the desired deviation of the initial inductance within ±25% of the nominal value.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

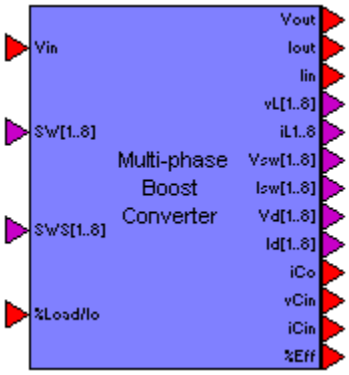
Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

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Multi-phase Boost Converter

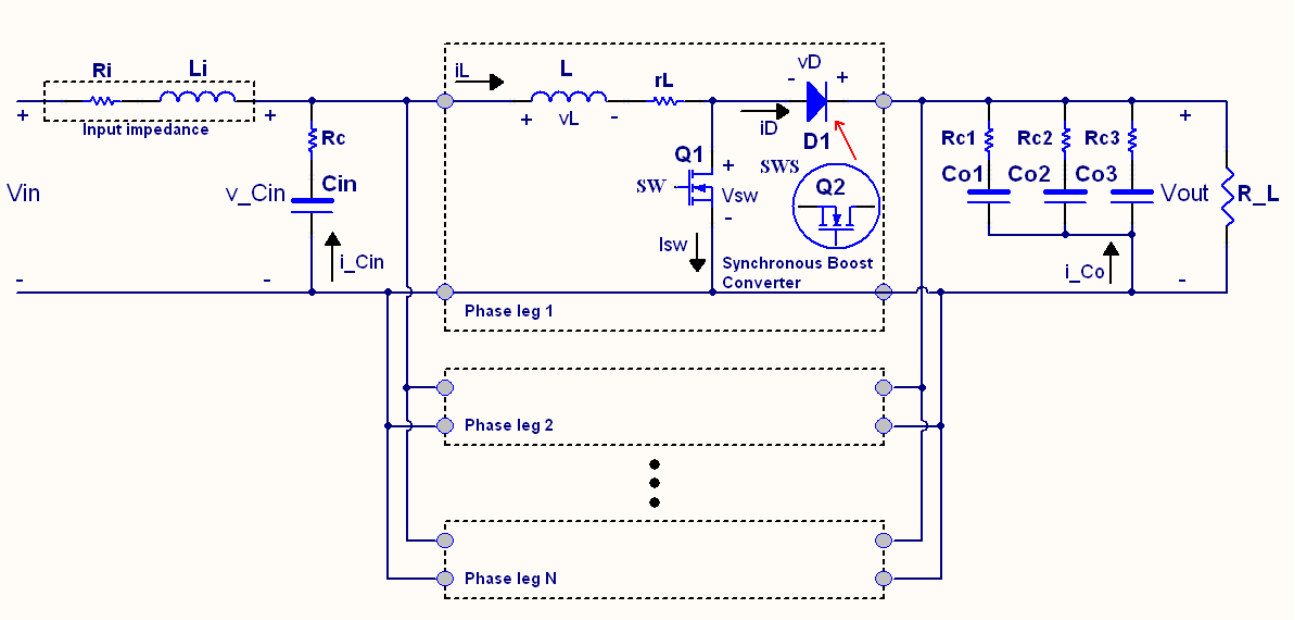
The multi-phase boost converter is an 8 leg boost converter with common input and output capacitors.

Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW1..8	Main switches control (SW < 1 = OFF, SW ≥ 1 = ON) – vector; rows = 1, columns = 8.
	SWS1..8	Synchronous switches control (SW < 1 = OFF, SW ≥ 1 = ON) – vector; rows = 1, columns = 8.
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V)
	Iout	Converter output current (A)
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered switch current for the case of the boost converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vL1..8	Voltage across the inductors (V) – vector rows = 1, columns = 8
	iL1..8	Current flowing through the inductors (A) – vector rows = 1, columns = 8
	Vsw1..8	Main switches Voltage (V) – Positive for forward voltages – vector.
	Isw1..8	Main switches Current (A) – Positive for forward current– vector.
	Vd1..8	Diodes / synch switches voltage (V) - Positive for reverse voltages – vector. The voltage across the boost output diode / synchronous switch.
	Id1..8	Diode / synch switches current (A) – Positive for forward current – vector. The current through the boost output diode / synchronous switch.
	iCo	Output Capacitor Current (A)
	vCin	Input capacitor Voltage (V)

iCin Input capacitor current (A)

%Eff Converter Efficiency (%), averaged over a switching cycle.

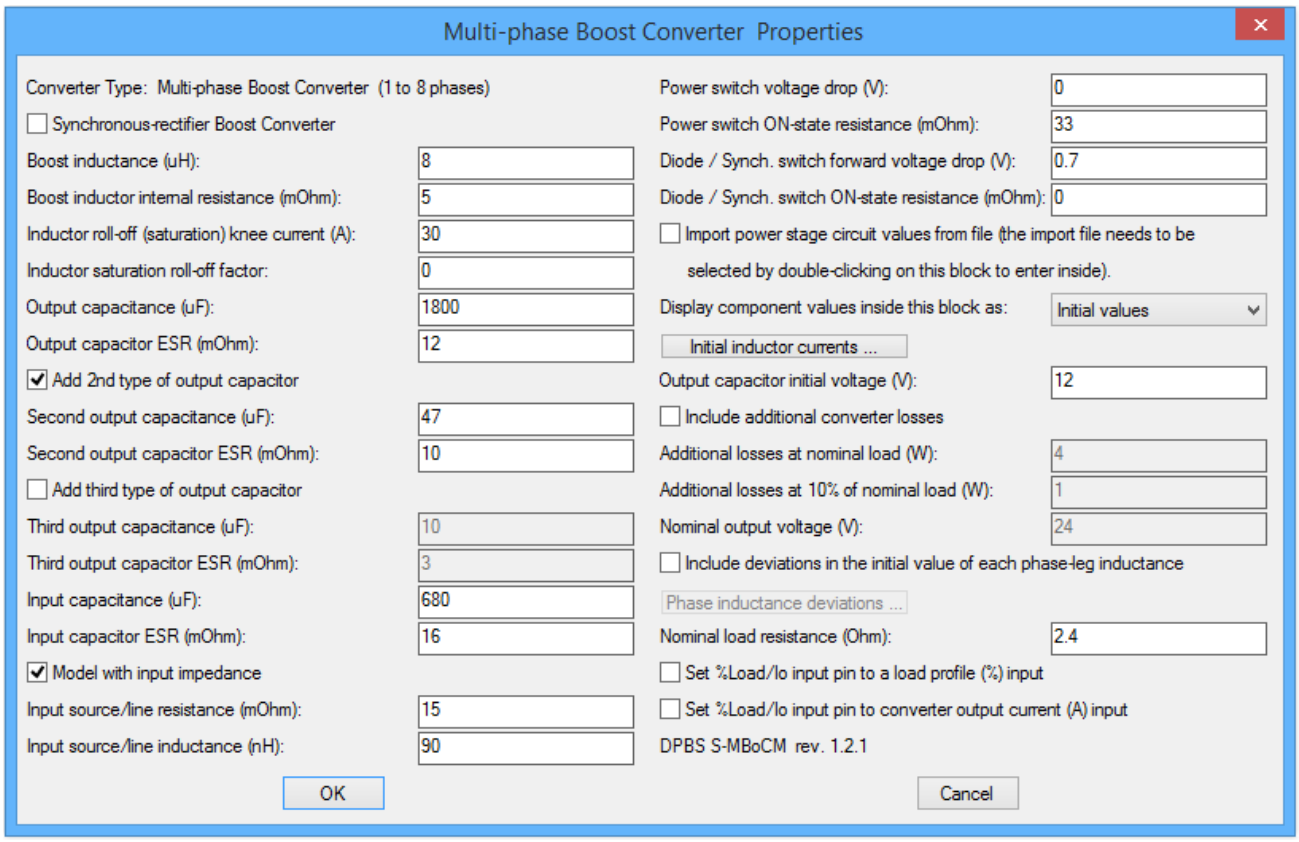
Circuit schematic: Multi-phase boost converter



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

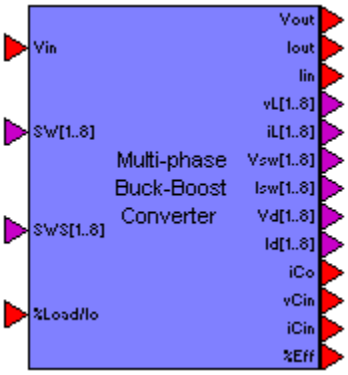
Dialog properties:

The multi-phase boost converter properties menu is shown in the following box which appears when right-clicking on the converter block.



The dialogs are very similar to the multi-phase buck converter and the boost converter.

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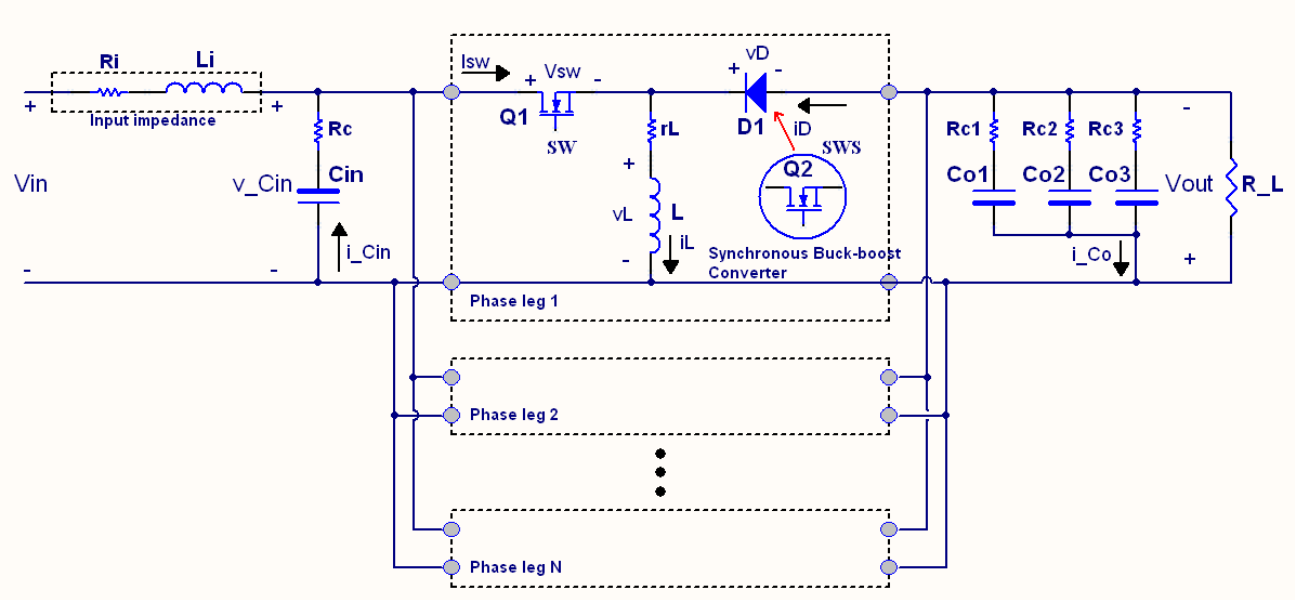
Multi-phase Buck-boost Converter

The multi-phase buck-boost converter is an 8 leg inverting (positive input, negative output) buck-boost converter with common input and output capacitors.

Input Pins:	**Vin**	Input voltage (V)
	SW1..8	Main switches control (SW < 1 = OFF, SW ≥ 1 = ON) – vector; rows = 1, columns = 8.
	SWS1..8	Synchronous switches control (SW < 1 = OFF, SW ≥ 1 = ON) – vector; rows = 1, columns = 8.
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V)
	Iout	Converter output current (A)
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered switch current for the case of the buck-boost converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vL1..8	Voltage across the inductors – vector rows = 1, columns = 8 (V).
	iL1..8	Current flowing through the inductors – vector rows = 1, columns = 8 (A)
	Vsw1..8	Main switches Voltage (V) – Positive for forward voltages – vector.
	Isw1..8	Main switches Current (A) – Positive for forward current– vector.
	Vd1..8	Diodes / synch switches voltage (V) - Positive for reverse voltages – vector. The voltage across the buck-boost output diode / synchronous switch.
	Id1..8	Diode / synch switches current (A) – Positive for forward current – vector. The current through the buck-boost output diode / synchronous switch.
	iCo	Output Capacitor Current (A)
	vCin	Input capacitor Voltage (V)
	iCin	Input capacitor current (A)

%Eff Converter Efficiency (%), averaged over a switching cycle.

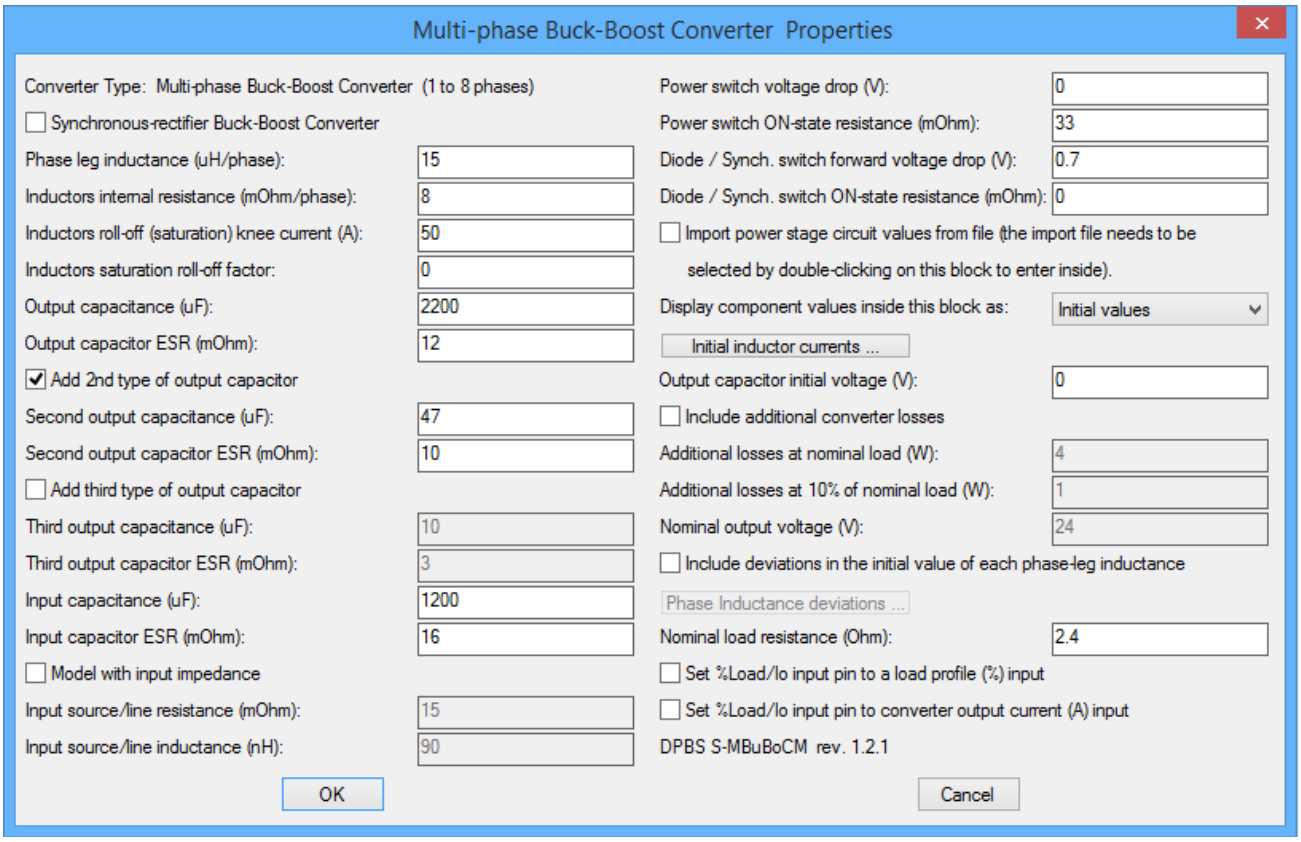
Circuit schematic: Multi-phase buck-boost converter



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

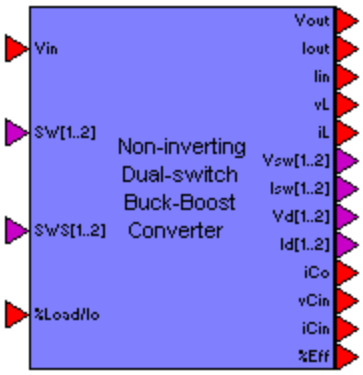
Dialog properties:

The multi-phase buck-boost converter properties menu is shown in the following box which appears when right-clicking on the converter block.



The dialogs are very similar to the multi-phase buck converter and the buck-boost converter.

Contents - Simulation



Non-inverting Dual-switch Buck-boost Converter

This converter will normally operate as a buck-boost converter with a positive output for a positive input (non-inverting). It can however function as a buck converter (SW2 remains off) or as a boost converter (SW1 remains permanently in the on state).

Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW1..2	Main switch control (SW < 1 = OFF, SW ≥ 1 = ON); vector rows = 1, columns = 2.
	SWS1..2	Synchronous switch control (SW < 1 = OFF, SW ≥ 1 = ON); vector rows = 1, columns = 2.
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V). Since this buck-boost configuration is a non-inverting converter, the output voltage will be positive.
	Iout	Converter output current (A)
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered switch current for the case of the non-inverting buck-boost converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vL	Voltage across the inductor (V)
	iL	Current flowing through the inductor (A)
	Vsw1..2	Switch Voltages (V) – Positive for forward voltages; vector rows = 1, columns = 2.
	Isw1..2	Switch Currents (A) – Positive for forward current; vector rows = 1, columns = 2.
	Vd1..2	Diode Voltages (V) - Positive for reverse voltages; vector rows = 1, columns = 2. The voltages across the buck-boost diodes / synchronous switches.
	Id1..2	Diode Currents (A) – Positive for forward current; vector rows = 1, columns = 2. The current through the buck-boost output diode / synchronous switches.
	iCo	Output Capacitor Current (A)
	vCin	Input capacitor Voltage (V)

This will be the voltage charge on input capacitor if the “model with input impedance” is selected, otherwise it will be directly the input voltage.

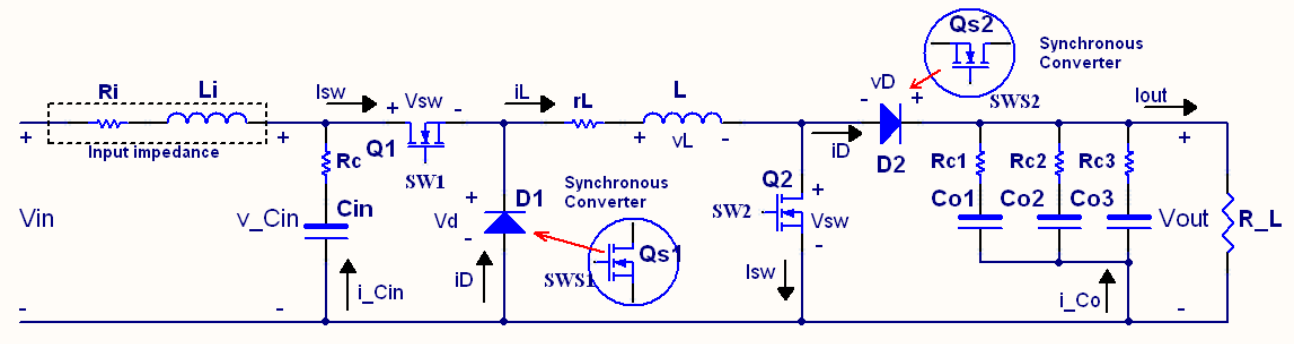
iCin Input capacitor current (A)

%Eff Converter Efficiency (%), averaged over a switching cycle.

The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switch and diode / synchronous switch conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR).

The switching losses and diode reverse recovery losses along with the inductor core losses are not included in the model.

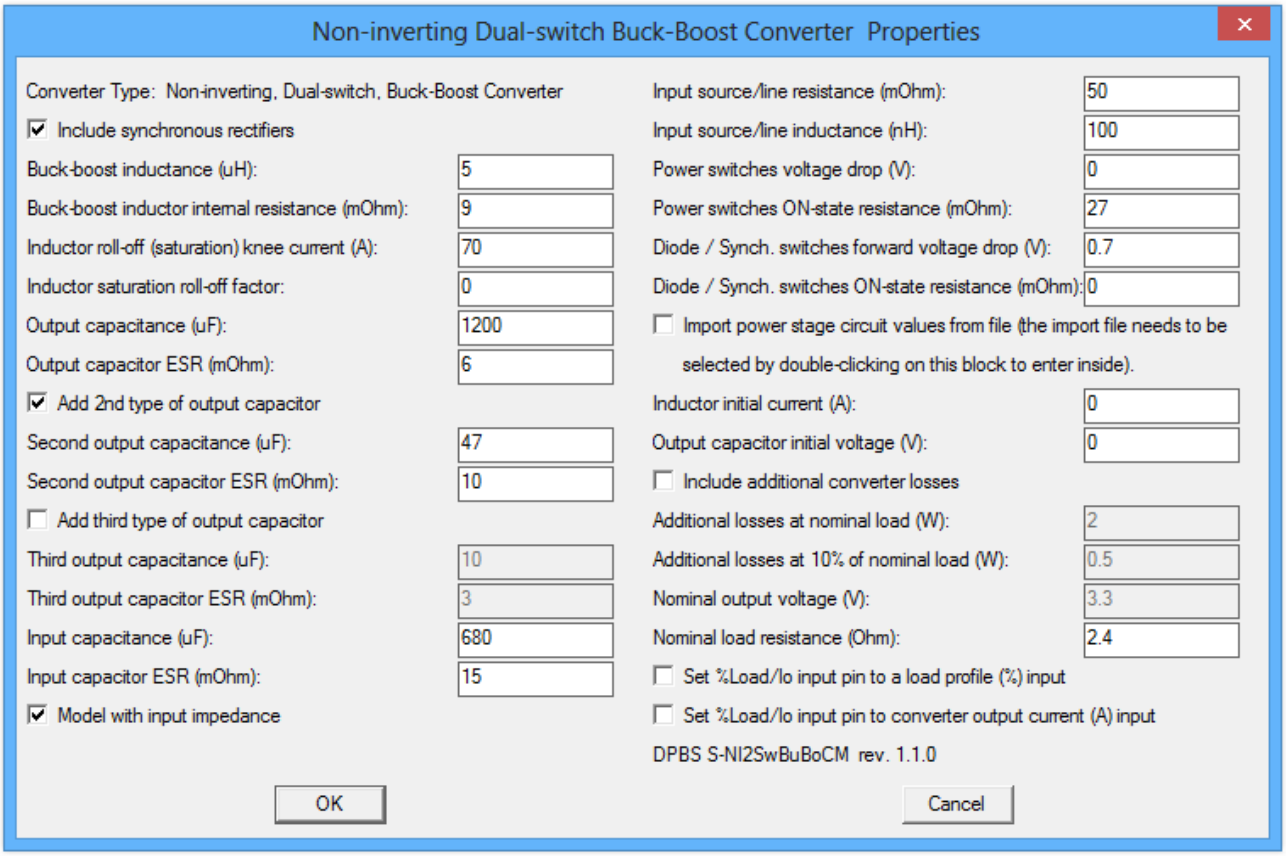
Circuit schematic: Non-inverting dual-switch buck-boost converter



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The non-inverting, dual-switch buck-boost converter properties menu is shown in the following box which appears when right-clicking on the buck-boost converter block.



Include synchronous rectifiers:

When this check box is activated the diodes of the non-inverting buck-boost converter will be modelled as controllable switches (usually MOSFETs). This will activate the SWS vector input pin.

Input inductance:

Insert the value of the buck-boost converter input inductance in micro-Henries.

Input inductor internal resistance:

The winding resistance of the buck-boost inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the current flowing through the inductor.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if "Model with input impedance" is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to include the input impedance in the buck-boost converter model. This can also be used to model the effects of an input filter in the buck-boost converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switches voltage drop:

The forward voltage drop, in Volts, across the main switch of the boost converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch. For a synchronous converter, if the current through the inductor is negative and both the switches are in the OFF state, this value will be used as the forward voltage drop of the integrated reverse diode of the main switch.

Power switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diodes / Synch. Switches forward voltage drop:

The forward voltage drop, in Volts, across the diodes / synchronous switches (in the case of a synchronous-rectifier converter) of the non-inverting buck-boost converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

Diodes / Synch. Switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file. The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Initial inductor current:

The initial inductor current (at simulation start) can be entered here in Amperes.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Since the converter duty cycle is a function of the efficiency as:

$$\mathbf{D} = \frac{\mathbf{Vo}}{\boldsymbol{\eta} \cdot \mathbf{Vi} + \mathbf{Vo}} \qquad \text{(Buck-boost converter in CCM)}$$

the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced .

Additional losses at nominal load:

Insert the required additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load..

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

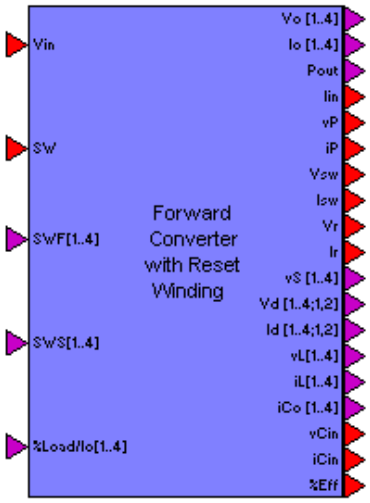
Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

Contents - Simulation



Forward Converter (with Reset Winding)

The forward converter is an isolated configuration of the buck converter. This converter configuration can have from one to four outputs, each controlled by a single switch on the primary side. The transformer is reset (or de-magnetised) during the switch off time by an additional winding which is clamped to the input voltage via a reverse diode.

Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW	Main switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	SWF(1..4)	Synchronous switch control of the secondary winding blocking diode for each of the four outputs; vector, rows = 1, columns = 4 (SW < 1 = OFF, SW ≥ 1 = ON).
	SWS(1..4)	Synchronous switch control of the re-circulating output forward diode for each of the four outputs; vector, rows = 1, columns = 4 (SW < 1 = OFF, SW ≥ 1 = ON).
	%Load/Io[1..4]	Proportion of the nominal load of each output in percent or the load currents in amperes, depending upon the configuration of this pin in the block dialog; vector, rows = 1, columns = 4. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout(1..4)**	Converter output voltages (V); vector, rows = 1, columns = 4. The voltage will be negative if "invert output" is selected for that output.
	Iout(1..4)	Converter output currents (A); vector, rows = 1, columns = 4, again the output current will be negative if "invert output" is selected for that output.
	Pout(1..4)	Converter output power of each output (W); vector, rows = 1, columns = 4.
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the input current averaged over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered primary current minus the reset winding current. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vP	Voltage across the transformer primary winding (V).
	iP	Current flowing through the transformer primary winding (A).
	Vsw	Switch Voltage (V) – Positive for forward voltages.

Isw Switch Current (A) – Positive for forward current; vector rows = 1, columns = 4.

Vr Voltage across the transformer reset winding (V).

Ir Current flowing through the transformer reset winding (A).

vS(1..4) Transformer secondary winding voltages (V); vector, rows = 1, columns = 4.

Vd(1..4;1,2) Diode Voltage of each output stage (V) - Positive for reverse voltages; vector rows = 2, columns = 4. The voltage across the forward output diodes / synchronous switches and the secondary winding output diodes /synchronous switches.

Id(1..4;1,2) Diode Current of each output stage (A) – Positive for forward current; vector rows = 2, columns = 4. The current through the forward output diodes / synchronous switches and the secondary winding output diodes /synchronous switches.

iCo(1..4) Output Capacitor Currents for each output (A) ; vector, rows = 1, columns = 4.

vCin Input capacitor Voltage (V)

This will be the voltage charge on input capacitor if the “model with input impedance” is selected, otherwise it will be directly the input voltage.

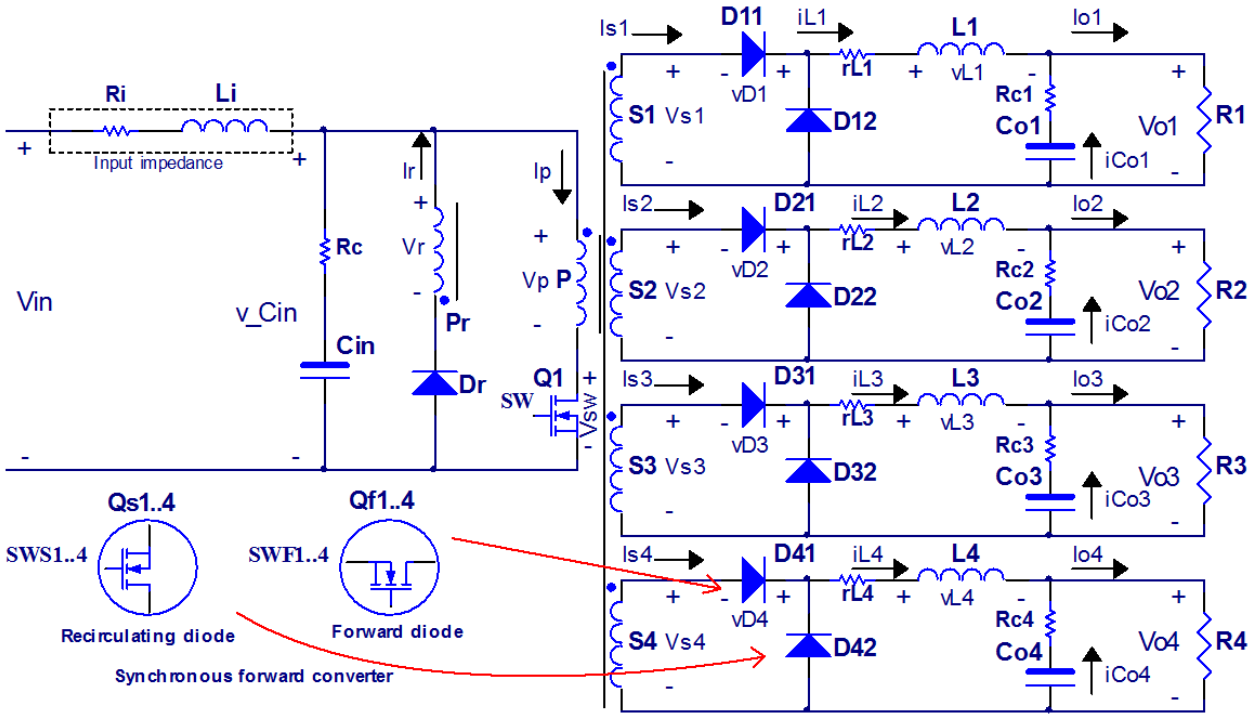
iCin Input capacitor current (A)

%Eff Converter Efficiency (%), averaged over a switching cycle.

The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switch and diode / synchronous switch conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR).

The switching losses and diode reverse recovery losses along with the transformer and inductors core losses are not included in the model.

Circuit schematic: Forward Converter

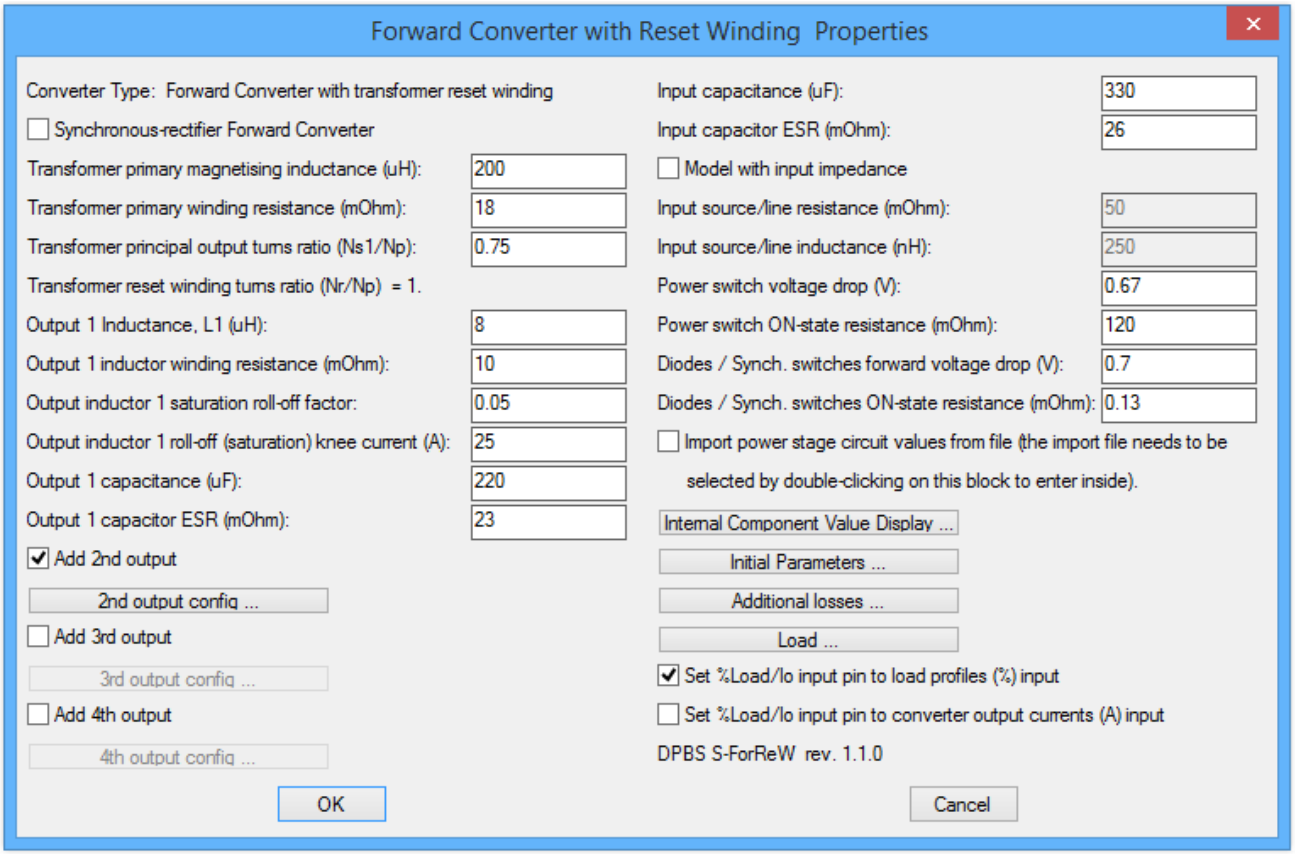


Any number from 1 to 4 separate output stages can be included in the forward converter model. Output stages can also be inverted for negative output voltages.

Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The forward converter properties menu is shown in the following box which appears when right-clicking on the forward converter block.



Synchronous-rectifier forward Converter:

When this check box is activated the output diodes of the forward converter will be modelled as a controllable switches (usually a MOSFET). This will activate the SWS and SWF vector input pins.

Transformer primary magnetising inductance:

Insert the value of the forward converter transformer magnetising inductance in micro-Henrys.

Transformer primary winding resistance:

The winding resistance of the transformer primary winding should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Transformer principal output turns ratio (Ns1/Np):

Enter the turns ratio of the first secondary winding with respect to the primary winding.

Transformer reset winding turns ration (Nr/Np) = 1:

Since the reset winding is clamped to the input voltage when the switch is off, the reset winding has a fixed turns ratio of 1:1.

Output inductance L1:

Insert the value of the forward converter output 1 inductance in micro-Henrys.

Output inductor internal resistance L1:

The winding resistance of the output1 inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Output inductor 1 roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the current flowing through the inductor.

Output inductor 1 saturation roll-off factor:

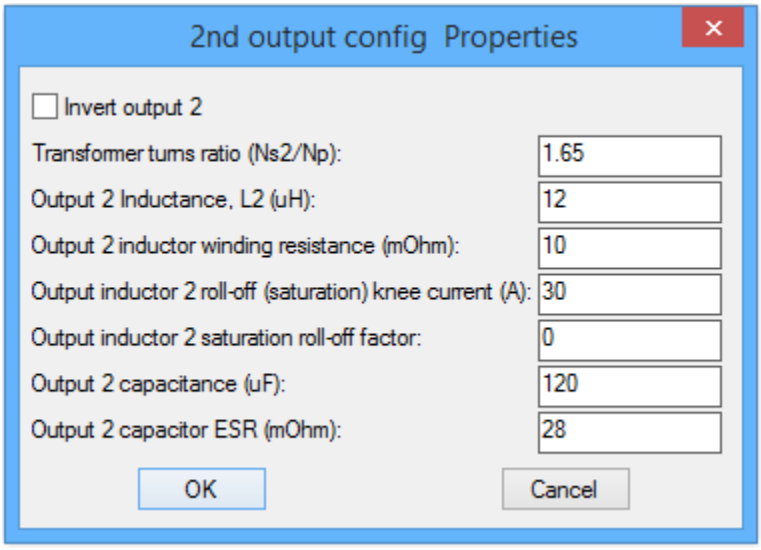
The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output 1 capacitance:

Insert the value of the capacitor of the first or principal output in micro-Farads.

Output 1 capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor 1 should be given here in milli-Ohms.



Add 2nd output:

Select this box to add a second output stage with additional transformer winding to the forward converter.

Invert output 2:

Select this box if a negative output is required for the 2nd output stage.

Transformer turns ratio (Ns2/Np):

Enter the turns ratio of the second output secondary winding with respect to the primary winding.

Output inductance L2:

Insert the value of the forward converter output 2 inductance in micro-Henries.

Output inductor internal resistance L2:

The winding resistance of the output2 inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Output inductor 2 roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the current flowing through the inductor.

Output inductor 2 saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output 2 capacitance:

Insert the value of the capacitor of the second output in micro-Farads.

Output 2 capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor 2 should be given here in milli-Ohms.

Add 3rd output:

Select this box to add a third output stage with another additional transformer winding to the forward converter. The component values must be given similar to the 2nd output stage above.

Add 4th output:

Select this box to add a fourth output stage with additional transformer winding to the forward converter. The component values must be given similar to the 2nd output stage above.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if “Model with input impedance” is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to include the input impedance in the forward converter model. This can also be used to model the effects of an input filter in the forward converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switch voltage drop:

The forward voltage drop, in Volts, across the main switch of the forward converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch. For a synchronous converter, if the current through the inductor is negative and both the switches are in the OFF state, this value will be used as the forward voltage drop of the integrated reverse diode of the main switch.

Power switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diodes / Synch. Switches forward voltage drop:

The forward voltage drop, in Volts, across the diodes / synchronous switches (in the case of a synchronous-rectifier converter) and the reset winding diode of the forward converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode. For synchronous converters, this value is only considered when the synchronous switch is off and its reverse diode is conducting.

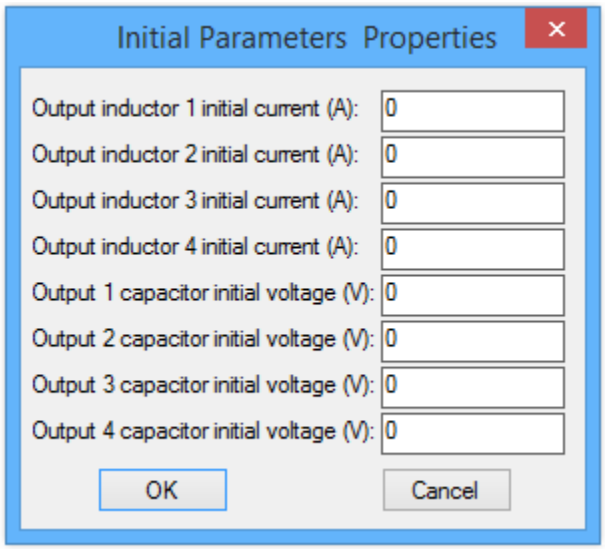
Diodes / Synch. Switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switches can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file.
The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Initial Parameters:



Output inductor 1..4 initial current:

The initial inductor current (at simulation start) of each output can be entered here in Amperes.

Output capacitor 1..4 initial voltage:

The initial voltage of the output capacitor (at simulation start) for each output can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Since the converter duty cycle is a function of the efficiency as:

$$D = \frac{Vo}{\eta \cdot N \cdot Vi} \qquad N = \frac{N_s}{N_p}$$ (Forward converter in CCM)

the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced .

Additional losses at nominal load:

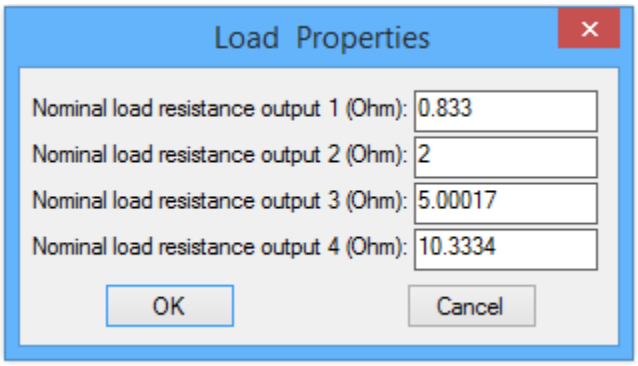
Insert the required additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load..

Nominal output voltage, output 1:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.



Nominal load resistance output 1..4:

The nominal (full-load) load resistance for each output must be entered here in Ohms.

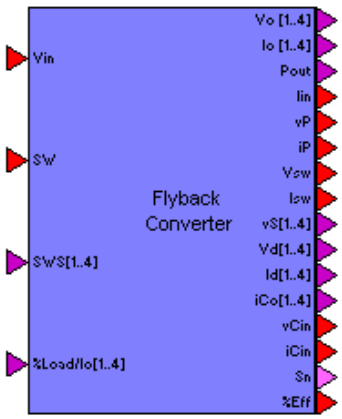
Set %Load/Io input pin to a load profiles (%) input:

Enable this check box to vary the loads according to the values at the %Load/Io vector input pin and the nominal load resistances.

Set %Load/Io input pin to converter output currents (A) input:

Enable this check box to vary the loads directly to the value of the current inputs in amperes. The nominal load resistances are not considered in this case.

Contents - Simulation



Flyback Converter (with RCD snubber)

The flyback converter is an isolated configuration of the buck-boost converter. The converter can have from one to four outputs, each controlled by a single switch on the primary side.

Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW	Main switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	SWS(1..4)	Synchronous switch control for each of the four outputs; vector rows = 1, columns = 4 (SW < 1 = OFF, SW ≥ 1 = ON).
	%Load/Io[1..4]	Proportion of the nominal load of each output in percent or the load currents in amperes, depending upon the configuration of this pin in the block dialog; vector, rows = 1, columns = 4. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout(1..4)**	Converter output voltages (V); vector, rows = 1, columns = 4. The voltage will be negative if "invert output" is selected for that output.
	Iout(1..4)	Converter output currents (A); vector, rows = 1, columns = 4, again the output current will be negative if "invert output" is selected for that output.
	Pout(1..4)	Converter output power of each output (W); vector, rows = 1, columns = 4.
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered primary winding + snubber current (when enabled) for the case of the flyback converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vP	Voltage across the transformer primary winding (V)
	iP	Current flowing through the transformer primary winding (A)
	Vsw	Switch Voltage (V) – Positive for forward voltages.
	Isw	Switch Current (A) – Positive for forward current.
	vS(1..4)	Transformer secondary winding voltages (V); vector, rows = 1, columns = 4.

Vd(1..4) Diode Voltages of each output (V) - Positive for reverse voltages; vector, rows = 1, columns = 4. The voltage across the flyback output diodes/ synchronous switches.

Id(1..4) Diode Currents of each output (A) – Positive for forward current; vector rows = 1, columns = 4. The current through the flyback output diodes / synchronous switches. This current is also the secondary winding current.

iCo(1..4) Output Capacitor Currents for each output (A) ; vector rows = 1, columns = 4.

vCin Input capacitor Voltage (V)

This will be the voltage charge on input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.

iCin Input capacitor current (A)

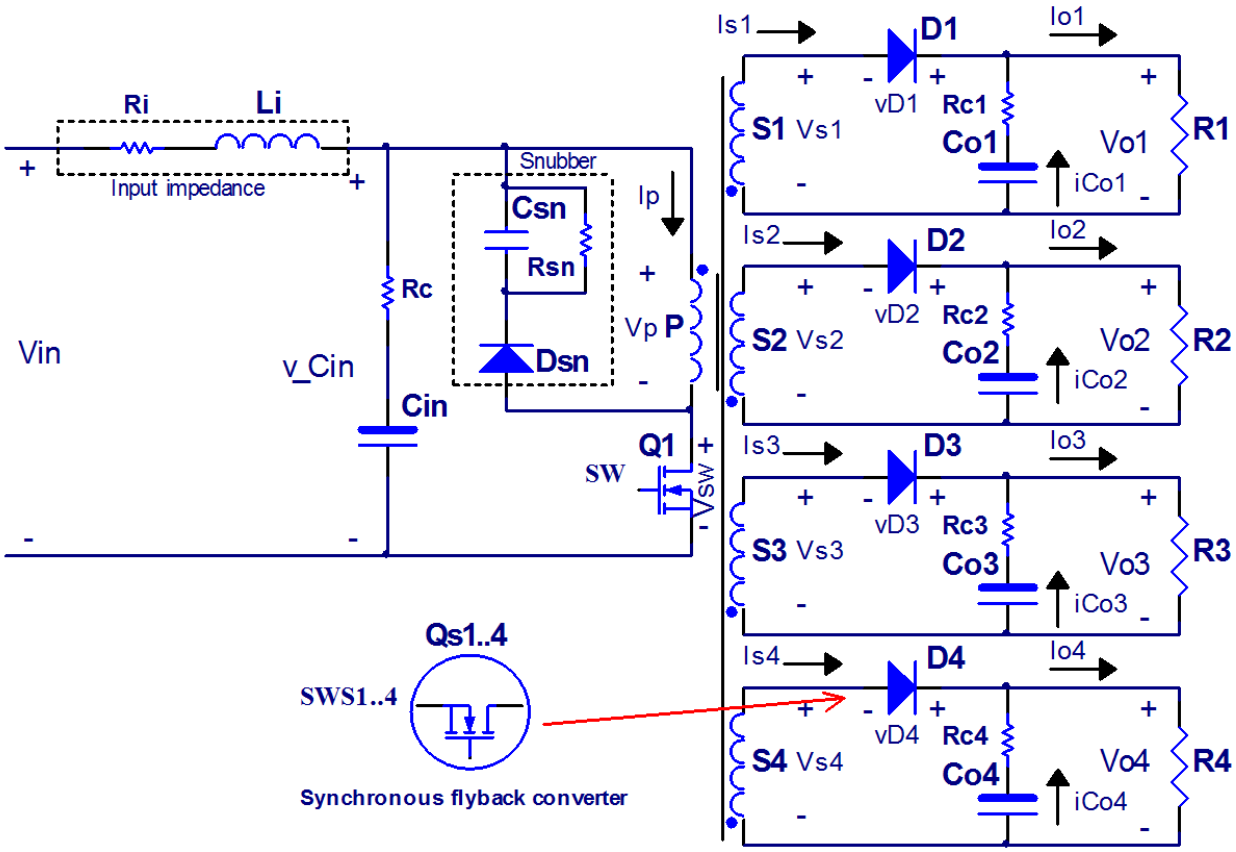
Sn Output (format struct) giving the various values of the RCD snubber circuit. See below for an explanation.

%Eff Converter Efficiency (%), averaged over a switching cycle.

The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switch and diode / synchronous switch conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR). The dissipative loss of the RCD snubber is also included when enabled for the flyback converter.

The switching losses and diode reverse recovery losses along with the inductor core losses are not included in the model.

Circuit schematic: Flyback Converter

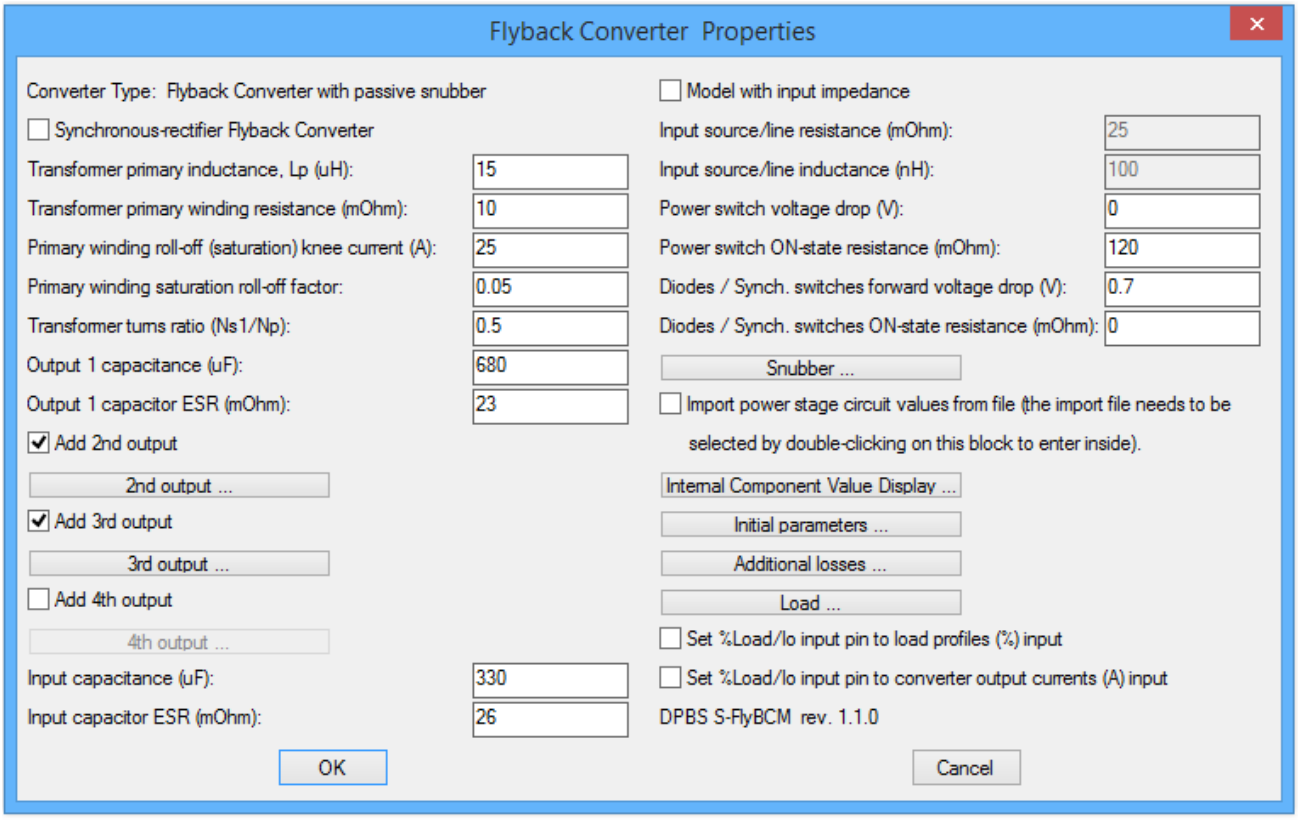


Any number from 1 to 4 separate output stages can be included in the flyback converter model. Output stages can also be inverted for negative output voltages.

Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The flyback converter properties menu is shown in the following box which appears when right-clicking on the flyback converter block.



Synchronous-rectifier Flyback Converter:

When this check box is activated the output diode of each output of the flyback converter will be modelled as a controllable switch (usually a MOSFET). This will activate the SWS vector input pin.

Transformer primary winding inductance, Lp:

Insert the value of the flyback converter transformer primary winding inductance in micro-Henrys.

Transformer primary winding internal resistance:

The winding resistance of the flyback converter primary winding should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Primary winding roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the current flowing through the inductor.

Primary winding saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Transformer principal output turns ratio (Ns1/Np):

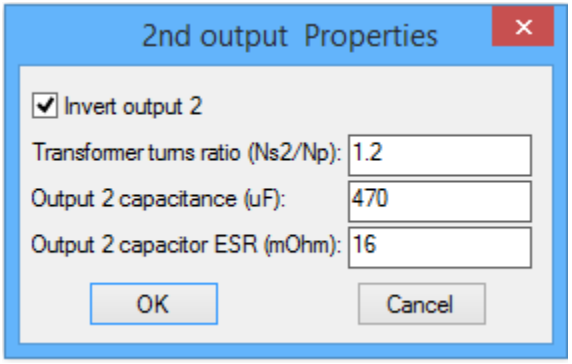
Enter the turns ratio of the first secondary winding with respect to the primary winding.

Output 1 capacitance:

Insert the value of the main output 1 capacitor in micro-Farads.

Output 1capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor 1 should be given here in milli-Ohms.



Add 2nd output:

Select this box to add a second output stage with additional transformer winding to the flyback converter.

Invert output 2:

Select this box if a negative output is required for the 2nd output stage.

Transformer turns ratio (Ns2/Np):

Enter the turns ratio of the second output secondary winding with respect to the primary winding.

Output 2 capacitance:

Enter the value of the capacitor of the second output in micro-Farads.

Output 2 capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor 2 should be given here in milli-Ohms.

Add 3rd output:

Select this box to add a third output stage with another additional transformer winding to the flyback converter. The component values must be given similar to the 2nd output stage above.

Add 4th output:

Select this box to add a fourth output stage with additional transformer winding to the flyback converter. The component values must be given similar to the 2nd output stage above.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if “Model with input impedance” is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to include the input impedance of the flyback converter model. This can also be used to model the effects of an input filter in the converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switch voltage drop:

The forward voltage drop, in Volts, across the main switch of the flyback converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch. For a synchronous converter, if the current through the inductor is negative and both the switches are in the OFF state, this value will be used as the forward voltage drop of the integrated reverse diode of the main switch.

Power switch ON-state resistance:

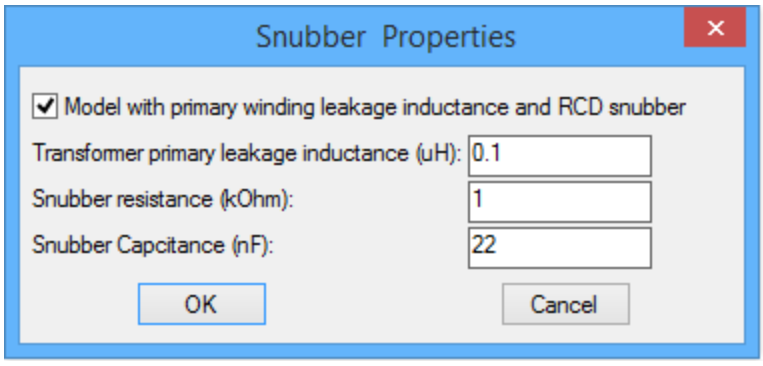
The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diodes / Synch. Switches forward voltage drop:

The forward voltage drop, in Volts, across the diodes / synchronous switches (in the case of a synchronous-rectifier converter) of the flyback converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

Diodes / Synch. Switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.



Model with primary winding leakage inductance and RCD snubber:

Check this box if the parasitic leakage inductance of the flyback converter is desired to be included in the model. A passive RCD (resistor-capacitor-diode) snubber will automatically be included in the model as part of the circuit diagram.

Transformer primary winding leakage inductance:

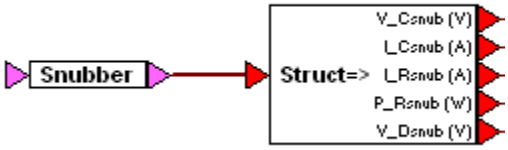
Enter the value of the leakage inductance (referred to the primary) in micro-Henries.

Snubber resistance:

Enter the value of the snubber dissipative resistor in kilo-Ohms.

Snubber capacitance:

Enter the value of the snubber capacitor in nano-Farads.



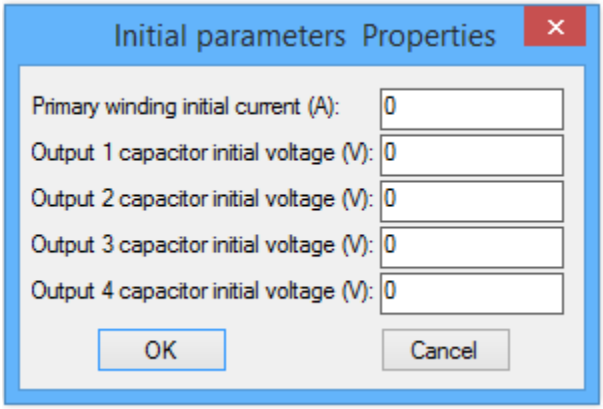
The struct pin output will provide the necessary values to characterize the snubber performance. Note that the leakage inductance is a parasitic component and will have values typically around 1% of the primary inductance. This means that the typical simulation frequency of one hundred times the switching frequency will not be sufficient to correctly represent the current generated by the leakage inductance. A simulation frequency of between one thousand and ten thousand times the switching frequency will be required in this case, considerably slowing down the simulation speed.

Import power stage circuit values from file:

The power component values can be directly read from a file.
The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Primary winding initial current:

The initial primary winding current (at simulation start) can be entered here in Amperes.



Output capacitor 1..4 initial voltage:

The initial voltage of the output capacitor (at simulation start) of each of the four possible outputs can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Since the converter duty cycle is a function of the efficiency as:

CCM) $D = \frac{Vo}{\eta \cdot N \cdot Vi + Vo}$ $N = \frac{N_s}{N_p}$ (Flyback converter in

the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced .

Additional losses at nominal load:

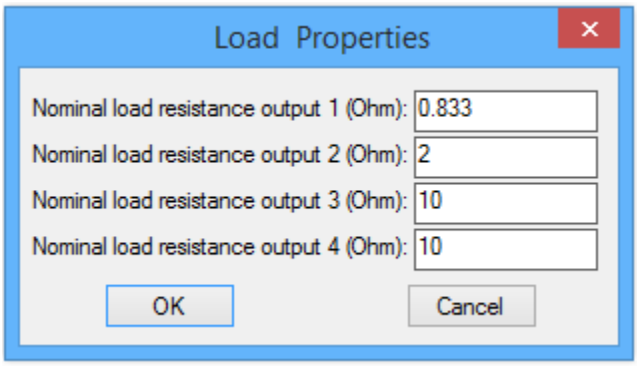
Insert the required additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load..

Nominal output voltage, output 1:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.



Nominal load resistance output 1..4:

The nominal (full-load) load resistance for each output must be entered here in Ohms.

Set %Load/Io input pin to a load profiles (%) input:

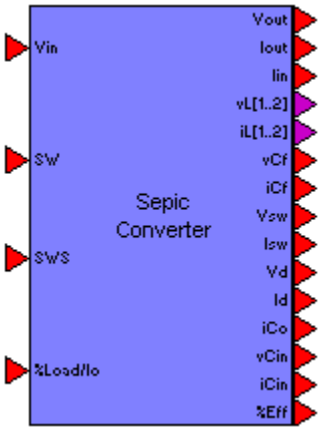
Enable this check box to vary the loads according to the values at the %Load/Io vector input pin and the nominal load resistances.

Set %Load/Io input pin to converter output currents (A) input:

Enable this check box to vary the loads directly to the value of the current inputs in amperes. The nominal load resistances are not considered in this case.

Contents - Simulation

Single Ended Primary Inductor Converter (SEPIC)



This converter, in its most basic form, is a fourth order converter with two inductors and an additional flying capacitor.

Input Pins:	**Vin**	Positive input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW	Main switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	SWS	Synchronous switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V). Since the sepic converter has a non-inverting configuration, the output voltage will be positive with a positive input voltage.
	Iout	Converter output current (A)
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered input inductor current for the case of the sepic converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vL1..2	Voltage across the inductors (V); vector, rows = 1, columns = 2.
	iL1..2	Current flowing through the inductor (A);vector, rows = 1, columns = 2.
	vCf	Flying Capacitor Voltage (V).
	iCf	Flying Capacitor Current (A).
	Vsw	Switch Voltage (V) – Positive for forward voltages.
	Isw	Switch Current (A) – Positive for forward current.
	Vd	Diode Voltage (V) - Positive for reverse voltages.
	Id	Diode Current (A) - Positive for forward current.

The current through the sepic output diode / synchronous switch.

iCo Output Capacitor Current (A)

vCin Input capacitor Voltage (V)

This will be the voltage charge on the input capacitor if the “model with input impedance” is selected, otherwise it will be directly the input voltage.

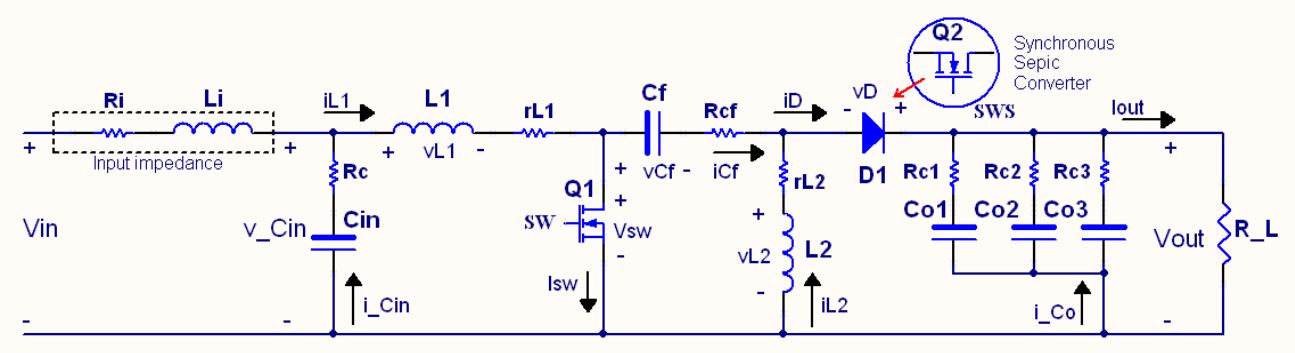
iCin Input capacitor current (A)

%Eff Sepic converter Efficiency (%), averaged over a switching cycle.

The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switch and diode / synchronous switch conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR).

The switching losses and diode reverse recovery losses along with the inductor core losses are not included in the model.

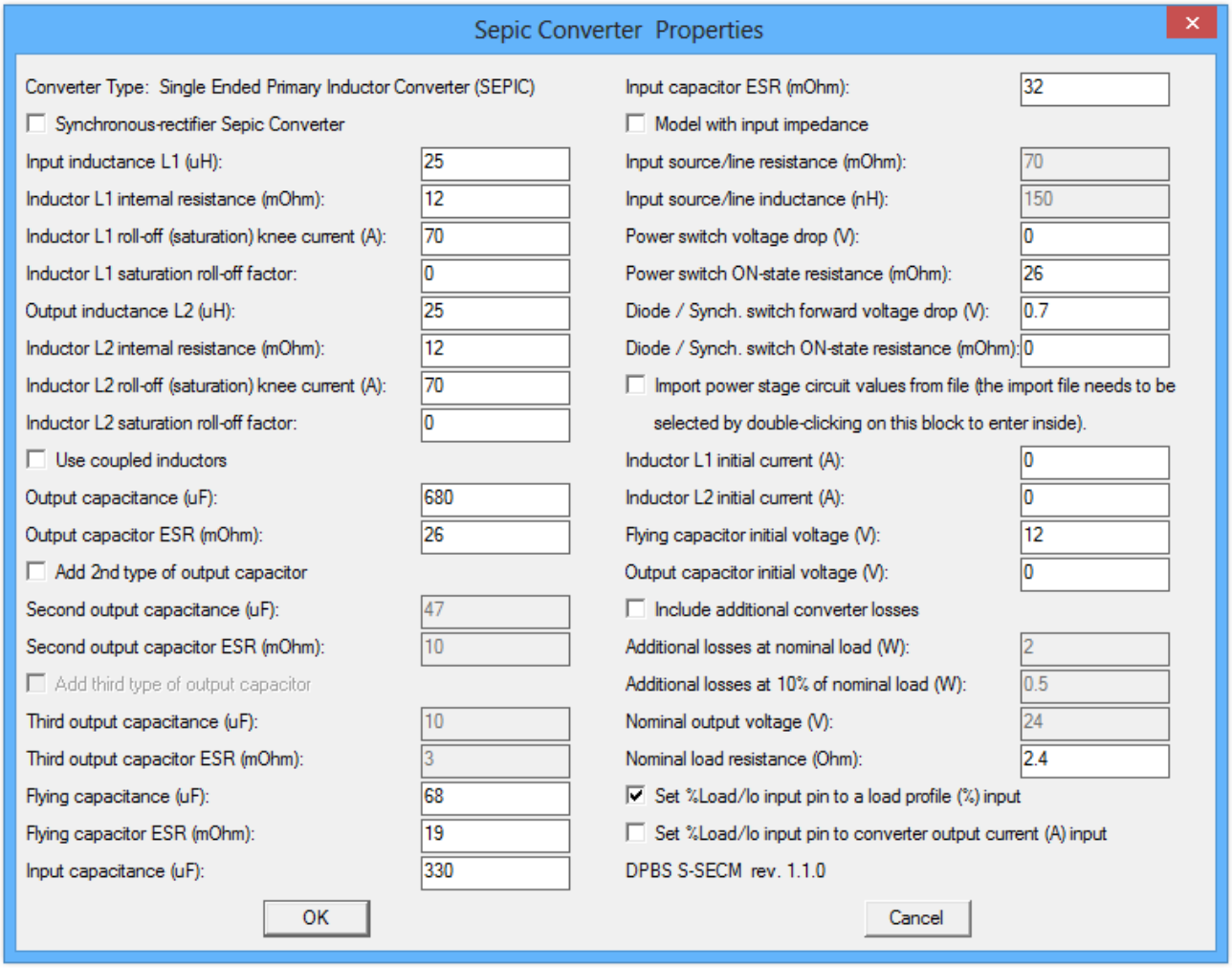
Circuit schematic: SEPIC converter



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The Sepic converter properties menu is shown in the following box which appears when right-clicking on the sepic converter block.



Synchronous rectifier Sepic Converter:

When this check box is activated the output diode of the sepic converter will be modelled as a controllable switch (MOSFET). This will activate the SWS input pin.

Input inductance L1:

Insert the value of the sepic input inductance in micro-Henrys.

Input inductor L1 internal resistance:

The winding resistance of the input inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor L1 roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce inductors with varying inductance dependent upon the current flowing through them.

Inductor L1 saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output inductance L2:

Insert the value of the sepic output inductance in micro-Henrys.

Output inductor L2 internal resistance:

The winding resistance of the output inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor L2 roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce inductors with varying inductance dependent upon the current flowing through them.

Inductor L2 saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Use coupled inductors:

The two inductors can be wound on the same core and in such a case the value of the two inductors must be the same in order to ensure flux balance. With coupled inductors, they are assumed to have perfect coupling and the leakage inductance is neglected. The inductors will behave as having double the inductance of two single un-coupled inductors.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Flying capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if “Model with input impedance” is selected below.

Flying capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if “Model with input impedance” is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to include the input impedance in the sepic converter model. This can also be used to model the effects of an input filter in the converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switches voltage drop:

The forward voltage drop, in Volts, across the main switch of the sepic converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch. For a synchronous converter, if the current through the inductor is negative and both the switches are in the OFF state, this value will be used as the forward voltage drop of the integrated reverse diode of the main switch.

Power switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diodes / Synch. Switches forward voltage drop:

The forward voltage drop, in Volts, across the diodes / synchronous switches (in the case of a synchronous-rectifier converter) of the sepic converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

Diodes / Synch. Switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file.
The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Inductor L1 and L2 initial current:

The initial inductor current (at simulation start) can be entered here in Amperes separately for the inductors L1 and L2.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Since the converter duty cycle is a function of the efficiency as:

$$\mathbf{D} = \frac{\mathbf{Vo}}{\boldsymbol{\eta} \cdot \mathbf{Vi} + \mathbf{Vo}}$$ (Sepic converter in CCM)

the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced .

Additional losses at nominal load:

Insert the required additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load..

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

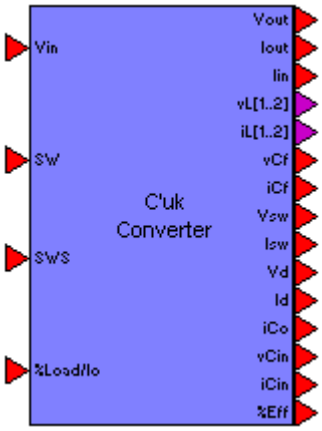
Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

Contents - Simulation



Ćuk Converter

The Ćuk converter, in its most basic form, is a fourth order converter with two inductors and an additional flying capacitor. The converter is similar to the sepic converter with the main differences being that it is an inverting converter (negative output for a positive input) and that the input and output currents are both smoothed with inductors.

Input Pins:

Vin Positive input voltage (V)

SW Main switch control (SW < 1 = OFF, SW ≥ 1 = ON).

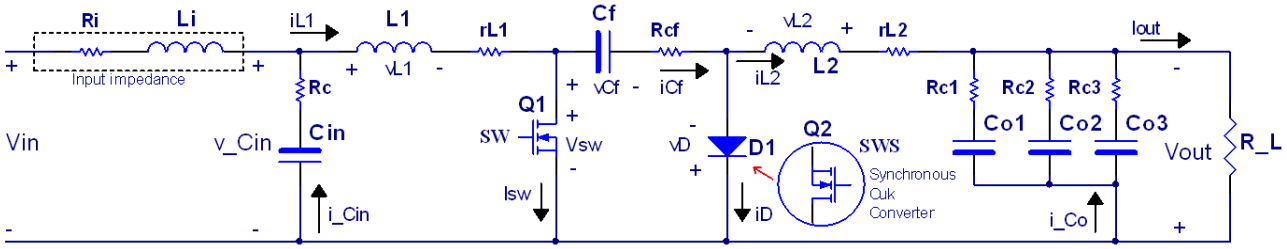
SWS Synchronous switch control (SW < 1 = OFF, SW ≥ 1 = ON).

%Load/Io Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog.

This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.

Output Pins:	**Vout**	Converter output voltage (V). Since the Ćuk converter has an inverting configuration, the output voltage will be negative with a positive input voltage.
	Iout	Converter output current, again negative (A).
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered input inductor current for the case of the Ćuk converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vL1..2	Voltage across the inductors (V); vector, rows = 1, columns = 2.
	iL1..2	Current flowing through the inductor (A); vector, rows = 1, columns = 2.
	vCf	Flying Capacitor Voltage (V).
	iCf	Flying Capacitor Current (A).
	Vsw	Switch Voltage (V) – Positive for forward voltages.
	Isw	Switch Current (A) – Positive for forward current.
	Vd	Diode Voltage (V) - Positive for reverse voltages.
	Id	Diode Current (A) - Positive for forward current. The current through the Ćuk output diode / synchronous switch.
	iCo	Output Capacitor Current (A)
	vCin	Input capacitor Voltage (V) This will be the voltage charge on the input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.
	iCin	Input capacitor current (A)
	%Eff	Ćuk converter Efficiency (%), averaged over a switching cycle.

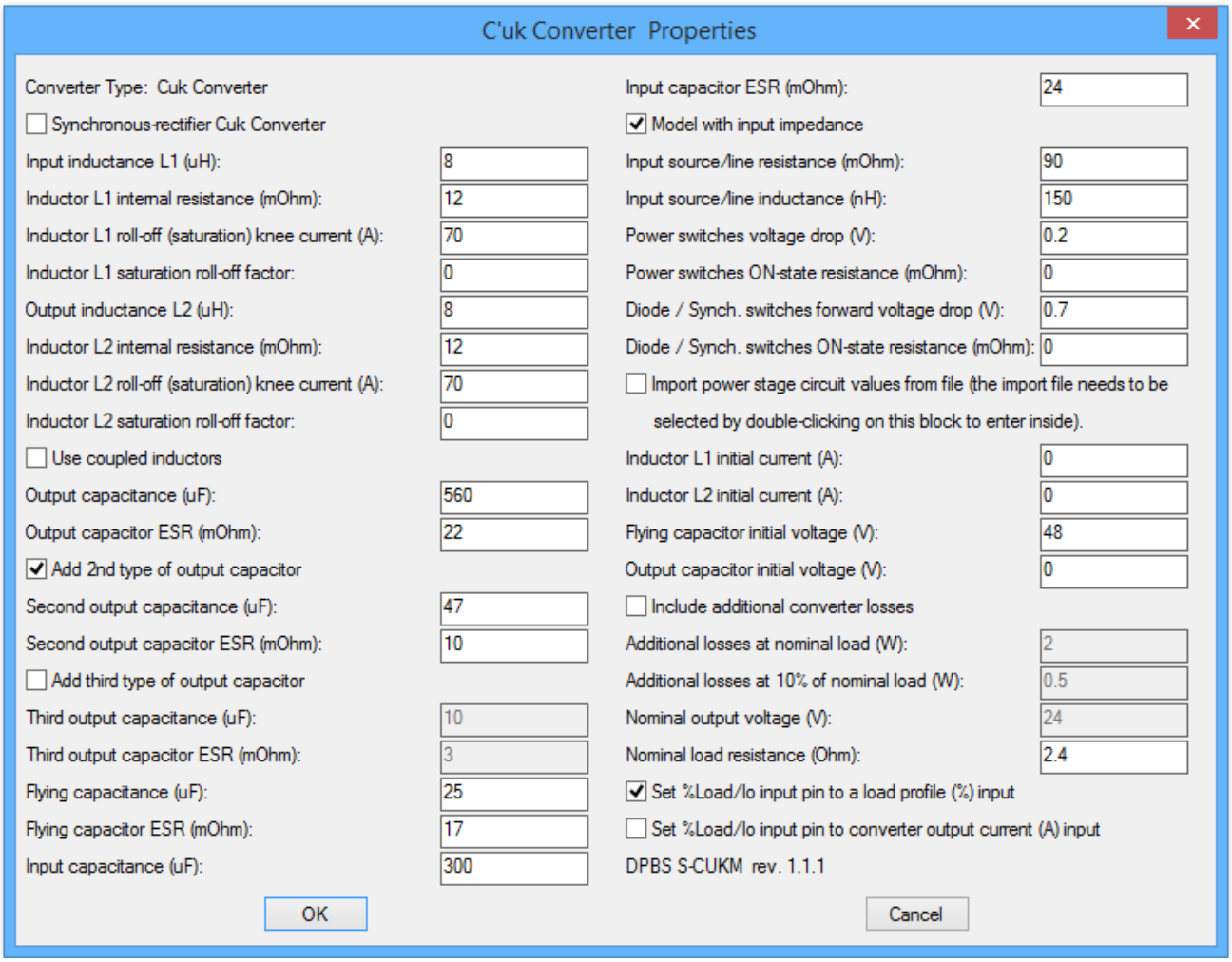
Circuit schematic: Ćuk converter

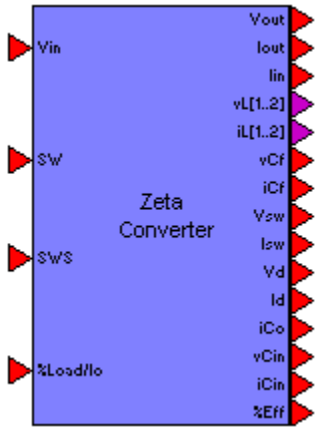


Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The dialog properties of the Ćuk converter are similar to the sepic converter.


C'uk Converter Properties
Converter Type: Cuk Converter
Synchronous-rectifier Cuk Converter
Input inductance L1 (uH): 8
Inductor L1 internal resistance (mOhm): 12
Inductor L1 roll-off (saturation) knee current (A): 70
Inductor L1 saturation roll-off factor: 0
Output inductance L2 (uH): 8
Inductor L2 internal resistance (mOhm): 12
Inductor L2 roll-off (saturation) knee current (A): 70
Inductor L2 saturation roll-off factor: 0
Use coupled inductors
Output capacitance (uF): 560
Output capacitor ESR (mOhm): 22
Add 2nd type of output capacitor
Second output capacitance (uF): 47
Second output capacitor ESR (mOhm): 10
Add third type of output capacitor
Third output capacitance (uF): 10
Third output capacitor ESR (mOhm): 3
Flying capacitance (uF): 25
Flying capacitor ESR (mOhm): 17
Input capacitance (uF): 300
Input capacitor ESR (mOhm): 24
Model with input impedance
Input source/line resistance (mOhm): 90
Input source/line inductance (nH): 150
Power switches voltage drop (V): 0.2
Power switches ON-state resistance (mOhm): 0
Diode / Synch. switches forward voltage drop (V): 0.7
Diode / Synch. switches ON-state resistance (mOhm): 0
Import power stage circuit values from file (the import file needs to be selected by double-clicking on this block to enter inside).
Inductor L1 initial current (A): 0
Inductor L2 initial current (A): 0
Flying capacitor initial voltage (V): 48
Output capacitor initial voltage (V): 0
Include additional converter losses
Additional losses at nominal load (W): 2
Additional losses at 10% of nominal load (W): 0.5
Nominal output voltage (V): 24
Nominal load resistance (Ohm): 2.4
Set %Load/Io input pin to a load profile (%) input
Set %Load/Io input pin to converter output current (A) input
DPBS S-CUKM rev. 1.1.1
OK
Cancel



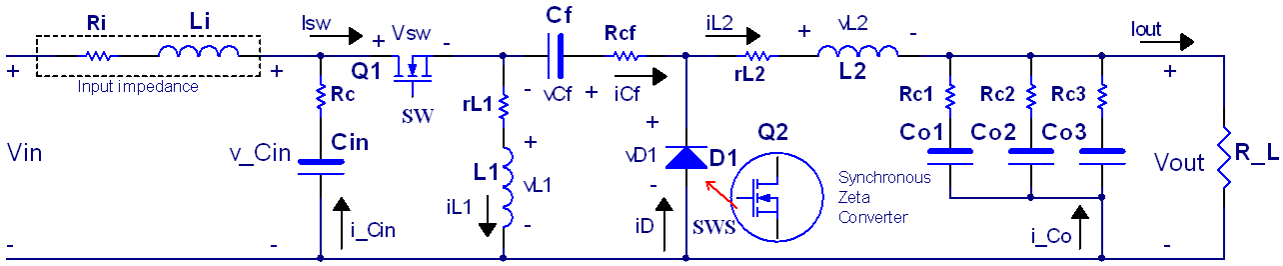
Zeta Converter

This converter, in its most basic form, similar to the sepic and Cuk converters is a fourth order converter with two inductors and an additional flying capacitor.

Input Pins:	**Vin**	Positive input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW	Main switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	SWS	Synchronous switch control (SW < 1 = OFF, SW ≥ 1 = ON).
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V). Since the zeta converter has a non-inverting configuration, the output voltage will be positive with a positive input voltage.
	Iout	Converter output current (A).
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered switch current for the case of the zeta converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vL1..2	Voltage across the inductors (V); vector, rows = 1, columns = 2.
	iL1..2	Current flowing through the inductor (A);vector, rows = 1, columns = 2.
	vCf	Flying Capacitor Voltage (V).
	iCf	Flying Capacitor Current (A).
	Vsw	Switch Voltage (V) – Positive for forward voltages.
	Isw	Switch Current (A) – Positive for forward current.
	Vd	Diode Voltage (V) - Positive for reverse voltages.
	Id	Diode Current (A) - Positive for forward current. The current through the zeta converter output diode / synchronous switch.

iCo	Output Capacitor Current (A)
vCin	Input capacitor Voltage (V) This will be the voltage charge on the input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.
iCin	Input capacitor current (A)
%Eff	Zeta converter Efficiency (%), averaged over a switching cycle.

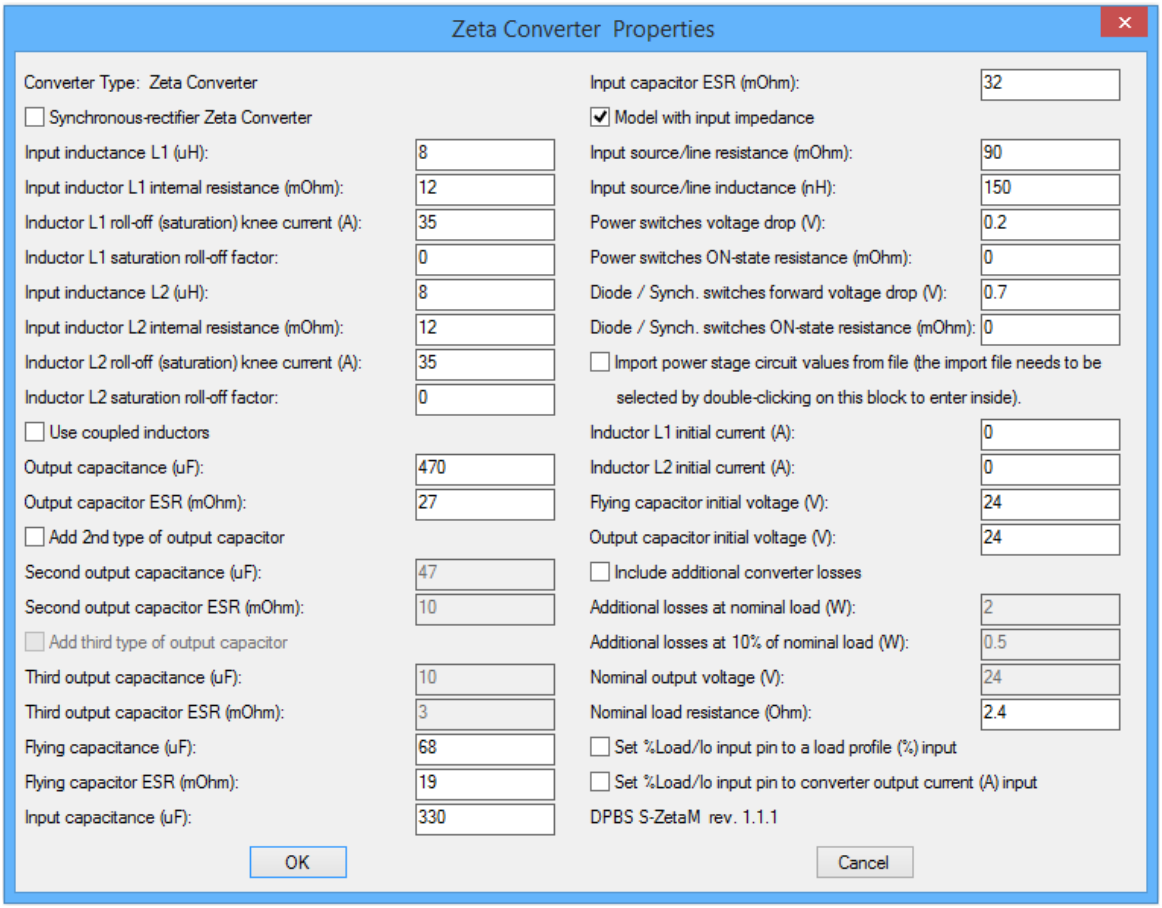
Circuit schematic: Zeta converter

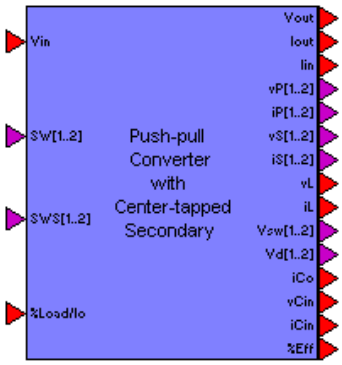


Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The dialog properties of the zeta converter are similar to the sepic converter.


Zeta Converter Properties
Converter Type: Zeta Converter
Synchronous-rectifier Zeta Converter
Input inductance L1 (uH): 8
Input inductor L1 internal resistance (mOhm): 12
Inductor L1 roll-off (saturation) knee current (A): 35
Inductor L1 saturation roll-off factor: 0
Input inductance L2 (uH): 8
Input inductor L2 internal resistance (mOhm): 12
Inductor L2 roll-off (saturation) knee current (A): 35
Inductor L2 saturation roll-off factor: 0
Use coupled inductors
Output capacitance (uF): 470
Output capacitor ESR (mOhm): 27
Add 2nd type of output capacitor
Second output capacitance (uF): 47
Second output capacitor ESR (mOhm): 10
Add third type of output capacitor
Third output capacitance (uF): 10
Third output capacitor ESR (mOhm): 3
Flying capacitance (uF): 68
Flying capacitor ESR (mOhm): 19
Input capacitance (uF): 330
OK
Input capacitor ESR (mOhm): 32
Model with input impedance
Input source/line resistance (mOhm): 90
Input source/line inductance (nH): 150
Power switches voltage drop (V): 0.2
Power switches ON-state resistance (mOhm): 0
Diode / Synch. switches forward voltage drop (V): 0.7
Diode / Synch. switches ON-state resistance (mOhm): 0
Import power stage circuit values from file (the import file needs to be selected by double-clicking on this block to enter inside).
Inductor L1 initial current (A): 0
Inductor L2 initial current (A): 0
Flying capacitor initial voltage (V): 24
Output capacitor initial voltage (V): 24
Include additional converter losses
Additional losses at nominal load (W): 2
Additional losses at 10% of nominal load (W): 0.5
Nominal output voltage (V): 24
Nominal load resistance (Ohm): 2.4
Set %Load/Io input pin to a load profile (%) input
Set %Load/Io input pin to converter output current (A) input
DPBS S-ZetaM rev. 1.1.1
Cancel



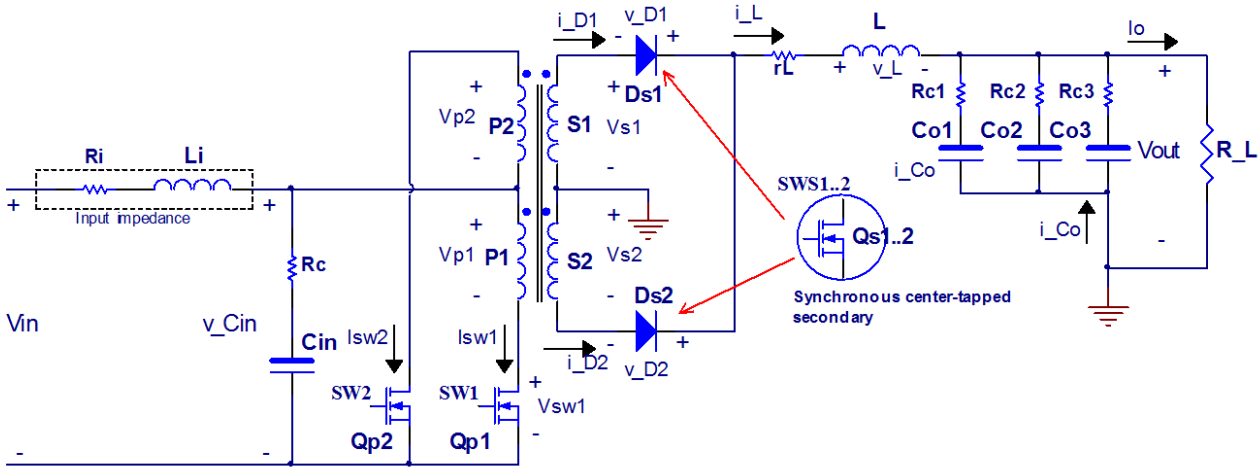
Push-Pull Converter (with centre-tapped secondary)

The push-pull converter is a buck-derived converter with electrical isolation between the input and output. The push-pull converter has two controlled switches on the centre-tapped primary side of the transformer. The centre-tapped secondary side has two controlled switches (synchronous converter) with a split secondary winding. The isolation is not directly represented here though the input and output voltages and currents are represented independently from each other. It can step-up or step-down the input voltage by appropriately setting the transformer turns ratio.

Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW[1..2]	Main switches control (SW < 1 = OFF, SW ≥ 1 = ON); vector rows = 1, columns = 2
	SWS[1..2]	Synchronous switches control (SW < 1 = OFF, SW ≥ 1 = ON) input vector.
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V)
	Iout	Converter output current (A)
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered sum of the primary winding currents for the case of the push-pull converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vP[1..2]	Voltage across the primary winding (V); vector rows = 1, columns = 2.
	iP[1..2]	Current through the primary winding (A); vector rows = 1, columns = 2.
	vS[1..2]	Voltage across the split secondary windings (V); vector rows = 1, columns = 2.
	iS[1..2]	Current through the split secondary windings (A); vector rows = 1, columns = 2. This is also the current through the output diodes / synchronous switches.
	vL	Voltage across the secondary side inductor (V)
	iL	Current flowing through the secondary side inductor (A)
	Vsw[1..2]	Switch Voltages (V) – Positive for forward voltages; vector rows = 1, columns = 2.
	Isw[1..2]	Switch Currents (A) – Positive for forward current; vector rows = 1, columns = 2.

Vd[1..2]	Diode Voltages (V) - Positive for reverse voltages; vector rows = 1, columns = 2.
	The voltage across the output diodes / synchronous switches.
iCo	Output Capacitor Current (A)
vCin	Input capacitor Voltage (V)
	This will be the voltage charge on input capacitor if the “model with input impedance” is selected, otherwise it will be directly the input voltage.
iCin	Input capacitor current (A)
%Eff	Converter Efficiency (%), averaged over a switching cycle.

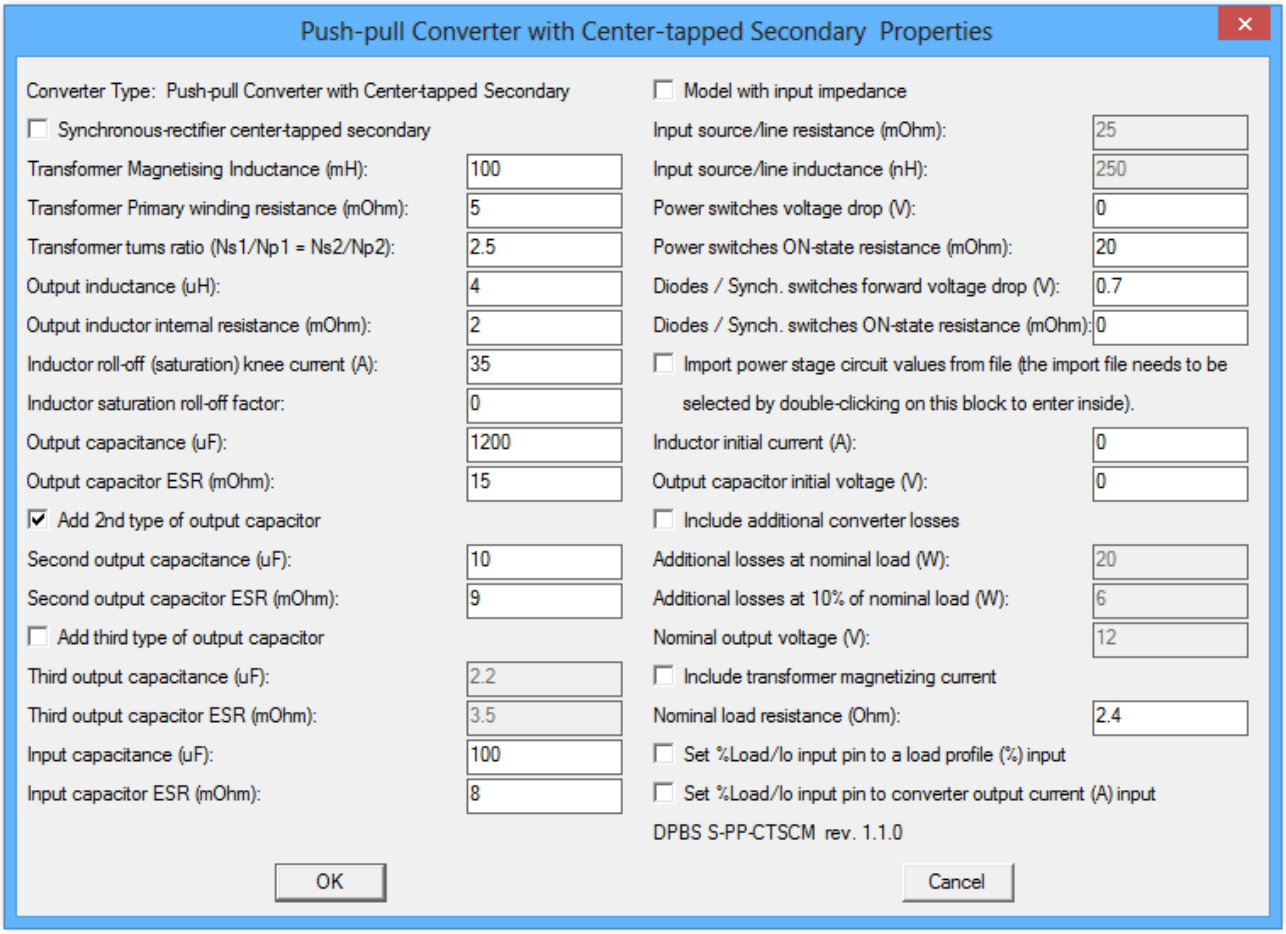
Circuit schematic: Push-pull Converter with centre-tapped secondary



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The push-pull converter properties menu is shown in the following box which appears when right-clicking on the block.



Synchronous-rectifier center-tapped secondary:

When this check box is activated the output diodes of the center-tapped secondary will be modelled as controllable switches (usually MOSFETs). This will activate the SWS vector input pin.

Add DC blocking capacitor in series with the primary winding:

Check this box if a capacitor in series with the primary winding is to be included in the model. This DC blocking capacitor is so called because it blocks the flow of DC currents in the primary winding of the transformer, preventing saturation. This capacitor is usually required in practise with voltage mode control. Simulations, however, may be performed without this capacitor since saturation of the primary winding is not modelled in the full-bridge converter block.

DC blocking capacitance:

Enter the value of the DC blocking capacitance in microfarads. Small values of capacitance could charge up quickly, robbing voltage from the primary winding and therefore reducing the transfer of energy capacity and increasing the duty cycle. Large values of capacitance will mean bulky and expensive components.

DC blocking capacitor parallel resistance:

Enter the value of the resistor in parallel to the blocking capacitor in Ohms. This resistor will allow discharging of any excessive charge on the blocking capacitor.

Transformer magnetizing inductance:

Enter the value of the transformer magnetizing inductance in milli-henries.

Transformer turns ratio (Ns1/Np = Ns2/Np):

Enter the turns ratio of the transformer N secondary divided by N primary.

Output inductance:

Enter the value of the push-pull converter output inductance in micro-Henrys.

Output inductor internal resistance:

The winding resistance of the buck inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if “Model with input impedance” is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to model the full-bridge converter with input impedance. This can also be used to model the effects of an input filter on the full-bridge converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switches voltage drop:

The forward voltage drop, in Volts, across the main switches of the push-pull converter can be entered. This value will provide a fixed forward ON-state voltage

regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch.

Power switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diode / Synch. Switches forward voltage drop:

The forward voltage drop, in Volts, across the diode / synchronous switch (in the case of a synchronous-rectifier converter) of the push-pull converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

Diode / Synch. Switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file.
The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Initial inductor current:

The initial inductor current (at simulation start) can be entered here in Amperes.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Since the converter duty cycle is a function of the efficiency, the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced when this box is checked.

Additional losses at nominal load:

Insert the additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load.

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Include transformer magnetizing current:

Check this box to include the transformer magnetizing inductance in the model. This effect may not always be necessary in the model for control purposes and can therefore be excluded, eliminating the magnetizing current component. Note that for small values of magnetizing inductance, this component should not be ignored.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

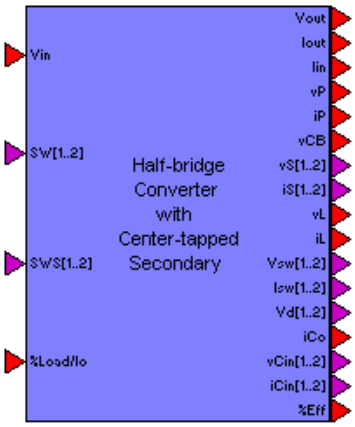
Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

Contents - Simulation



Half-bridge Converter (with center-tapped secondary)

The half-bridge converter is a buck-derived converter with electrical isolation between the input and output. The half-bridge converter has two controlled switches on the primary side of the transformer with a split input capacitor configuration. The centre-tapped secondary side has two controlled switches (synchronous converter) with a split secondary winding. The isolation is not directly represented here though the input and output voltages and currents are represented independently from each other. It can step-up or step-down the input voltage by appropriately setting the transformer turns ratio.

Input Pins:

Vin Input voltage (V)

This is usually connected from a source block or it can be the output of another converter.

SW[1..2] Main switches control (SW < 1 = OFF, SW ≥ 1 = ON); vector rows = 1, columns = 2

SWS[1..2] Synchronous switches control (SW < 1 = OFF, SW ≥ 1 = ON) input vector.

%Load/Io Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog.

This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.

Output Pins:

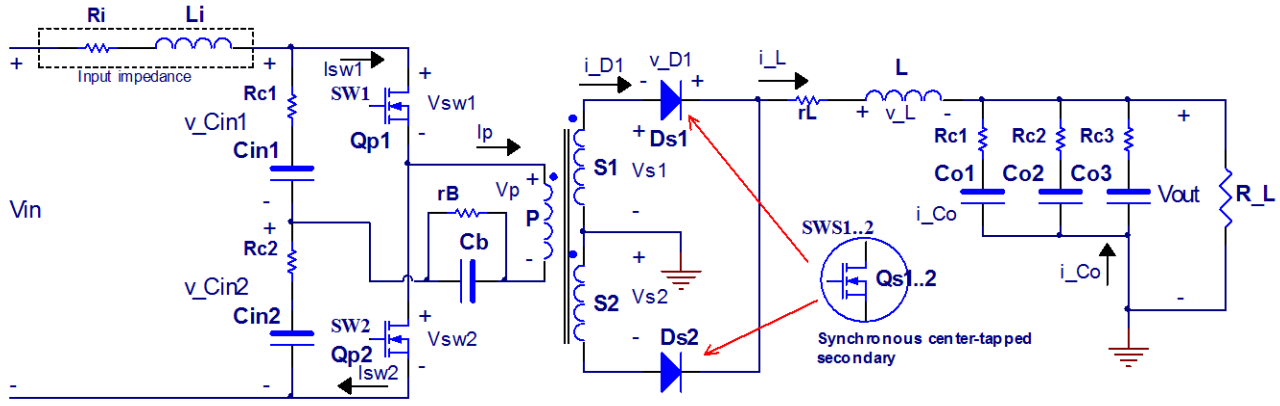
Vout Converter output voltage (V)

Iout Converter output current (A)

Iin Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered sum of the switch currents for the case of the half-bridge converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.

vP	Voltage across the primary winding (V)
iP	Current through the primary winding (A)
vCB	Voltage across the DC blocking capacitor Cb (V)
vS[1..2]	Voltage across the split secondary windings (V); vector rows = 1, columns = 2.
iS[1..2]	Current through the split secondary windings (A); vector rows = 1, columns = 2.
	This is also the current through the output diodes / synchronous switches.
vL	Voltage across the secondary side inductor (V)
iL	Current flowing through the secondary side inductor (A)
Vsw[1..2]	Switch Voltages (V) – Positive for forward voltages; vector rows = 1, columns = 2.
Isw[1..2]	Switch Currents (A) – Positive for forward current; vector rows = 1, columns = 2.
Vd[1..2]	Diode Voltages (V) - Positive for reverse voltages; vector rows = 1, columns = 2.
	The voltage across the output diodes / synchronous switches.
iCo	Output Capacitor Current (A)
vCin	Input capacitor Voltage (V)
	This will be the voltage charge on input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.
iCin	Input capacitor current (A)
%Eff	Converter Efficiency (%), averaged over a switching cycle.

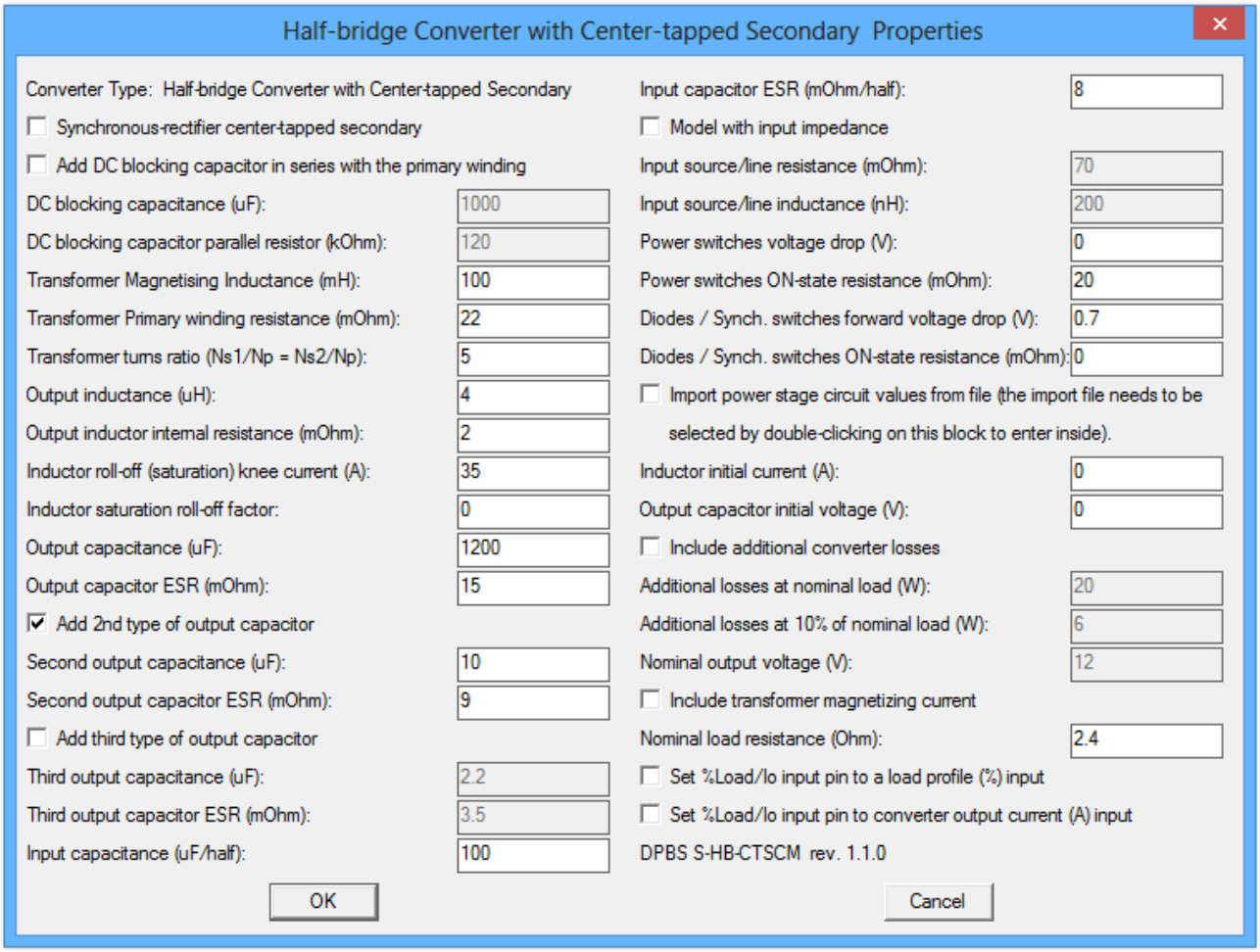
Circuit schematic: Half-bridge Converter with centre-tapped secondary



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The half-bridge converter properties menu is shown in the following box which appears when right-clicking on the block.



Synchronous-rectifier center-tapped secondary:

When this check box is activated the output diodes of the center-tapped secondary will be modelled as controllable switches (usually MOSFETs). This will activate the SWS vector input pin.

Add DC blocking capacitor in series with the primary winding:

Check this box if a capacitor in series with the primary winding is to be included in the model. This DC blocking capacitor is so called because it blocks the flow of DC currents in the primary winding of the transformer, preventing saturation. This capacitor is usually required in practise with voltage mode control. Simulations, however, may be performed without this capacitor since saturation of the primary winding is not modelled in the full-bridge converter block.

DC blocking capacitance:

Enter the value of the DC blocking capacitance in microfarads. Small values of capacitance could charge up quickly, robbing voltage from the primary winding and therefore reducing the transfer of energy capacity and increasing the duty cycle. Large values of capacitance will mean bulky and expensive components.

DC blocking capacitor parallel resistance:

Enter the value of the resistor in parallel to the blocking capacitor in Ohms. This resistor will allow discharging of any excessive charge on the blocking capacitor.

Transformer magnetizing inductance:

Enter the value of the transformer magnetizing inductance in milli-henries.

Transformer turns ratio (Ns1/Np = Ns2/Np):

Enter the turns ratio of the transformer N secondary divided by N primary.

Output inductance:

Enter the value of the half-bridge converter output inductance in micro-Henries.

Output inductor internal resistance:

The winding resistance of the half-bridge output inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if “Model with input impedance” is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to model the full-bridge converter with input impedance. This can also be used to model the effects of an input filter on the full-bridge converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switches voltage drop:

The forward voltage drop, in Volts, across the main switch of the half-bridge converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch.

Power switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diode / Synch. Switches forward voltage drop:

The forward voltage drop, in Volts, across the diodes / synchronous switches (in the case of a synchronous-rectifier converter) of the half-bridge converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diodes.

Diode / Synch. Switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifiers are MOSFET switches, the forward voltage across the diodes (switches) will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file.
The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Initial inductor current:

The initial inductor current (at simulation start) can be entered here in Amperes.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Similar to the buck converter, since the converter duty cycle is a function of the efficiency, the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced when this box is checked.

Additional losses at nominal load:

Insert the additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load.

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Include transformer magnetizing current:

Check this box to include the transformer magnetizing inductance in the model. This effect may not always be necessary in the model for control purposes and can therefore be excluded, eliminating the magnetizing current component. Note that for small values of magnetizing inductance, this component should not be ignored.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

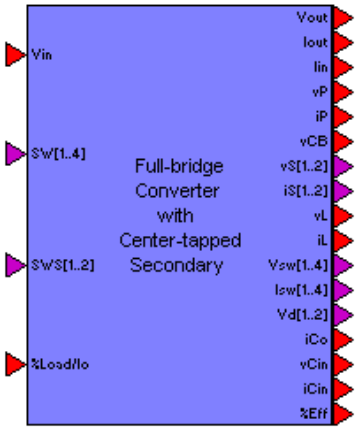
Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

Contents - Simulation



Full-bridge Converter (with center-tapped secondary)

The full-bridge converter is a buck-derived converter with electrical isolation between the input and output. The full-bridge converter has four controlled switches on the primary side of the transformer. The centre-tapped secondary side has two controlled switches (synchronous converter) with a split secondary winding. The isolation is not directly represented here though the input and output voltages and currents are represented independently from each other. It can step-up or step-down the input voltage by appropriately setting the transformer turns ratio.

Input Pins:

Vin Input voltage (V)

This is usually connected from a source block or it can be the output of another converter.

SW[1..4] Main switches control (SW < 1 = OFF, SW ≥ 1 = ON); vector rows = 1, columns = 4

SWS[1..2] Synchronous switches control (SW < 1 = OFF, SW ≥ 1 = ON) input vector.

%Load/Io Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog.

This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.

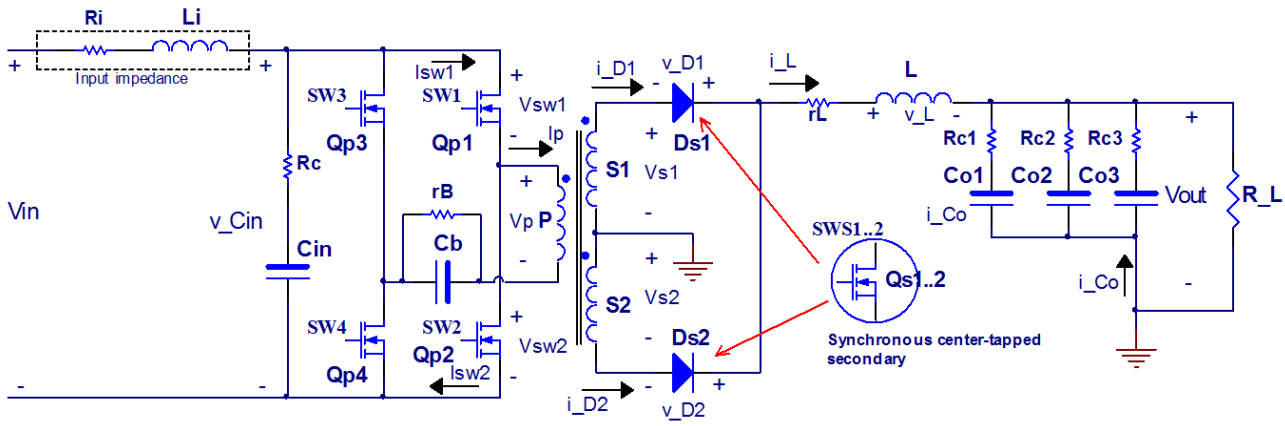
Output Pins:

Vout Converter output voltage (V)

Iout Converter output current (A)

Iin	Converter input current (A). If “model with input impedance” is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered sum of the top switch currents for the case of the full-bridge converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
vP	Voltage across the primary winding (V)
iP	Current through the primary winding (A)
vCB	Voltage across the DC blocking capacitor Cb (V)
vS[1..2]	Voltage across the split secondary windings (V); vector rows = 1, columns = 2.
iS[1..2]	Current through the split secondary windings (A); vector rows = 1, columns = 2. This is also the current through the output diodes / synchronous switches.
vL	Voltage across the secondary side inductor (V)
iL	Current flowing through the secondary side inductor (A)
Vsw[1..4]	Switch Voltages (V) – Positive for forward voltages; vector rows = 1, columns = 4.
Isw[1..4]	Switch Currents (A) – Positive for forward current; vector rows = 1, columns = 4.
Vd[1..2]	Diode Voltages (V) - Positive for reverse voltages; vector rows = 1, columns = 2. The voltage across the output diodes / synchronous switches.
iCo	Output Capacitor Current (A)
vCin	Input capacitor Voltage (V) This will be the voltage charge on input capacitor if the “model with input impedance” is selected, otherwise it will be directly the input voltage.
iCin	Input capacitor current (A)
%Eff	Converter Efficiency (%), averaged over a switching cycle. The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switches and diodes / synchronous switches conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR). The switching losses and diode reverse recovery losses along with the inductor core losses are not included in the model.

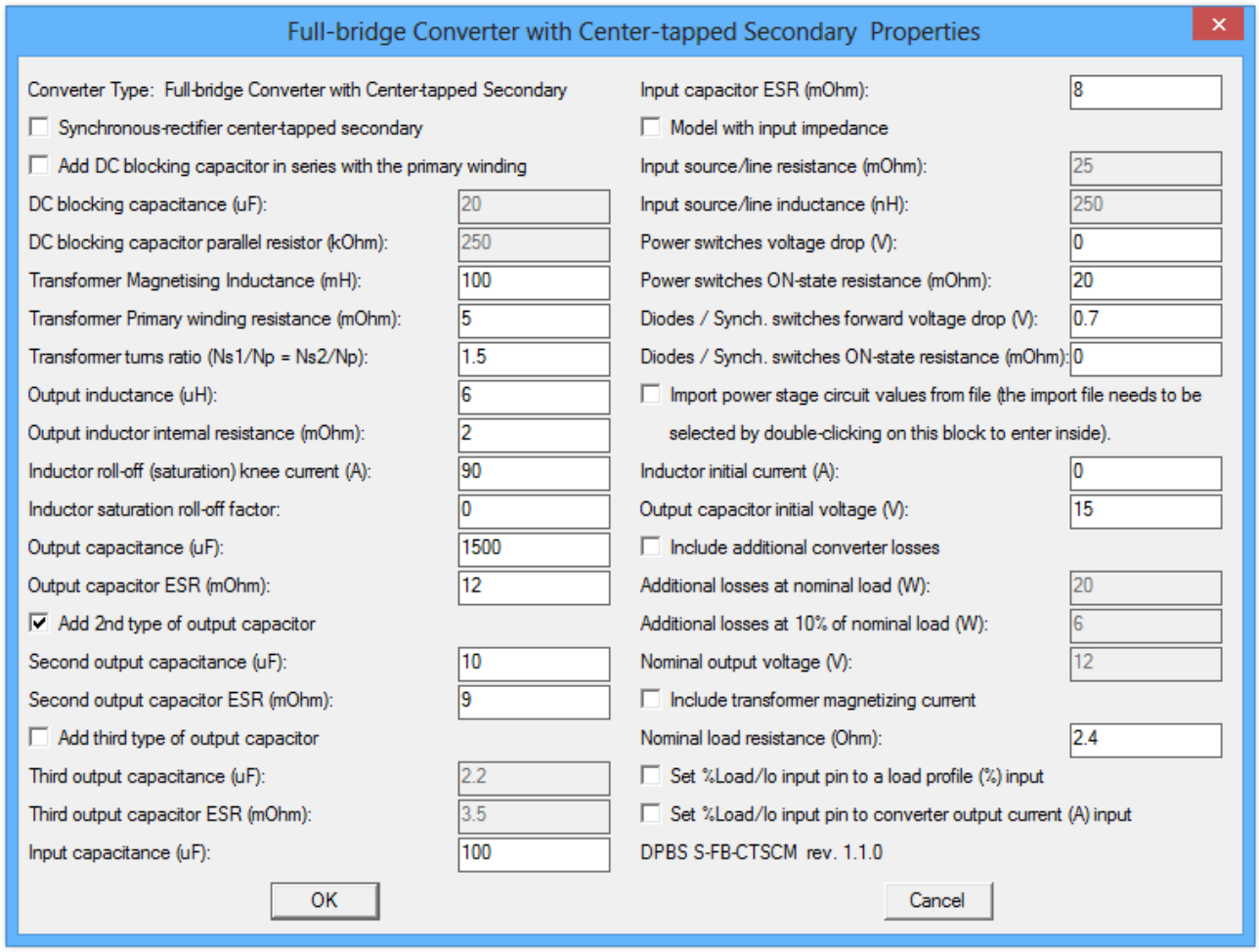
Circuit schematic: Full-bridge Converter with center-tapped secondary



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The full-bridge converter properties menu is shown in the following box which appears when right-clicking on the block.



Synchronous-rectifier center-tapped secondary:

When this check box is activated the output diodes of the center-tapped secondary will be modelled as controllable switches (usually MOSFETs). This will activate the SWS vector input pin.

Add DC blocking capacitor in series with the primary winding:

Check this box if a capacitor in series with the primary winding is to be included in the model. This DC blocking capacitor is so called because it blocks the flow of DC currents in the primary winding of the transformer, preventing saturation. This capacitor is usually required in practise with voltage mode control. Simulations, however, may be performed without this capacitor since saturation of the primary winding is not modelled in the full-bridge converter block.

DC blocking capacitance:

Enter the value of the DC blocking capacitance in microfarads. Small values of capacitance could charge up quickly, robbing voltage from the primary winding and therefore reducing the transfer of energy capacity and increasing the duty cycle. Large values of capacitance will mean bulky and expensive components.

DC blocking capacitor parallel resistance:

Enter the value of the resistor in parallel to the blocking capacitor in Ohms. This resistor will allow discharging of any excessive charge on the blocking capacitor.

Transformer magnetizing inductance:

Enter the value of the transformer magnetizing inductance in milli-henries.

Transformer turns ratio (Ns1/Np = Ns2/Np):

Enter the turns ratio of the transformer N secondary divided by N primary.

Output inductance:

Enter the value of the full-bridge converter output inductance in micro-Henrys.

Output inductor internal resistance:

The winding resistance of the full-bridge output inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if "Model with input impedance" is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to model the full-bridge converter with input impedance. This can also be used to model the effects of an input filter on the full-bridge converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switch voltage drop:

The forward voltage drop, in Volts, across the main switches of the full-bridge converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch.

Power switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Diode / Synch. Switch forward voltage drop:

The forward voltage drop, in Volts, across the diodes / synchronous switches (in the case of a synchronous-rectifier converter) of the full-bridge converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

Diode / Synch. Switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifiers are MOSFET switches, the forward voltage across the diodes (switches) will depend only on this value when the switches are in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switches are not controlled.

Import power stage circuit values from file:

The power component values can be directly read from a file.
The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Initial inductor current:

The initial inductor current (at simulation start) can be entered here in Amperes.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Similar to the forward converter, since the converter duty cycle is a function of the efficiency, the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced when this box is checked.

Additional losses at nominal load:

Insert the additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load.

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Include transformer magnetizing current:

Check this box to include the transformer magnetizing inductance in the model. This effect may not always be necessary in the model for control purposes and can therefore be excluded, eliminating the magnetizing current component. Note that for small values of magnetizing inductance, this component should not be ignored.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

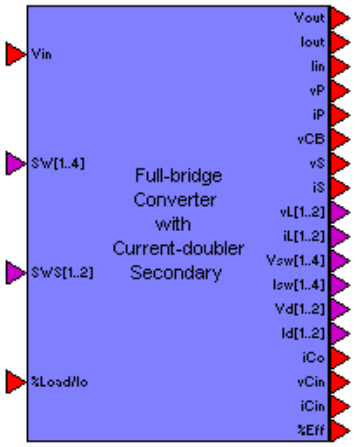
Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

Contents - Simulation



Full-bridge Converter (with current-doubler secondary)

The full-bridge converter is a buck-derived converter with electrical isolation between the input and output. This full-bridge converter has four controlled switches on the primary side of the transformer and four uncontrolled diode switches on the secondary side of the transformer. The transformer of this converter has a single secondary winding. This secondary configuration has 2 inductors and could have applications for high currents at lower output voltages. This converter is included as a comparison only to the center-tapped and full-bridge secondary configurations of the full-bridge converter.

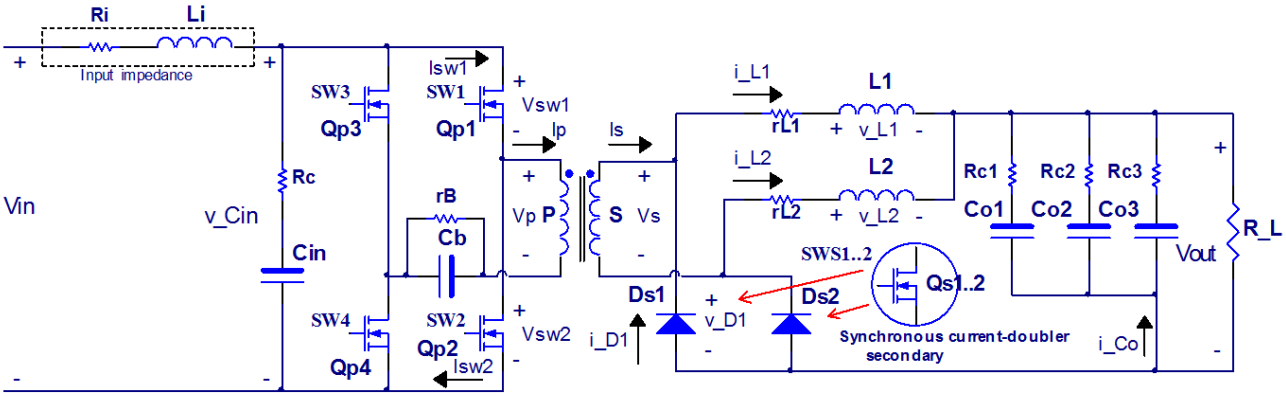
Input Pins:	**Vin**	Input voltage (V)
	SW[1..4]	Main switches control (SW < 1 = OFF, SW ≥ 1 = ON); vector rows = 1, columns = 4
	SWS[1..2]	Synchronous switches control (SW < 1 = OFF, SW ≥ 1 = ON); vector rows = 1, columns = 2.
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V).
	Iout	Converter output current (A).
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered sum of the top switch currents for the case of the full-bridge converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vP	Voltage across the primary winding (V)
	iP	Current through the primary winding (A)
	vCB	Voltage across the DC blocking capacitor Cb (V)
	vS	Voltage across the secondary winding (V).
	iS	Current through the secondary winding (A).
	vL[1..2]	Voltage across the secondary side inductors (V); vector, rows = 1, columns = 2.
	iL[1..2]	Current flowing through the secondary side inductors (A); vector, rows = 1, columns = 2.
	Vsw[1..4]	Switch Voltages (V) – Positive for forward voltages; vector rows = 1, columns = 4.
	Isw[1..4]	Switch Currents (A) – Positive for forward current; vector rows = 1, columns = 4.

Vd[1..2]	Diode / Sync switch Voltages (V) - Positive for reverse voltages; vector rows = 1, columns = 2.
Id[1..2]	Diode / synch switch currents (A) - Positive for forward currents; vector rows = 1, columns = 2.
iCo	Output Capacitor Current (A)
vCin	Input capacitor Voltage (V) This will be the voltage charge on input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.
iCin	Input capacitor current (A)
%Eff	Converter Efficiency (%), averaged over a switching cycle.

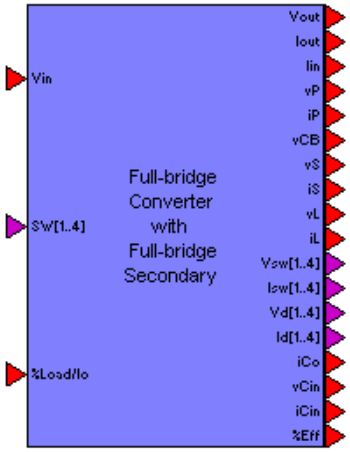
Dialog properties:

The dialog and features are similar to the full-bridge converter with centre-tapped secondary.

Circuit schematic: Full-bridge Converter with current-doubler secondary



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.



Full-bridge Converter (with full-bridge secondary)

The full-bridge converter is a buck-derived converter with electrical isolation between the input and output. This full-bridge converter has four controlled switches on the primary side of the transformer and four uncontrolled diode switches on the secondary side of the transformer. The transformer has a single secondary winding. This converter is not synchronous as there are always two diodes in series conducting on the secondary side and a synchronous converter is not practical for this case. This converter would normally be applied with higher voltages and power ratings compared to the centre-tapped version.

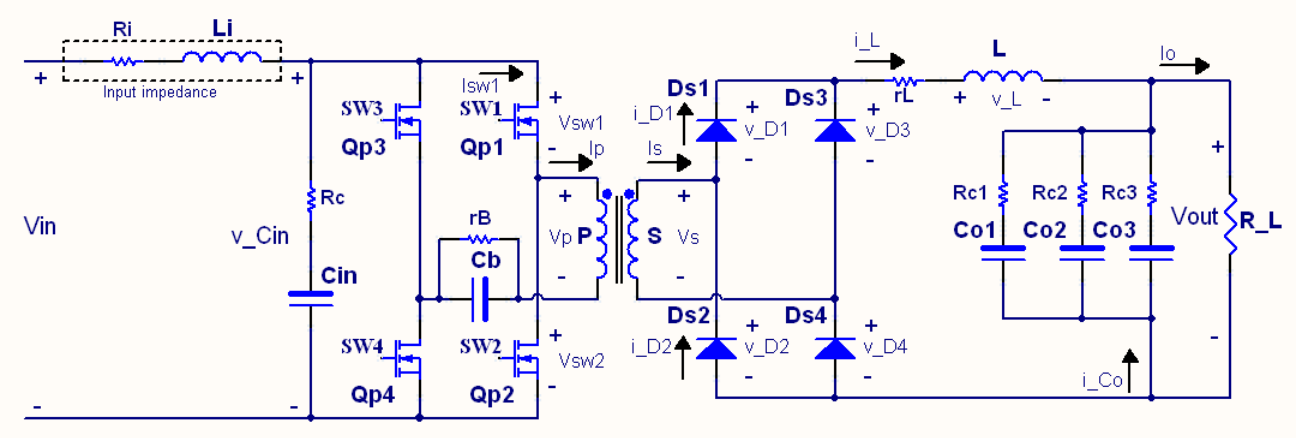
Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW[1..4]	Main switches control (SW < 1 = OFF, SW ≥ 1 = ON); vector, rows = 1, columns = 4.
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V).
	Iout	Converter output current (A).
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered sum of the top switch currents for the case of the full-bridge converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	vP	Voltage across the primary winding (V)
	iP	Current through the primary winding (A)
	vCB	Voltage across the DC blocking capacitor Cb (V)
	vS	Voltage across the secondary winding (V).
	iS	Current through the secondary winding (A).
	vL	Voltage across the secondary side inductor (V)
	iL	Current flowing through the secondary side inductor (A)
	Vsw[1..4]	Switch Voltages (V) – Positive for forward voltages; vector rows = 1, columns = 4.
	Isw[1..4]	Switch Currents (A) – Positive for forward current; vector rows = 1, columns = 4.
	Vd[1..4]	Diode Voltages (V) - Positive for reverse voltages; vector rows = 1, columns = 4.

Id[1..4]	Diode currents (A) - Positive for forward currents; vector rows = 1, columns = 4.
iCo	Output Capacitor Current (A)
vCin	Input capacitor Voltage (V) This will be the voltage charge on input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.
iCin	Input capacitor current (A)
%Eff	Converter Efficiency (%), averaged over a switching cycle.

Dialog properties:

The dialog and features are similar to the full-bridge converter with centre-tapped secondary.

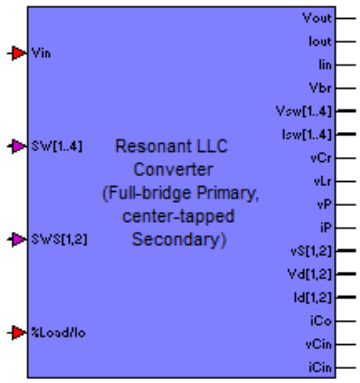
Circuit schematic: Full-bridge Converter with full-bridge secondary



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Contents - Simulation

Power Converter Blocks – Resonant Converters (DC-DC)

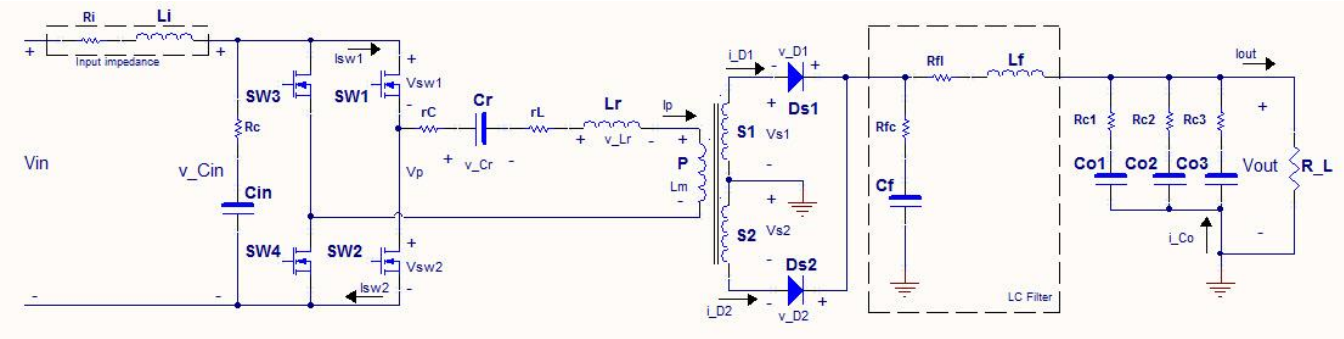


Resonant LLC Converter (FBP-CTS)

This block is a model of the resonant LLC converter with a full-bridge primary stage and a center-tapped secondary stage. The converter consists of a series resonant inductor-inductor-capacitor (LLC) resonant tank in the primary of the high-frequency isolation transformer.

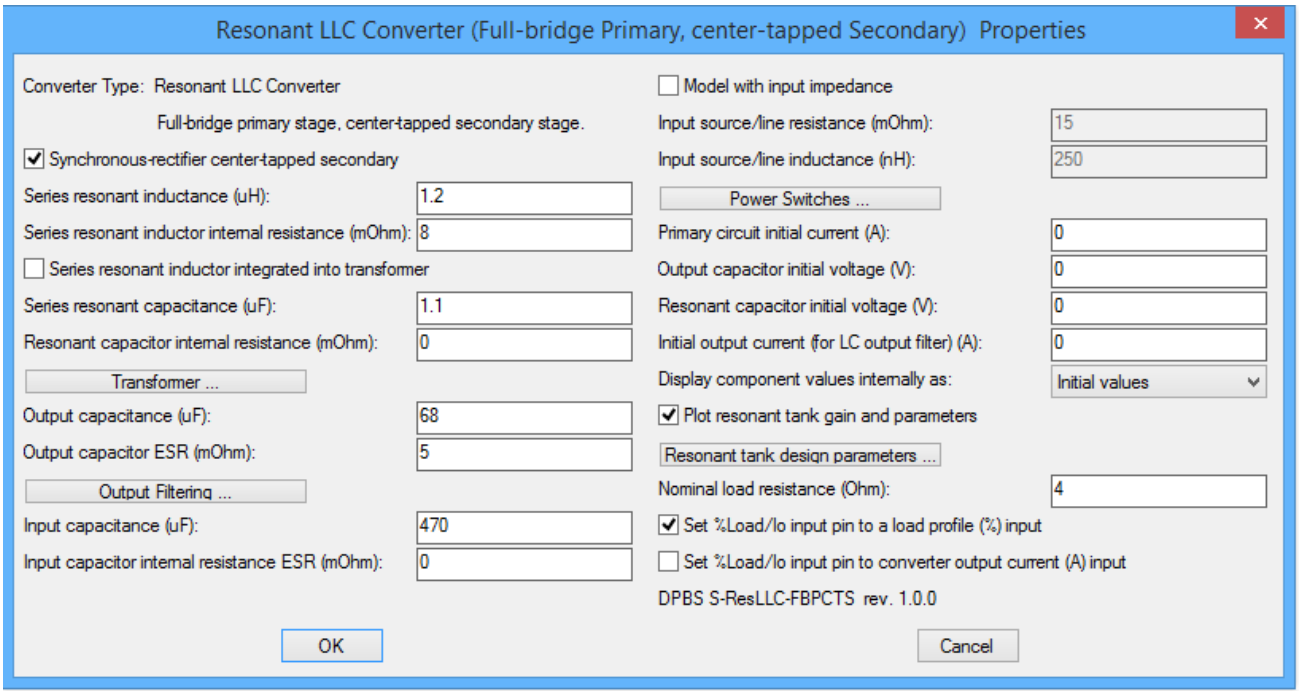
Input Pins:	**Vin**	The input AC voltage of the rectifier (V)
	SW[1..4]	Main switch control inputs of the full-bridge primary input stage.
	SWS[1..2]	Synchronous switch control inputs of the center-tapped secondary stage (when enabled).
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog.
Output Pins:	**Vout**	The converter output voltage of the rectifier (V).
	Iout	The converter output current in Amperes.
	Iin	The input current drawn by the converter in Amperes.
	Vsw[1..4]	The voltage across the four primary stage switches.
	Isw[1..4]	The current through the four primary stage switches.
	vCr	The voltage across the resonant tank capacitor.
	vLr	The voltage appearing across the resonant tank inductor (V).
	vP	The voltage across the transformer primary winding.
	iP	The current through the primary winding (and resonant tank circuit).
	vS[1,2]	The voltage across the transformer secondary windings.
	Vd[1,2]	The voltage across the secondary stage diodes / synchronous switches.
	Id[1,2]	The current through the secondary stage diodes / synchronous switches.
	iCo	The current in the output capacitor in Amperes.
	vCin	The input capacitor voltage.
	iCin	The input capacitor current.

Circuit schematic: Resonant LLC Converter (non-synchronous secondary)



Dialog properties:

The resonant LLC converter block properties menu is shown in the following figure which appears when right-clicking on the block.



Synchronous-rectifier center-tapped secondary:

When this check box is activated the output diodes of the resonant LLC converter will be modelled as a controllable switch (usually a MOSFET). This will activate the SWS input vector pin.

Series resonant inductance:

Enter the value of the series resonant inductance in micro-Henrys.

Series resonant internal resistance:

The winding resistance of the resonant inductor should be given here in milli-Ohms.

Series resonant inductor integrated into transformer:

Select if the only series resonant inductance is that integrated into the transformer parameters. The above series resonant inductance will be ignored in this case.

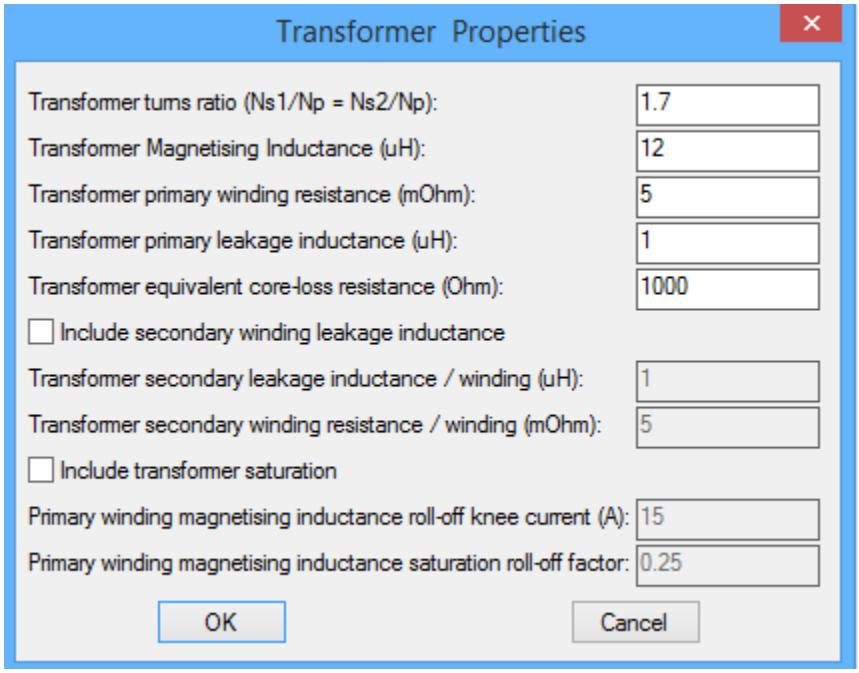
Series resonant capacitance:

Insert the value of the series resonant capacitor in micro-Farads.

Series resonant capacitor internal resistance:

The equivalent series resistance (ESR) of the series resonant capacitor should be given here in milli-Ohms.

Transformer:



Transformer turns ratio (Ns1/Np = Ns2/Np):

Enter the turns ratio of the transformer Ns (secondary) divided by Np (primary). The turns ratio of the 2 secondary windings are identical.

Transformer magnetising inductance:

Enter the value of the transformer magnetising inductance in micro-Henrys. This value forms part of the resonant tank circuit.

Primary winding internal resistance:

Enter the winding resistance of the primary winding in milli-Ohms. The resistance of any connections can be summed into the given value.

Primary winding leakage inductance:

Enter the leakage inductance value of the transformer primary winding. This value will be used as part of the resonant tank circuit regardless of whether the series resonant inductor is integrated in the resonant circuit or not.

Transformer equivalent core-loss resistance:

Enter the value of the effective primary winding parallel resistance modelling the core-loss of the transformer.

Include secondary winding leakage inductance:

Select this to model with secondary winding leakage inductance.

Secondary winding leakage inductance:

Enter the leakage inductance value of each of the transformer secondary windings (assumed to be equal since the turns ratios are equal).

Secondary winding internal resistance:

Enter the winding resistance of the secondary winding in milli-Ohms.

Include transformer saturation:

Select this if saturation effects of the primary winding are to be modelled.

Primary winding saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Primary winding roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

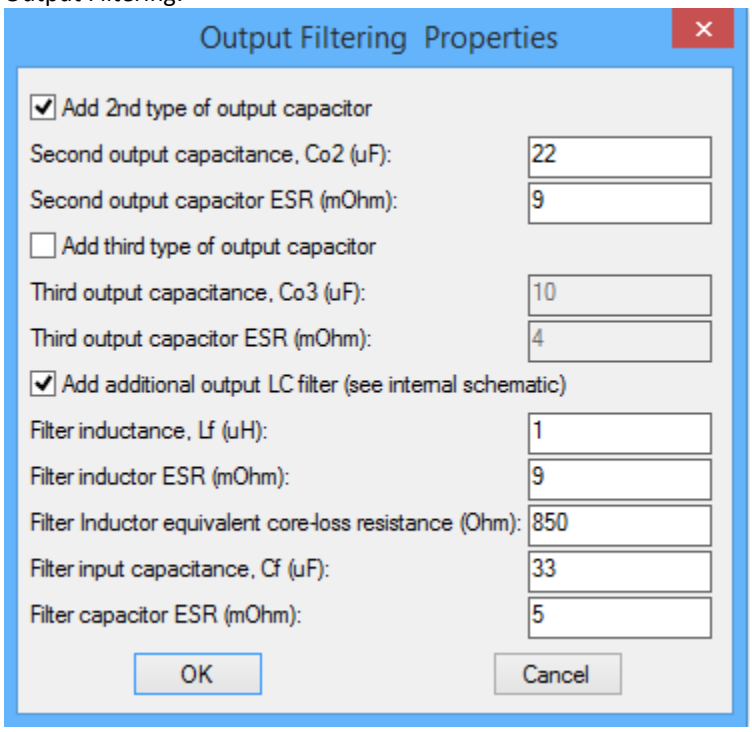
Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Output Filtering:



Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value to the main output capacitor) which is connected in parallel with the main capacitor, can be included in the model.

Add 3rd type of output capacitor:

A third type of output capacitor maybe included.

Add additional LC filter:

An additional LC filter can be added to the output filter of the converter if this is selected here. The additional elements are as indicated in the circuit schematic above.

Filter Inductance:

Enter the value of the inductance of the LC filter inductor in micro-Henrys.

Filter Inductor ESR:

Enter the value of the equivalent series resistance of the LC filter inductor in milli-Ohms.

Filter inductor equivalent core-loss resistance:

Enter the value of the effective filter inductor parallel resistance modelling the core-loss of the inductor.

Filter input capacitance, Cf:

Enter the value of the LC filter capacitance (before the inductor) in micro-Farads.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the LC filter capacitor in milli-Ohms.

Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if “Model with input impedance” is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to model the buck converter with input impedance. This can also be used to model the effects of an input filter on the buck converter.

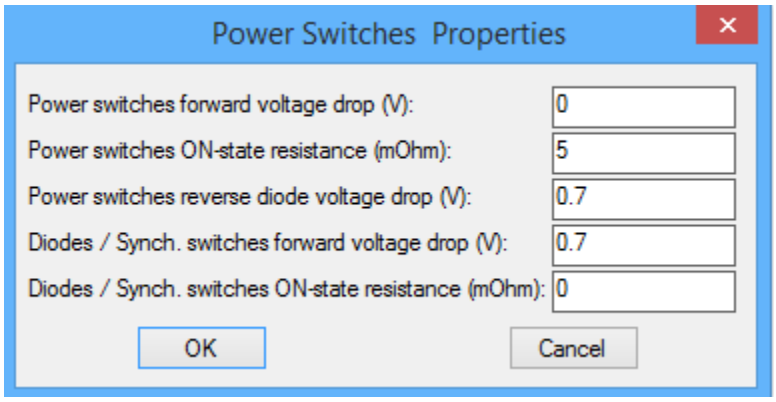
Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switches:



Power switches voltage drop:

The forward voltage drop, in Volts, across the primary switches can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch.

Power switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the primary switches can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switches such as with MOSFETs.

Power switches reverse drop:

The reverse voltage drop, in Volts, across the primary switches. This parameter is relevant particularly in synchronous converters when the current through the primary switches can reverse and is returned to the source.

Diode / Synch. Switch forward voltage drop:

The forward voltage drop, in Volts, across the diode / synchronous switches (in the case of a synchronous-rectifier secondary) can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode.

Diode / Synch. Switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the synchronous switch can be entered. In the case of synchronous converters where the synchronous rectifier is a MOSFET switch, the forward voltage across the diode will depend only on this value when the switch is in the on-state (the SWS control ≥ 1), otherwise it will depend upon the forward voltage drop only if forward biased and the switch is not controlled.

Primary circuit initial current:

The initial current (at simulation start) of the primary series circuit can be entered here in Amperes.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

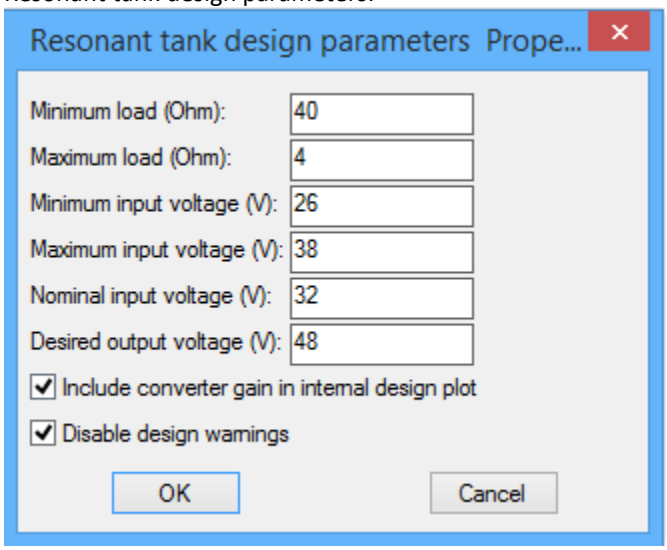
Resonant capacitor initial voltage:

The initial voltage of the resonant capacitor (at simulation start) can be entered here in Volts.

Initial output current:

The initial output current of the optional LC filter inductor can be entered here in Amperes when the optional output filter is selected.

Resonant tank design parameters:



Minimum load:
: Enter the expected minimum designed load in ohms.

Maximum load:
: Enter the expected maximum designed load in ohms.

Minimum input voltage:
: Enter the required designed minimum input voltage in Volts.

Maximum input voltage:
: Enter the required designed maximum input voltage in Volts.

Nominal input voltage:
: Enter the required nominal input voltage in Volts.

Desired output voltage:
: Enter the required nominal output voltage in Volts.

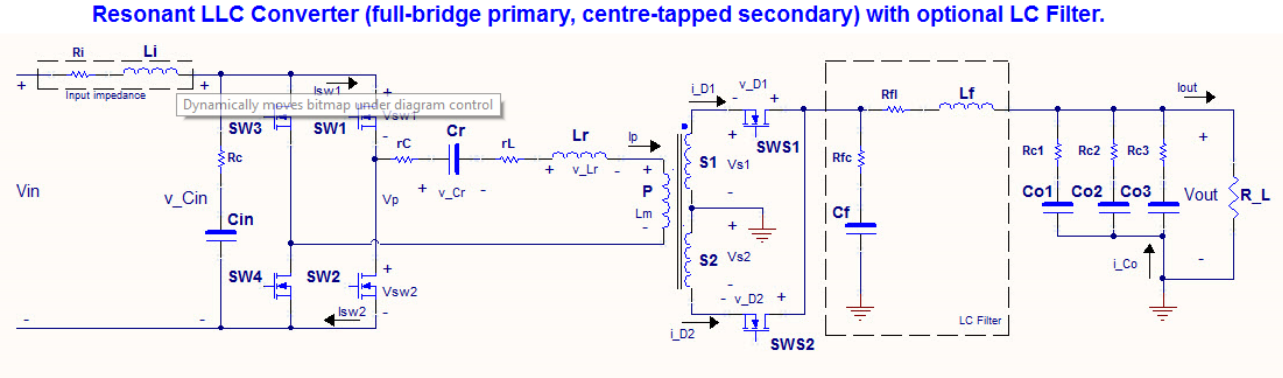
Include converter gain in internal design plot:
: If selected, the gain of the converter will be considered in the resonant tank gain plot otherwise the gain plot will be normalised at unity at the resonant frequency.

Disable design warnings:
: Select this to disable any design warnings.

Nominal load resistance:
: The nominal (full-load) load resistance must be given here in Ohms.

Set %Load/Io input pin to a load profile (%) input:
: Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:
: Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

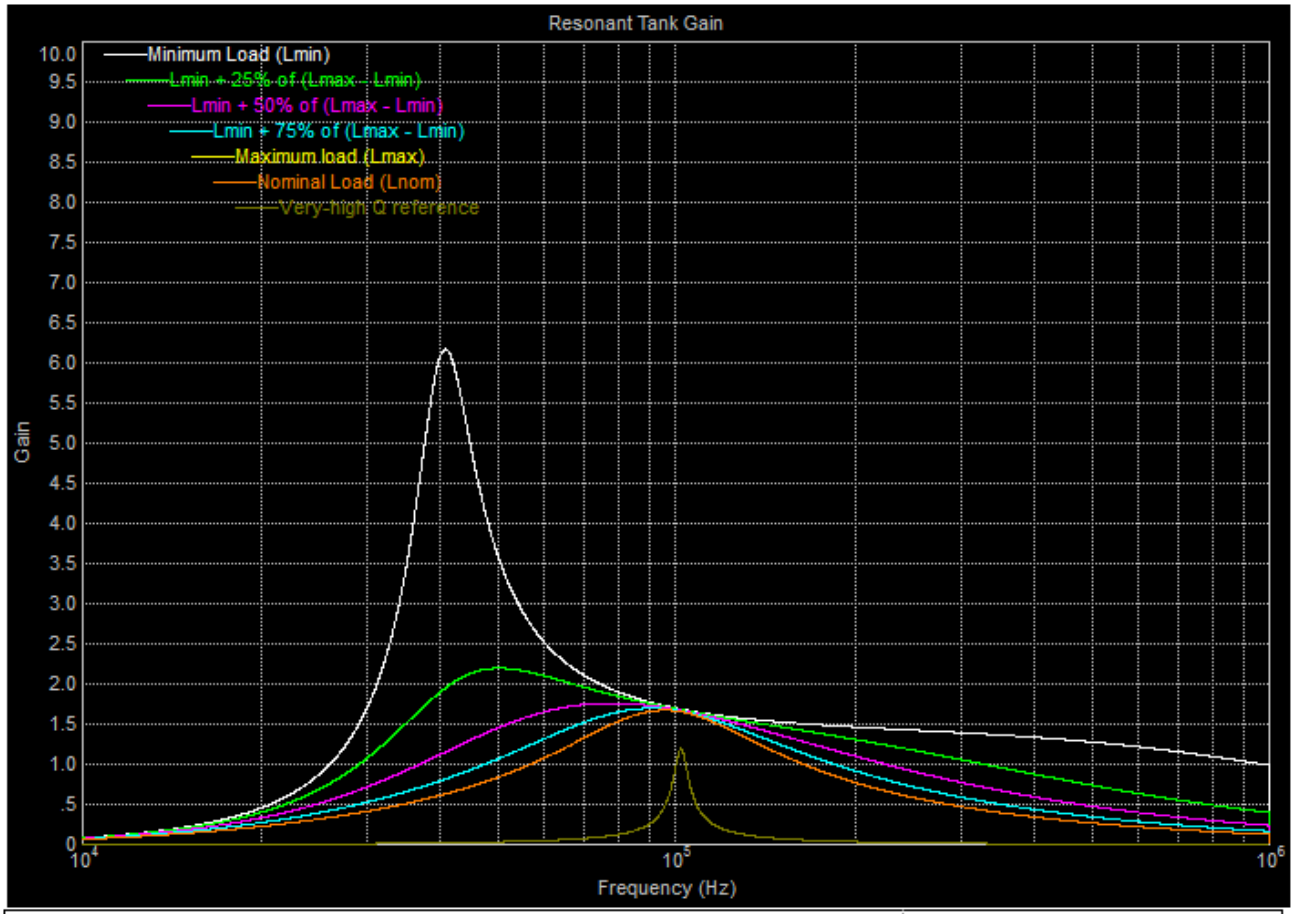


Component Value Display

Component	Value
File	Dialog values
Ri (mOhm)	N/A
Li (uH)	N/A
Cin (uF)	470.0000
Cin-esr, Rc (mOhm)	.0000
Magnetising inductance, Lm (uH)	12.0000
Rw, primary winding (mOhm)	5.0000
Leakage inductance primary (uH)	14.2000
Turns ratio n = Ns1/Np = Ns2/Np	1.7000
Rw, secondary winding (mOhm)	N/A
Leakage inductance secondary (uH)	N/A
Resonant capacitor, Cr (uF)	1.1000
Cr-esr, rC (mOhm)	.0000
Resonant inductor, Lr (uH)	.0000
Lr-esr, rL (mOhm)	8.0000
Co1 (uF)	68.0000
Rc1 (mOhm)	5.0000
Co2 (uF)	22
Rc2 (mOhm)	9
Co3 (uF)	N/A
Rc3 (mOhm)	N/A
Primary switches VswON (V)	.0000
Primary switches RswON (mOhm)	5.0000
Secondary diodes VdON (V)	.7000
Secondary diodes RdON (mOhm)	.0000
Output Filter Inductance, Lf (uH)	N/A
Output Filter Inductor ESR (mOhm)	N/A
Output Filter Capactance, Cf (uF)	N/A
Output Filter Capacitor ESR (mOhm)	N/A
Load R_L (Ohm)	4.0000

Resonant Tank Parameters

Internal view of the resonant LLC converter showing the current circuit schematic, the components selected and the internal compound block for the resonant tank design parameters display.

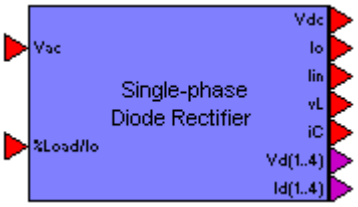


Design Parameter	Value
Resonant frequency, Fr (kHz)	102.3087
Converter Gain at Fr and nom. load	1.6658
Required Fsw at Vin nom. and nom. load, Fnom (kHz)	118.9842
Converter gain at Fnom	1.4995
Min. design Fsw at max. load, Fmin (kHz)	95.9821
Converter gain at Fmin	1.6849
Fsw at Vin max. and min. load, Fmax (kHz)	548.3813
Converter gain at Fmax	1.2620
Rac - reflected to prim. at min. load (Ohm)	11.2190
Rac - reflected to prim. at max. load (Ohm)	1.1219
Quality Factor, Q at min. load	.1261
Quality Factor, Q at max. load	1.2606
m = Lr:Lm	.1833
Characteristic Impedance (Ohm)	1.4142

Resonant tank design.

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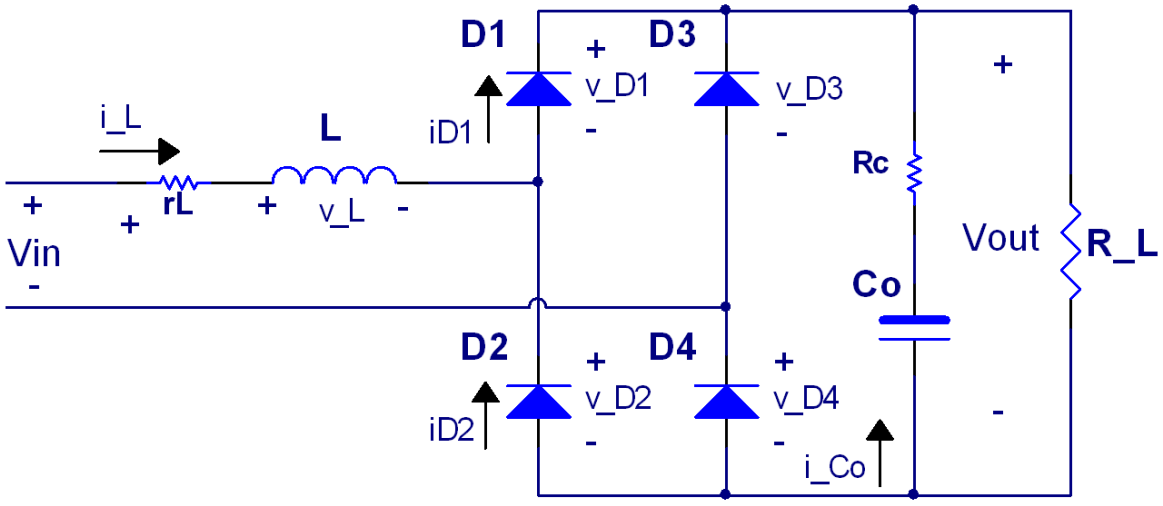
Power Converter Blocks (AC-DC)



Single-phase Diode Rectifier

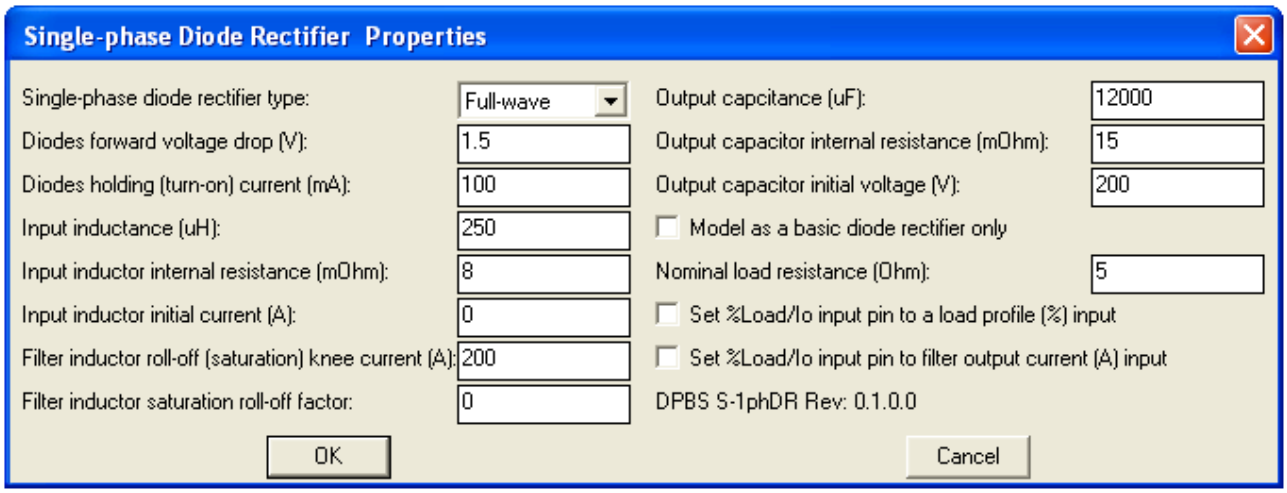
This block represents a single-phase uncontrolled diode rectifier.

Input Pins:	**Vac**	The input AC voltage of the rectifier (V)
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vdc**	The rectifier output voltage of the rectifier (V).
	Io	The rectifier output current in Amperes.
	Iin	The input current drawn by the rectifier in Amperes.
	vL	The voltage appearing across the input inductor (V).
	iC	The current in the output capacitor in Amperes.
	Vd(1..4)	The voltage across the rectifier diodes.
	Id(1..4)	The current through the rectifier diodes.
Circuit schematic:		Single-phase diode rectifier.



Dialog properties:

The single-phase diode rectifier block properties menu is shown in the following figure which appears when right-clicking on the block.



Single-phase diode rectifier type:

The choices are:

1. Half-wave (only one diode is used).
2. Full-wave (four diodes are used).

Diodes forward voltage drop:

Enter the value of the diode forward voltage drop of each diode in Volts.

Diodes holding current:

Enter the value of the diode holding current, required to keep the diode in conduction in milli-Amperes.

Input Inductance:

Enter the value of the rectifier input inductance in micro-Henrys.

Input inductor internal resistance:

The winding resistance of the input inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Input inductor initial current:

The initial inductor current (at simulation start) can be entered here in Amperes.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitance:

Insert the value of the output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Model as a basic diode rectifier only:

Check this box if the input inductance and output capacitance are to be ignored and a basic diode rectifier is desired to be modelled.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

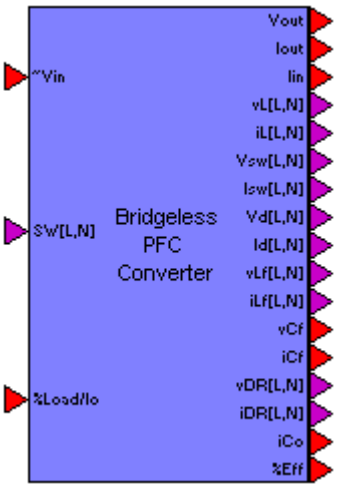
Set %Load/Io input pin to a load profile (%) input:

If this box is checked, the load (nominal load resistance) will be varied according to the value at this pin.

Set %Load/Io input pin to the rectifier output current input:

If this box is checked, the value of the nominal load resistance will be ignored and the rectifier will be modelled according to the effective load determined by the value of the output current at this input pin.

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Bridgeless PFC Converter

The bridgeless PFC is basically a dual phase boost converter with one phase connected to the mains input active line and the second phase connected to the mains input neutral line. This converter has advantages over the traditional PFC converter configuration, with a full-bridge input and subsequent boost stage, in that one diode is removed from the current path, therefore improving efficiency.

Input Pins:

~Vin Input AC line voltage (V). This is usually connected from an AC source block.

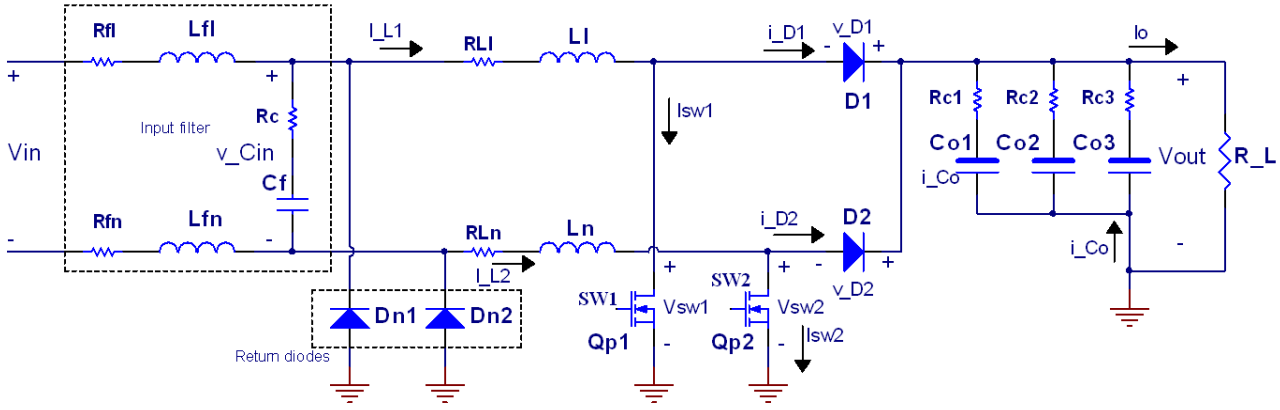
SW[L,N] Switches control (SW < 1 = OFF, SW ≥ 1 = ON); vector, rows = 1, columns = 2. Element 1 is the mains input active line switch control, element 2 is the neutral line switch control.

%Load/Io Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog.

This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.

Output Pins:	**Vout**	Converter output voltage (V)
	Iout	Converter output current (A)
	Iin	Converter input current (A). If “include input filter” is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered sum of the inductor currents. Otherwise, the current will be calculated at each simulation step based upon the filter inductance and capacitance.
	vL[L,N]	Voltages across the input boost inductors (V)
	iL[L,N]	Current through the input boost inductors (A).
	Vsw[L,N]	Switch voltages (V) – Positive for forward voltages; vector, rows = 1, columns = 2.
	Isw[L,N]	Switch currents (A) – Positive for forward current; vector, rows = 1, columns = 2.
	Vd[L,N]	Diode voltages (V) - Positive for reverse voltages; vector, rows = 1, columns = 2.
	Id[L,N]	Current through the output diodes; vector rows = 1, columns = 2. This is also the current through the split secondary windings.
	vLf[L,N]	Voltages across the input filter inductors (V)
	iLf[L,N]	Current through the input filter inductors (A).
	vCf	Input filter capacitor Voltage (V). This will be the voltage charge on input capacitor if the “include input filter” is selected, otherwise it will be directly the input voltage.
	iCf	Input filter capacitor current (A).
	vDR[L,N]	Voltage across the input return diodes in volts (when “Include input return diodes” is selected in the dialog).
	iDR[L,N]	Current through the input return path diodes (A).
	iCo	Output Capacitor Current (A)
	%Eff	Converter Efficiency (%), averaged over a switching cycle.

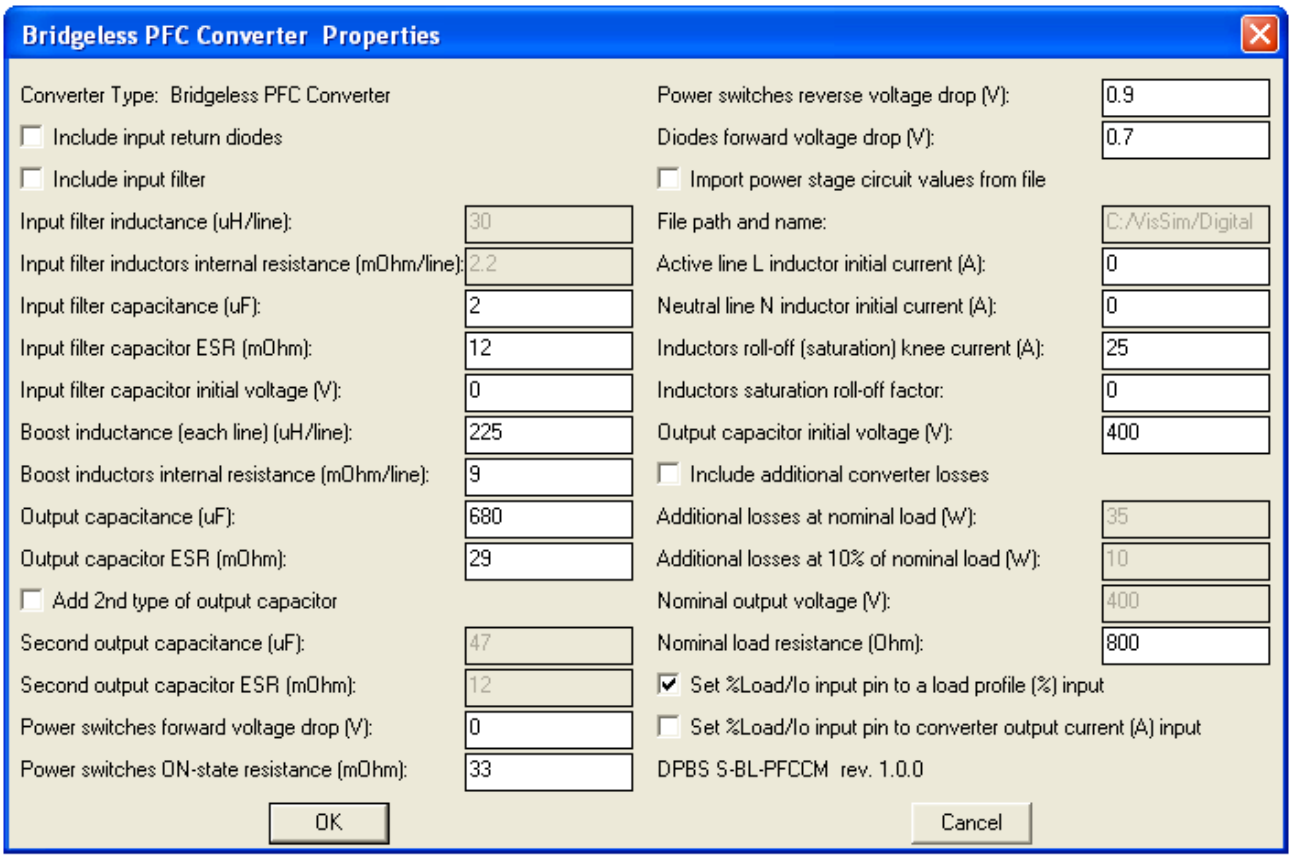
Circuit schematic: Bridgeless PFC Converter.



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The bridgeless PFC converter properties menu is shown in the following box which appears when right-clicking on the block.



Include input return diodes:

Check this box to include two return path diodes, Dn1 and Dn2 as indicated in the circuit schematic. The advantages of such a configuration is given in the literature. Note that in this bridgeless PFC converter model, it is assumed that all of the current flows through this return path when selected here. This will often not be the case in practise.

Include input filter:

Check this box to include an LLC filter at the input as shown in the circuit schematic (an input inductance on each line will be included).

Input filter inductance (each line):

Enter the value of the input filter inductance in micro-henrys for each input line (active and neutral).

Input inductor internal resistance:

The winding resistance of the boost inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Input filter capacitance:

Enter the value of the input filter capacitance in micro-farads. Note that the actual capacitance value will only affect the converter performance if “include input filter” is selected.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Boost inductance (each line):

Enter the value of the input boost inductance of each input line in micro-henrys.

Boost inductors internal resistance:

Insert the value of the equivalent series resistance of each boost inductor in milli-Ohms.

Output capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output capacitor ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Power switches forward voltage drop:

The forward voltage drop, in Volts, across the main switches can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch.

Power switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switches can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Power switches reverse voltage drop:

The reverse voltage drop, in Volts, across the main switches can be entered. This value will model the voltage drop across the reverse diode of the power switches.

Diodes forward voltage drop:

The forward voltage drop, in Volts, across the diodes of the bridgeless PFC converter can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the diode. This voltage drop also applies to the input return diodes (when this configuration is selected).

Import power stage circuit values from file:

The power component values can be directly read from a file.
The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Active line L initial inductor current:

The initial inductor current for the active line (at simulation start) can be entered here in Amperes.

Neutral line N initial inductor current:

The initial inductor current for the neutral line (at simulation start) can be entered here in Amperes.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Include additional converter losses:

Similarly to the boost converter, the power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected.

Additional losses at nominal load:

Insert the required additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load..

Nominal output voltage:

The nominal output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

Set %Load/Io input pin to a load profile (%) input:

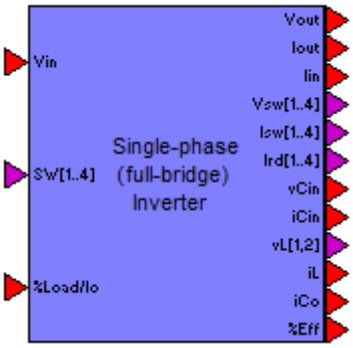
Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

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Power Converter Blocks (DC-AC)



Single-phase Inverter (Full-bridge)

This single-phase inverter model has a full-bridge (4 switches) and a split output inductance.

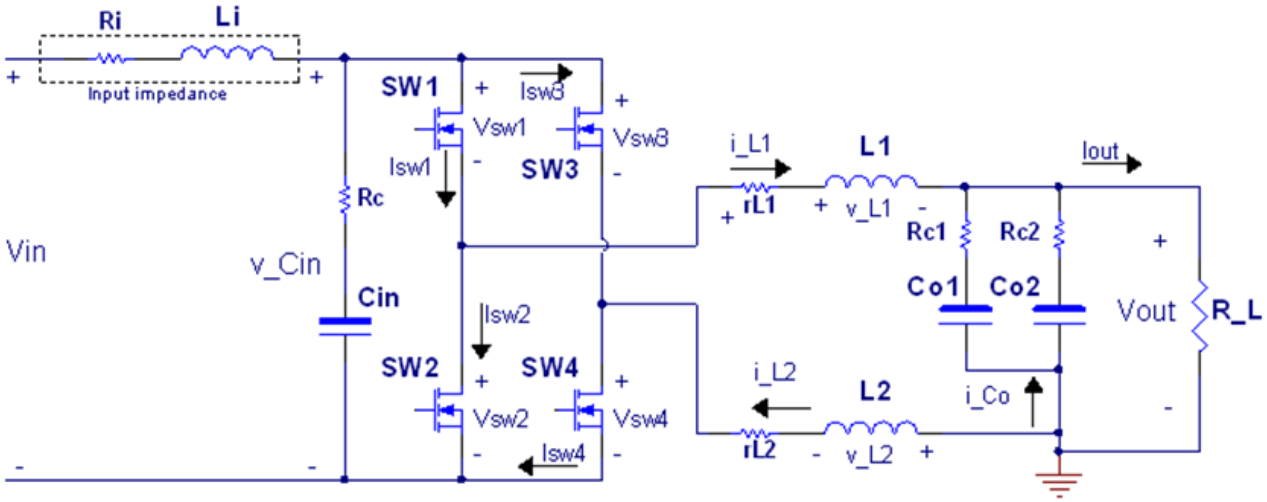
Input Pins:	**Vin**	Input voltage (V) This is usually connected from a source block or it can be the output of another converter.
	SW[1..4]	Main switches control (SW < 1 = OFF, SW ≥ 1 = ON); vector rows = 1, columns = 4
	%Load/Io	Proportion of the nominal load in percent or the load current in amperes, depending upon the configuration of this pin in the block dialog. This pin controls the amount of load to be applied to the converter at any time instant. Note that one of the "Set %Load/Io input pin to…" selections must be checked to enable this pin. The value at this pin is a percentage of the nominal load, determined by the nominal load resistance value in the dialog (see below) or directly the load current, depending upon the dialog selection.
Output Pins:	**Vout**	Converter output voltage (V)
	Iout	Converter output current (A)
	Iin	Converter input current (A). If "model with input impedance" is not selected within the dialog, then this current will be the average of the input current over each switching period. If the input capacitor is not present (Cin = 0), then this will be the unfiltered sum of the top switch currents for the case of the full-bridge converter. Otherwise, the current will be calculated at each simulation step based upon the input impedance and input capacitance.
	Vsw[1..4]	Switch Voltages (V) – Positive for forward voltages; vector rows = 1, columns = 4.
	Isw[1..4]	Switch Currents (A) – Positive for forward current; vector rows = 1, columns = 4.
	Ird[1..4]	Reverse diode currents (A) - Positive for reverse voltages; vector rows = 1, columns = 4. The voltage across the output diodes / synchronous switches.
	vCin	Input capacitor Voltage (V) This will be the voltage charge on input capacitor if the "model with input impedance" is selected, otherwise it will be directly the input voltage.
	iCin	Input capacitor current (A)

vL[1,2]	Voltage across the output filter side inductors (V)
iL	Current flowing through the output filter inductors (A)
iCo	Output Capacitor Current (A)
%Eff	Converter Efficiency (%), averaged over a switching cycle.

The value at this pin is the efficiency of the converter averaged over the last switching cycle. The converter losses included within the model are the main switches and diodes / synchronous switches conduction losses, the inductor winding resistance and the input and output capacitor losses due to their internal equivalent series resistance (ESR).

The switching losses and diode reverse recovery losses along with the inductor core losses are not included in the model.

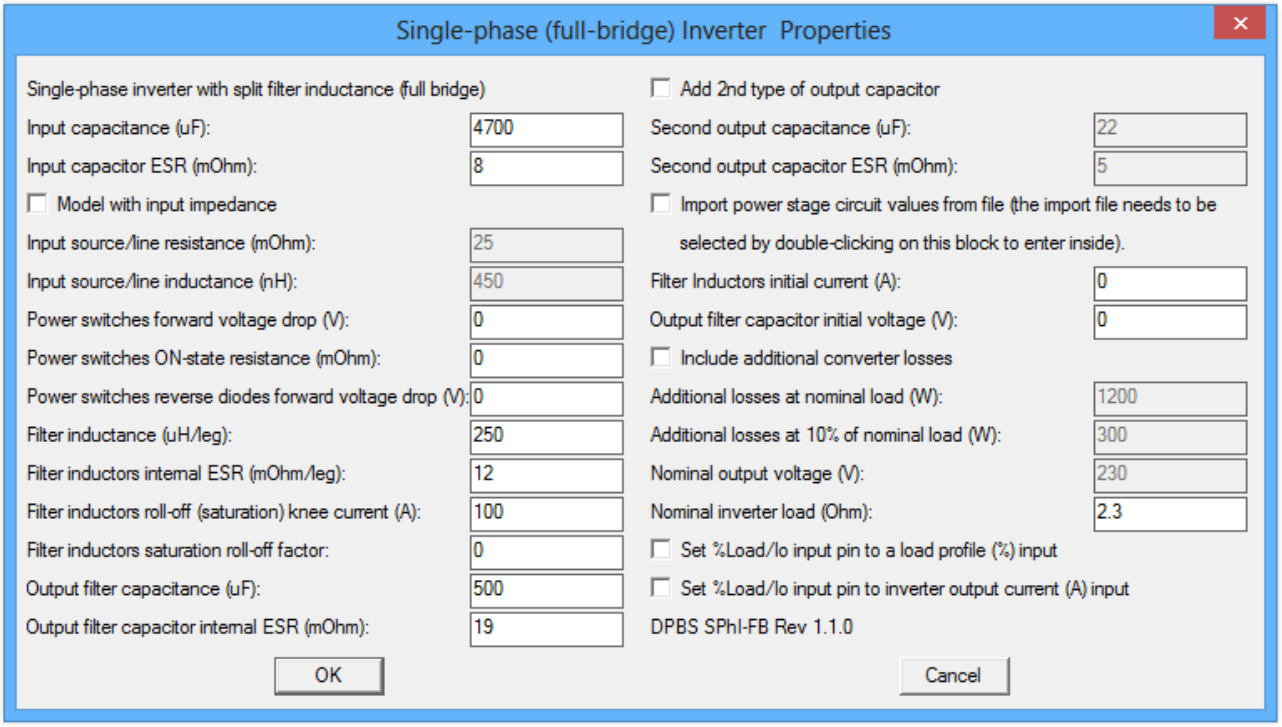
Circuit schematic: Single-phase Full-bridge Inverter



Note that the circuit schematic, along with the component values, can be viewed during a simulation by double-left clicking on the power converter block. See the buck converter description for an explanation.

Dialog properties:

The single-phase, full-bridge inverter properties menu is shown in the following box which appears when right-clicking on the block.



Input capacitance:

The value of the input capacitor in micro-Farads must be given. Note that the actual capacitance value will only affect the converter performance if “Model with input impedance” is selected below.

Input capacitor ESR:

Insert the value of the equivalent series resistance of the input capacitor in milli-Ohms.

Model with input impedance:

Check this box to model the full-bridge converter with input impedance. This can also be used to model the effects of an input filter on the full-bridge converter.

Input source/line resistance:

Insert the value of the source and / or line resistance in milli-Ohms.

Input source/line inductance:

Insert the value of the source and / or line inductance in nano-Henries.

Power switches voltage drop:

The forward voltage drop, in Volts, across the main switches of the inverter full-bridge can be entered. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch. This value can be combined with the ON-state resistance below to model an IGBT switch.

Power switches ON-state resistance:

The ON-state resistance, in milli-Ohms, of the main switches can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

Power switches reverse diodes forward voltage drop:

The forward voltage drop, in Volts, across the reverse diodes of the inverter full-bridge switches can be entered. This value will provide a fixed forward ON-state voltage regardless of the reverse current flowing through the switch.

Filter inductance:

Enter the value of the output filter inductance in micro-Henrys for each leg. The effective filter inductance will be 2 times this value.

Filter inductor internal resistance:

The winding resistance of the filter inductor should be given here in milli-Ohms. The resistance of any connections can be summed into the given value.

Inductor roll-off (saturation) knee current:

The converter inductor can be modelled with saturation and this is useful for inductors constructed with soft magnetic materials. This modelling will produce an inductor with varying inductance dependent upon the load on the converter.

Inductor saturation roll-off factor:

The roll-off factor of the inductor permeability should be inserted here. For inductors modelled without saturation, enter a value of zero here.

Output filter capacitance:

Insert the value of the main output capacitor in micro-Farads.

Output filter capacitor internal ESR:

The equivalent series resistance (ESR) of the modelled output capacitor should be given here in milli-Ohms.

Add 2nd type of output capacitor:

An additional output capacitor (usually of a different type and a different ESR value) which is connected in parallel with the main capacitor, can be included in the model.

Import power stage circuit values from file:

The power component values can be directly read from a file.
The file can be entered and viewed by double-left clicking on the main block. See the buck converter description for details on this visualization.

Filter inductors initial current:

The initial filter inductors current (at simulation start) can be entered here in Amperes.

Output filter capacitor initial voltage:

The initial voltage of the output capacitor (at simulation start) can be entered here in Volts.

Include additional converter losses:

The power converter does not model all the component losses and therefore the input to output efficiency will be higher than expected. Similar to the forward converter, since the converter duty cycle is a function of the efficiency, the duty cycle will also be lower than expected. To compensate for this, additional losses can be introduced when this box is checked.

Additional losses at nominal load:

Insert the additional full-load losses in Watts.

Additional losses at 10% load:

Insert the additional losses in Watts at 10% of full-load.

Nominal output voltage:

The nominal rms output voltage in Volts should be entered into the box. The additional converter losses will be constant from zero to 10% applied load and increase linearly from 10% to the nominal (100%) applied load.

Nominal load resistance:

The nominal (full-load) load resistance must be given here in Ohms.

Set %Load/Io input pin to a load profile (%) input:

Enable this check box to vary the load according to the value at the %Load/Io input pin and the nominal load resistance.

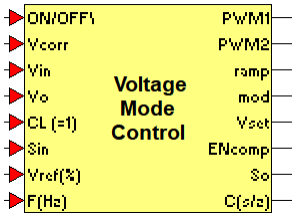
Set %Load/Io input pin to converter output current (A) input:

Enable this check box to set the load directly to the value of the current input in amperes. The nominal load resistance is not considered in this case.

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Controllers

Controllers implement a particular control technique to achieve the desired converter regulation. They are used together with one or more compensator blocks. The frequency response of the controllers model only the delays associated with any PWM generation and the computational delay in the case of digital controllers. The actual frequency response model of the control method is left to the be modelled in the power converter frequency response.



Voltage mode controller (VMC)

This controller implements the typical voltage mode control (VMC) and uses a ramp-up function to determine the duty-cycle. The PWM outputs can be single (PWM1) or dual with inverting PWM or alternating PWM with deadtime.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the voltage mode controller.
	Vcorr	Input pin usually from the output of a compensator.
	Vin	Input voltage measurement pin. This measurement is used for feed-forward compensation in VMC.
	Vo	Output voltage measurement pin. This measurement is only used for feed-forward compensation with the boost and buck-boost configurations.
	CL (=1)	Current limit trigger input. A value ≥ 1 activates the current limit, switching off the output PWM to be reset on the next switching cycle – a cycle-by-cycle (CBC) current limit.
	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and "Sample the controller on the Sin pin" is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if "Use Vref profile" is checked.
	F (Hz)	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output pins:	**PWM1**	The pulse-width modulated (PWM) output which can be connected to a power converter SW input.
	PWM2	A second pulse-width modulated (PWM) output which can be connected to a power converter SWS input for synchronous converters or the SW input for converters with two control switches such as the half-bridge, full-bridge and push-pull converters. Note that this pin is only active when the "Enable the second PWM output" option is checked.
	Ramp	The internal control ramp at the PWM frequency.
	mod	The internal modulation which along with the ramp determines the duty cycle of the PWM output.
	Vset	This is the set point voltage sent out to this pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.

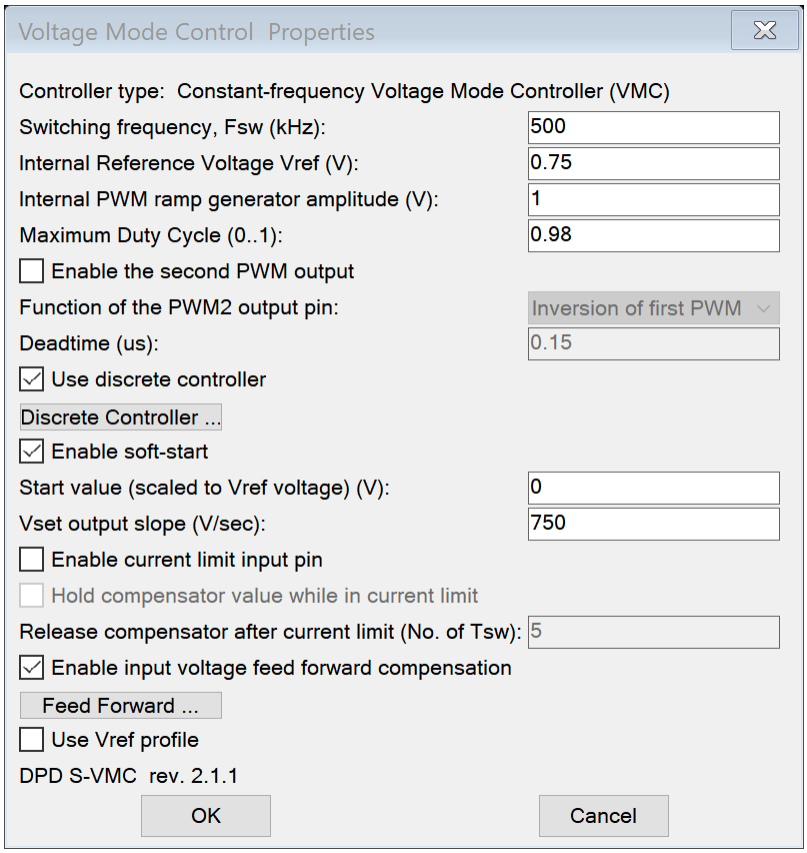
ENcomp This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.

So When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).

C(s/z) When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The voltage mode controller block properties menu is shown in the following dialog box which appears when right-clicking on the block.



Switching frequency:

Enter the required switching frequency in kHz of the buck converter to be controlled. This will set the output PWM frequency.

Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Internal PWM ramp generator amplitude (V):

Enter the peak voltage of the internal up ramp generator (usually = 1 but can be any value > 0).

Maximum duty cycle:

Enter the maximum duty cycle. This will limit the duty cycle so that it cannot exceed this given value. If not used, the value should be equal to 1.

Enable second PWM output:

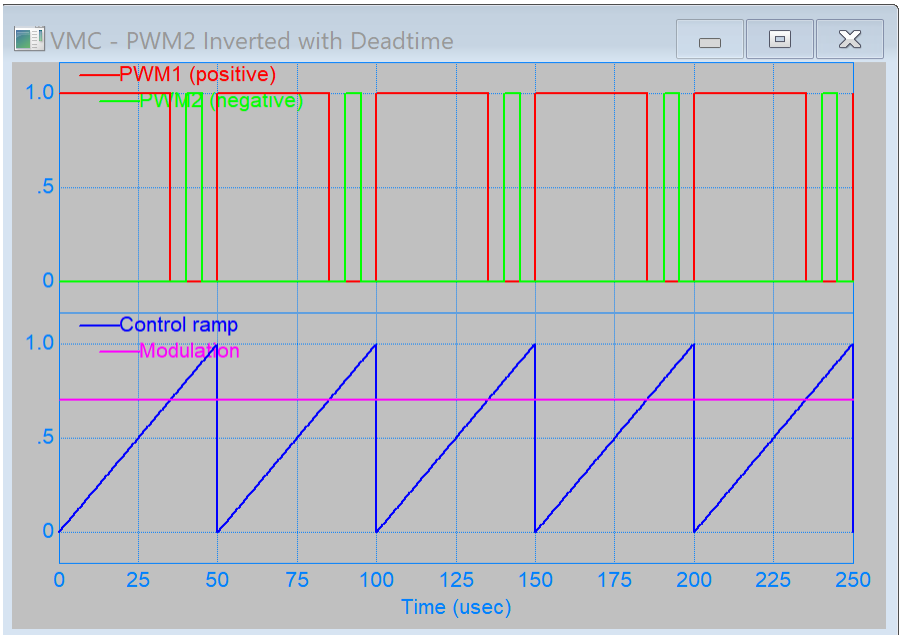
If this box is checked, the second PWM output will be activated.

Function of the PWM2 output:

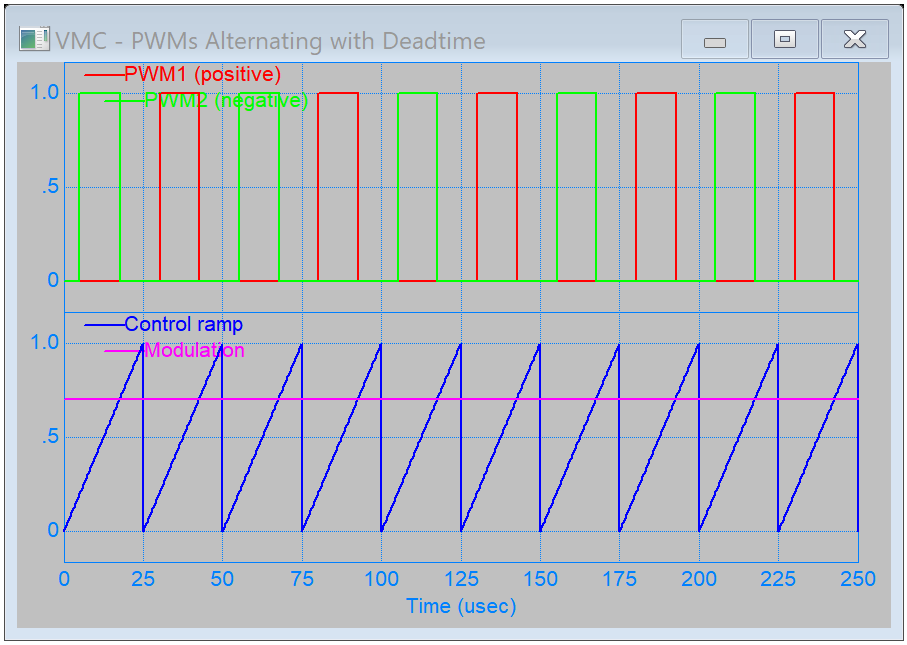
The choices are:

1. Inversion of first PWM
2. Alternating PWM

In case 1, the second PWM output will be a direct inversion of the first PWM output. In this case, the dead-time is applied to the leading edge and the rising edge of the second PWM output, maintaining the set duty cycle on PWM1. The second PWM output in this case is applicable for synchronous converters.



In case 2, the two PWM outputs will alternate and be modulated at 180° out-of-phase considering the given converter switching period, with each PWM output limited to 50% of the switching period at a duty cycle of 1. The switching frequency will be the given frequency for each PWM output; effectively doubled when considering both outputs. In this case, the dead-time is applied to the rising edge of each PWM output, reducing the duty cycle according to the ratio of the dead-time to the switching period. This PWM scheme is useful for controlling converters with dual, alternate control switches or combinations of switches such as the half-bridge, full-bridge and push-pull converters.

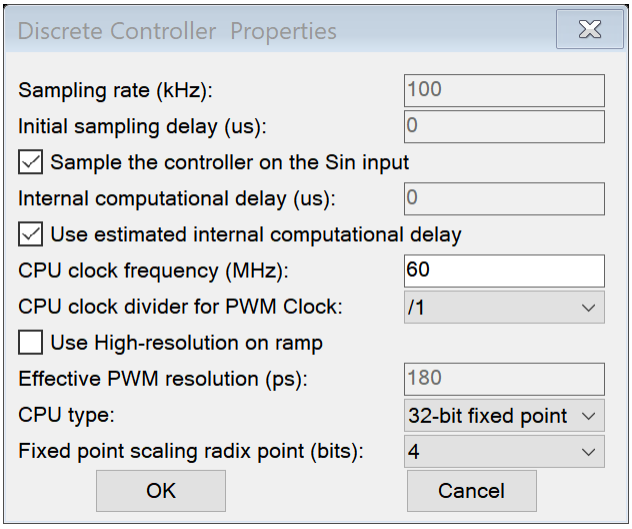


Dead-time:

If the second PWM is enabled, enter the desired dead-time between alternate PWM switchings in microseconds.

Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

CPU clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

Use high resolution on ramp:

Select this if the default resolution of the PWM is not used and a higher resolution is required. The high-resolution will be implemented internally on the ramp.

Effective PWM resolution (ps):

In the case of high-resolution, enter the effective resolution of the output PWM in picoseconds. This will be implemented into the ramp resolution. Note that this option can be used for any value of resolution.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

Enable current limit input pin:

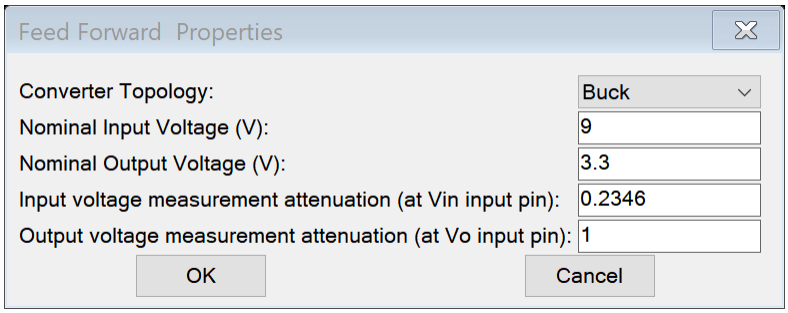
Check this box to enable current limiting of the PWM output (determined by the input pin CL).

Hold compensator value while in current limit:

If this box is checked, the compensator is disabled with its internal values “frozen” while the current limitation persists. The compensator will be released when the current limitation is removed.

Release compensator after current limit:

Enter the number of switching cycles that the compensator is to remain frozen after the removal of the current limitation. The minimum amount of cycles for the control feature to remain active is two, while in practise this would be longer due to filtering of a noisy measurement.



Enable input voltage feed forward compensation:

Check this box to enable input voltage feed-forward compensation to improve the converter response on changes of the input voltage.

Converter topology:

The choices are:

1. Buck
2. Boost
3. Buck-boost

Nominal input voltage:

Enter the nominal input voltage in volts.

Nominal output voltage:

Enter the nominal output voltage in volts. This is only required if one of the boost or buck-boost configurations are selected.

Input voltage measurement attenuation:

Enter the attenuation on the input voltage measurement seen at the Vin input pin of the controller.

Output voltage measurement attenuation:

Enter the attenuation on the output voltage measurement seen at the Vo input pin of the controller.

The input voltage feed-forward is based upon the power converter model gain with voltage mode control in continuous current mode (CCM) which is given by:

Where $G_{pz}(s)$ $\mathbf{H(s) = G_V \cdot G_{pz}(s)}$ are the transfer function poles and zeros and G_v is given by:

$$\mathbf{G_V = Vin}$$ for the buck configuration,

$$\mathbf{G_V = \frac{Vin}{(1 - D)^2} = \frac{V_o^2}{Vin}}$$ for the boost configuration and

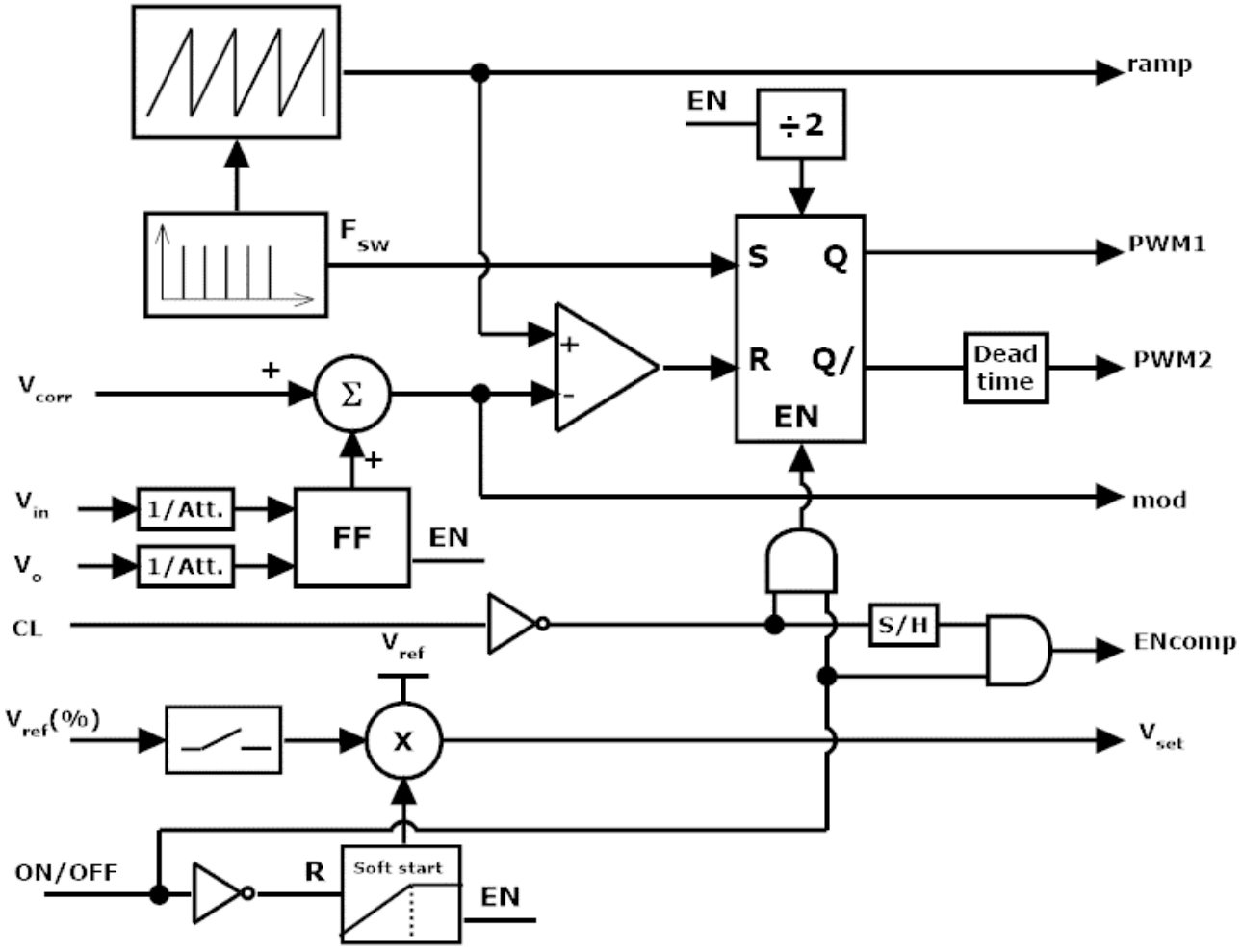
$$\mathbf{G_V = \frac{Vin}{(1 - D)^2} = \frac{(V_{in} + V_o)^2}{Vin}}$$ for the buck-boost configuration.

The compensation is most effective in the buck configuration due to its simplicity and it does not rely upon the measurement of the output voltage to determine the required gain coefficient. For this reason, feed-forward is not normally used in boost and buck-boost configurations. Also, during an input voltage transient, the actual control duty cycle may vary from the conventional or steady-state duty cycle for a given configuration as used in the G_v equations above.

Use Vref profile:

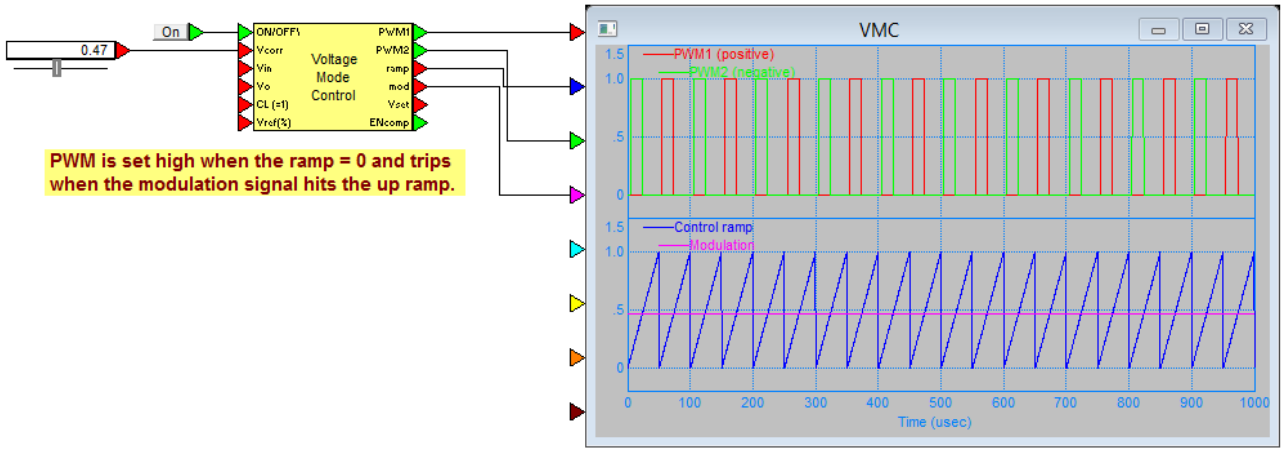
Check this box to enable the use of the input Vref% pin in order to vary the reference voltage.

The following figure is a functional block diagram of the voltage-mode controller detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.

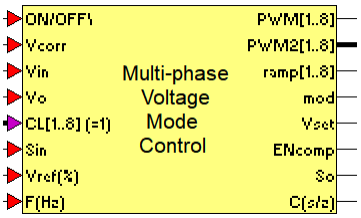


The following figure demonstrates the voltage mode controller in alternating PWM mode and the corresponding Embed example diagram can be found under

Digital Power > Examples > Simulation > Controllers > VMC-PCMC.vsm:



Contents - Simulation



Multi-phase voltage mode controller (MVMC)

The multi-phase voltage mode controller (MVMC) is a voltage mode controller block capable of controlling up to 8 interleaved buck stages. The interleaving is automatically accounted for with each successive stage being controlled with a phase

delay of $\Phi = 360 \cdot \frac{n-1}{N}$ degrees.

Where n is the actual phase leg and N is the total number of phase legs in the system.

This block is similar to the Voltage Mode Controller, except that it can control a multi-phase converter with up to 8 phase legs.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the voltage mode controller.
	Vcorr	Input pin usually from the output of a compensator.
	Vin	Input voltage measurement pin. This measurement is used for feed-forward compensation in VMC.
	Vo	Output voltage measurement pin. This measurement is only used for feed-forward compensation with the boost and buck-boost configurations.
	CL[1..8] (=1)	Current limit trigger input. A value ≥ 1 activates the current limit, switching off the output PWM to be reset on the next switching cycle – a cycle-by-cycle (CBC) current limit. Format is a vector with rows = 1, columns = 8.
	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and "Sample the controller on the Sin pin" is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if "Use Vref profile" is checked.
	F (Hz)	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output pins:	**PWM[1..8]**	The pulse-width modulated (PWM) output which can be connected to a multi-phase power converter SW input. Format is a vector with rows = 1, columns = 8.
	PWM/[1..8]	A second pulse-width modulated (PWM) output which can be connected to a multi-phase power converter SWS input for synchronous converters or the SW input for converters with two control switches such as the half-bridge, full-bridge and push-pull converters. Note that this pin is only active when the "Enable the second PWM output" option is checked. Format is a vector with rows = 1, columns = 8.
	Ramp[1..8]	The internal control ramp at the PWM frequency. Format is a vector with rows = 1, columns = 8.
	mod	The internal modulation which along with the ramp determines the duty cycle of the PWM output.
	Vset	This is the set point voltage sent out to this pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.

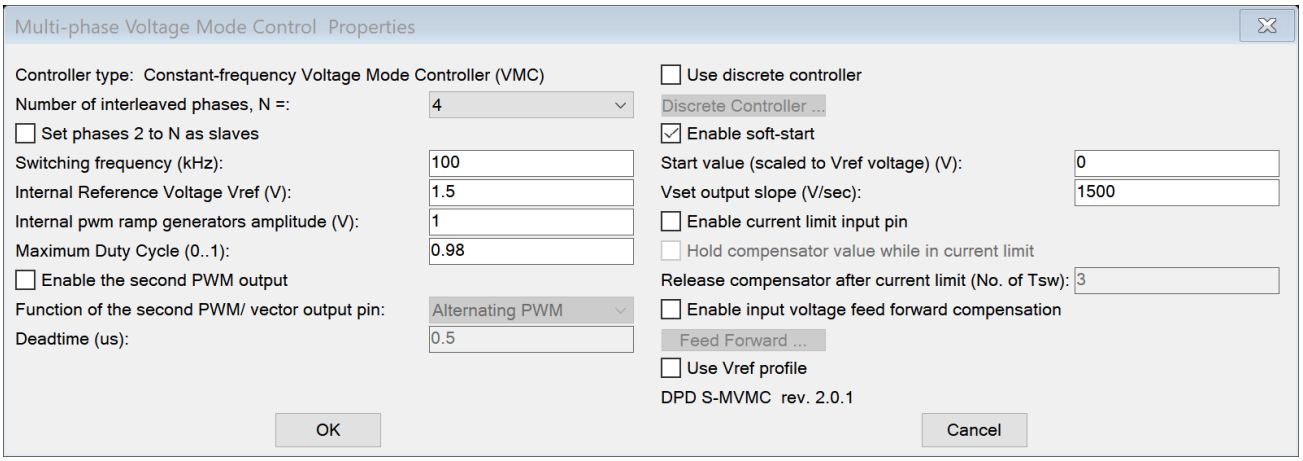
ENcomp This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.

So When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).

C(s/z) When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The multi-phase voltage mode controller block properties menu is shown in the following box which appears when right-clicking on the block.



Number of interleaved phases:

Select the number of phase legs of the multiphase converter from 1 to 8.

Set phases 2 to 8 as slaves:

If this box is checked, the enabled phase legs from 2 to 8 will be set as slaves to the first phase leg. This means that a single ramp for the first phase control will be used and the duty cycle of the remaining phases will be identical to that of the master (first) phase. If left unchecked, a phase-displaced ramp will be used individually for all phases so that the duty cycle could vary between phases, particularly during transients. The current sharing between the phases may be improved when they are set as slaves and the control may be simpler, though the response will vary for the two cases.

Switching frequency:

Enter the required switching frequency of the power converter to be controlled. This will set the output PWM frequency.

Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Internal PWM ramp generator amplitude (V):

Enter the peak voltage of the internal up ramp generator (usually = 1 but can be any value > 0).

Maximum duty cycle:

Enter the maximum duty cycle. This will limit the duty cycle so that it cannot exceed this given value. If not used, the value should be equal to 1.

Enable second PWM output:

If this box is checked, the second PWM output will be activated.

Function of the PWM2 output:

The choices are:

1. Inversion of first PWM
2. Alternating PWM (F = Fsw/2).

In case 1, the second PWM output will be a direct inversion of the first PWM output. In this case, the dead-time is applied to the leading edge and the rising edge of the second PWM output, maintaining the set duty cycle on PWM1. The second PWM output in this case is applicable for synchronous converters.

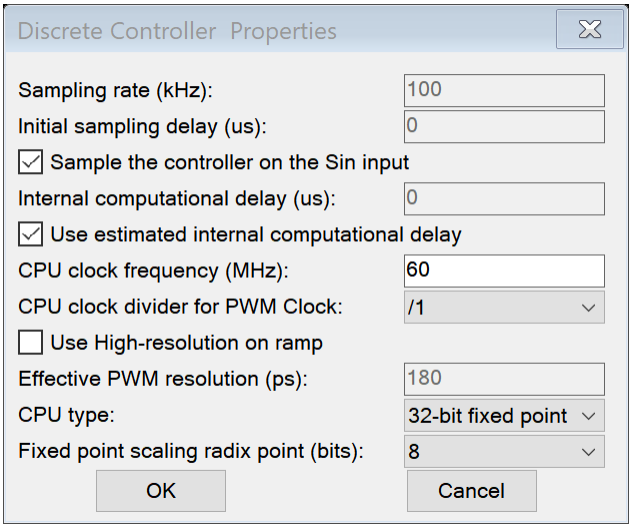
In case 2, the two PWM outputs will alternate and be modulated at 180° out-of-phase considering the given converter switching period, with each PWM output limited to 50% of the switching period at a duty cycle of 1. The switching frequency will be the given frequency for each PWM output; effectively doubled when considering both outputs. In this case, the dead-time is applied to the rising edge of each PWM output, reducing the duty cycle according to the ratio of the dead-time to the switching period. This PWM scheme is useful for controlling converters with dual, alternate control switches or combinations of switches such as the half-bridge, full-bridge and push-pull converters.

Dead-time:

Enter the desired dead-time in microseconds.

Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

Use high resolution on ramp:

Select this if the default resolution of the PWM is not used and a higher resolution is required. The high-resolution will be implemented internally on the ramp.

Effective PWM resolution (ps):

Enter the effective resolution of the output PWM in picoseconds. This will be implemented into the ramp resolution.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.
e.g. For a fixed point scaling of fx4.16, 4 should selected here.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

Enable current limit input pin:

Check this box to enable current limiting of the PWM output (determined by the input pin CL).

Hold compensator value while in current limit:

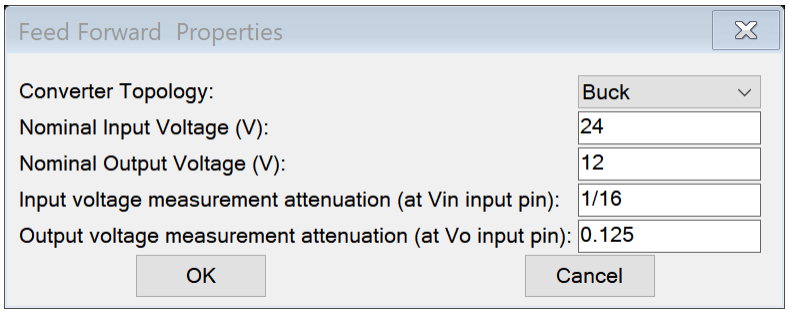
If this box is checked, the compensator is disabled with its internal values “frozen” while the current limitation persists. The compensator will be released when the current limitation is removed.

Release compensator after current limit:

Enter the number of switching cycles that the compensator is to remain frozen after the removal of the current limitation. The minimum amount of cycles for the control feature to remain active is two, while in practise this would be longer due to filtering of a noisy measurement.

Enable input voltage feed forward compensation:

Check this box to enable input voltage feed-forward compensation to improve the converter response on changes of the input voltage.



Converter topology:

The choices are:

1. Buck
2. Boost
3. Buck-boost

Nominal input voltage:

Enter the nominal input voltage in volts.

Nominal output voltage:

Enter the nominal output voltage in volts.

Input voltage measurement attenuation:

Enter the attenuation on the input voltage measurement seen at the Vin input pin of the controller.

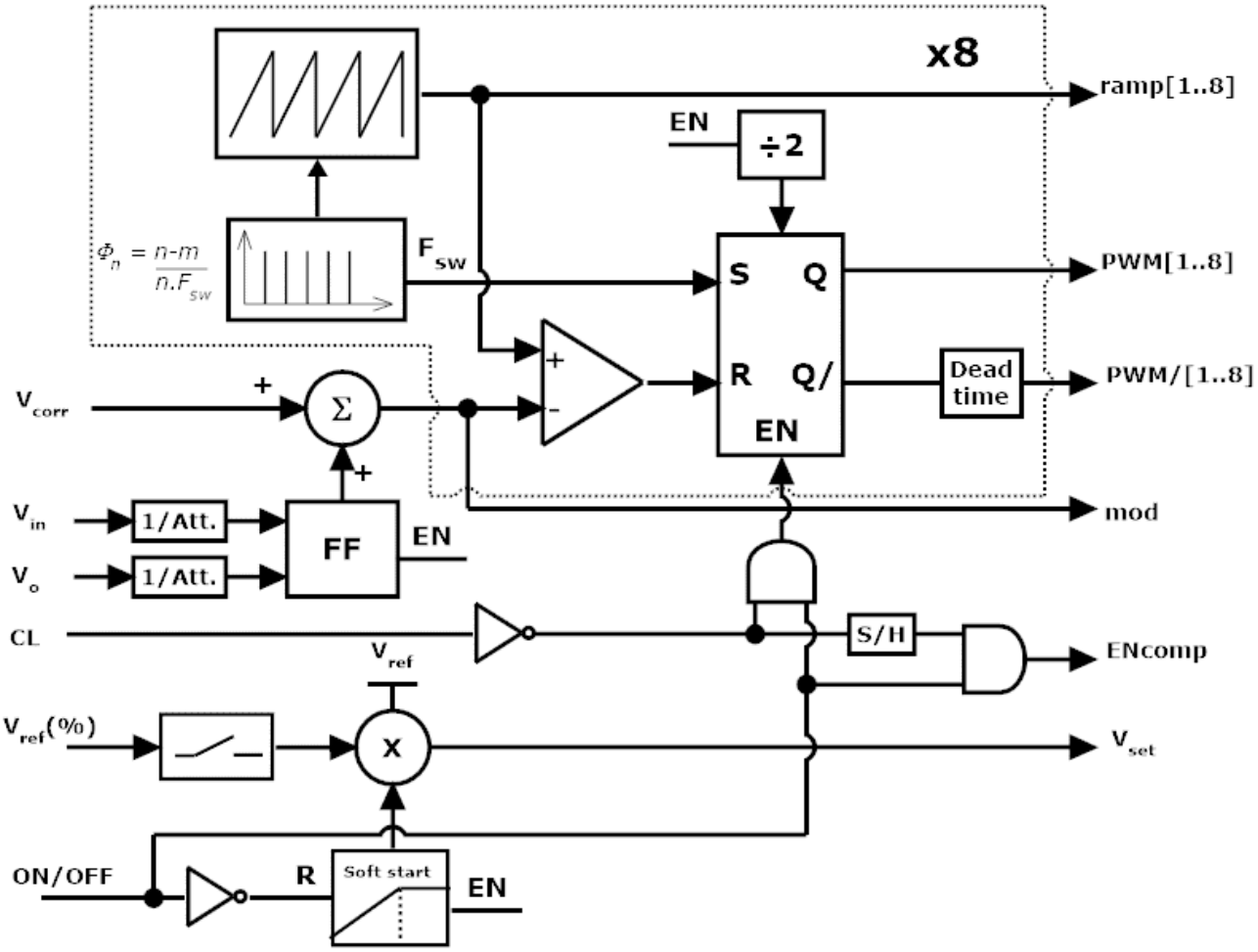
Output voltage measurement attenuation:

Enter the attenuation on the output voltage measurement seen at the Vo input pin of the controller.

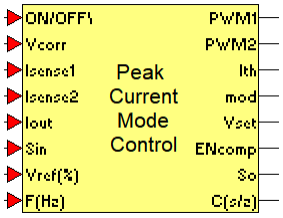
Use Vref profile:

Check this box to enable the use of the input Vref% pin.

The following figure is a functional block diagram of the multi-channel voltage-mode controller detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.



Contents - Simulation



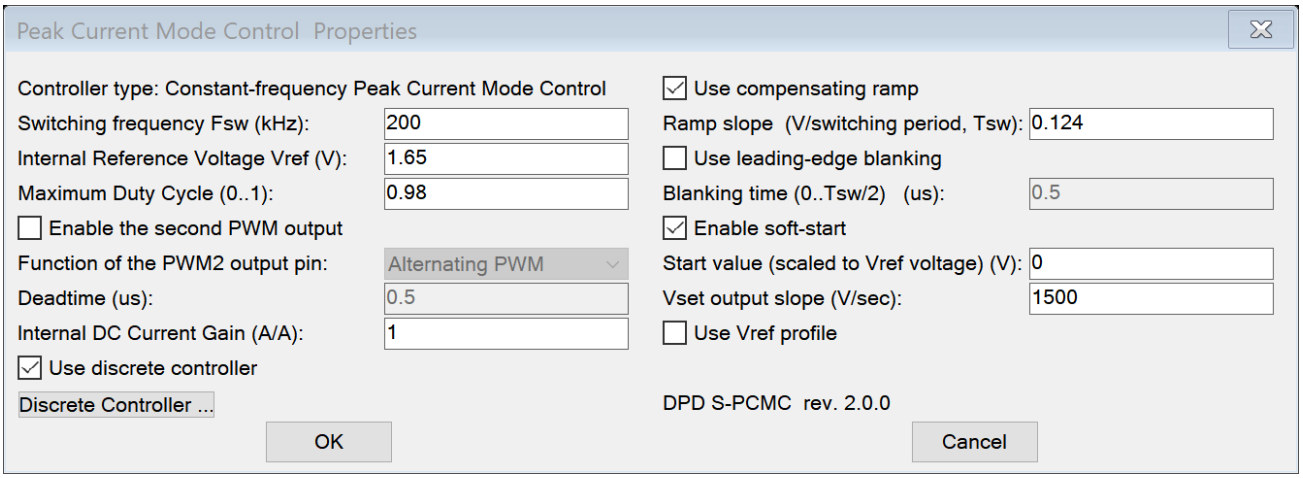
Peak current mode controller (PCMC)

This controller implements the typical peak current mode control (PCMC) and the duty-cycle is determined by the point at which the current reaches the modulation value plus a compensating ramp. The PWM outputs can be single (PWM1) or dual with inverting PWM or alternating PWM with deadtime.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the voltage mode controller.
	Vcorr	Input pin usually from the output of a compensator.
	Isense1	Current sense input for peak current regulation.
	Isense2	A second current sense input for peak current regulation. For two-leg converters there may be two individual current sensors; one in each leg.
	Iout	The output current measurement.
	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and “Sample the controller on the Sin pin” is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if “Use Vref profile” is checked.
	F (Hz)	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram
Output pins:	**PWM1**	The pulse-width modulated (PWM) output which can be connected to a power converter SW input.
	PWM2	A second pulse-width modulated (PWM) output which can be connected to a power converter SWS input for synchronous converters or the SW input for converters with two control switches such as the half-bridge, full-bridge and push-pull converters. Note that this pin is only active when the “Enable the second PWM output” option is checked.
	Ith	The current threshold which is the regulation signal (dependent upon the voltage error) plus the compensating ramp if enabled.
	mod	The internal modulation signal without the compensating ramp.
	Vset	This is the set point voltage sent out to this pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.
	ENcomp	This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.
	So	When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).
	C(s/z)	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The peak current mode controller block properties menu is shown in the following box which appears when right-clicking on the block.



Switching frequency:

Enter the required switching frequency of the power converter to be controlled. This will set the output PWM frequency.

Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Maximum duty cycle:

Enter the maximum duty cycle. This will limit the duty cycle so that it cannot exceed this given value. If not used, the value should be equal to 1.

Enable second PWM output:

If this box is checked, the second PWM output will be activated.

Function of the PWM2 output:

The choices are:

1. Inversion of first PWM
2. Alternating PWM (F = Fsw/2).

In case 1, the second PWM output will be a direct inversion of the first PWM output. In this case, the dead-time is applied to the leading edge and the rising edge of the second PWM output, maintaining the set duty cycle on PWM1. The second PWM output in this case is applicable for synchronous converters.

In case 2, the two PWM outputs will alternate and be modulated at 180° out-of-phase considering the given converter switching period, with each PWM output limited to 50% of the switching period at a duty cycle of 1. The switching frequency will be the given frequency for each PWM output; effectively doubled when considering both outputs. In this case, the dead-time is applied to the rising edge of each PWM output, reducing the duty cycle according to the ratio of the dead-time to the switching period. This PWM scheme is useful for controlling converters with dual, alternate control switches or combinations of switches such as the half-bridge, full-bridge and push-pull converters.

Dead-time:

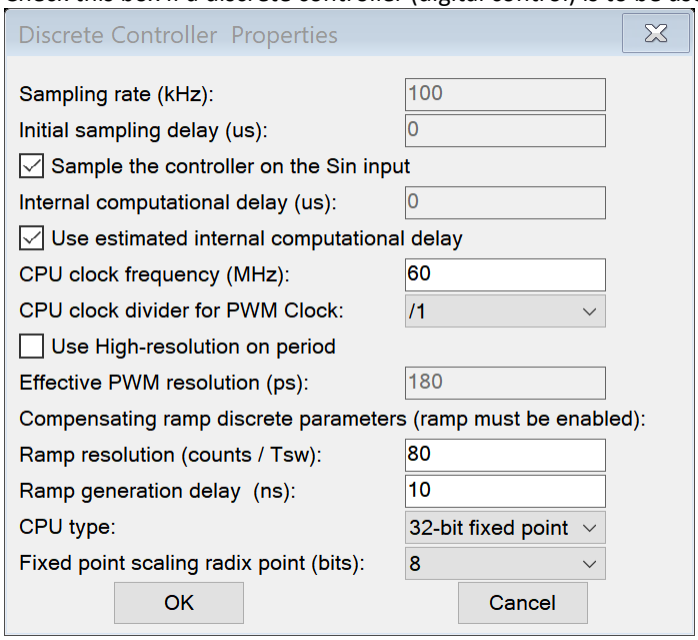
Enter the desired dead-time in micro-seconds.

Internal DC current gain:

Enter the DC gain of the measured current used for peak current regulation.

Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

CPU clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

Use high resolution on period:

Select this if the default resolution of the PWM period is not used and a higher resolution is required. The high-resolution will be implemented internally to calculate the period of the switching PWM.

Effective PWM resolution (ps):

Enter the effective resolution of the output PWM in picoseconds. This will be implemented into the period resolution.

Compensating ramp discrete parameters (when the compensating ramp is enabled):

Ramp resolution (counts / Tsw):

Enter the resolution of the compensating ramp in the number of counts per switching period.

Ramp generation delay (ns):

Enter any delay which may occur due to the generation of the ramp (e.g. DAC delay time).

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

Use compensating ramp:

Check this box if slope compensation is required. For peak current control, with a duty cycle around 50% and higher, sub-harmonic oscillations are a problem and the control loop must be compensated, typically using a compensating ramp at the converter switching frequency.

Ramp slope:

Enter the value of the slope of the compensating ramp in Volts / switching period.

Ramp resolution:

Enter the resolution of the compensating ramp (digital control). The ramp will be typically quantized if it is constructed digitally (e.g. in a CLA) and the resolution can be entered here.

Ramp generation delay:

Again if the compensating ramp is constructed digitally, a delay can be entered here corresponding to the calculation delay of each point on the ramp.

Use leading-edge blanking:

Check this box if leading-edge blanking is required. Leading-edge blanking (LEB) is normally used in peak current mode to filter the current measurement signal, or more precisely “ignore” it for a given window of time. This is useful to filter out any noise impulses during the switching instant of power semiconductor devices.

Blanking time:

Enter the required blanking time in microseconds up to a maximum of half the switching period.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

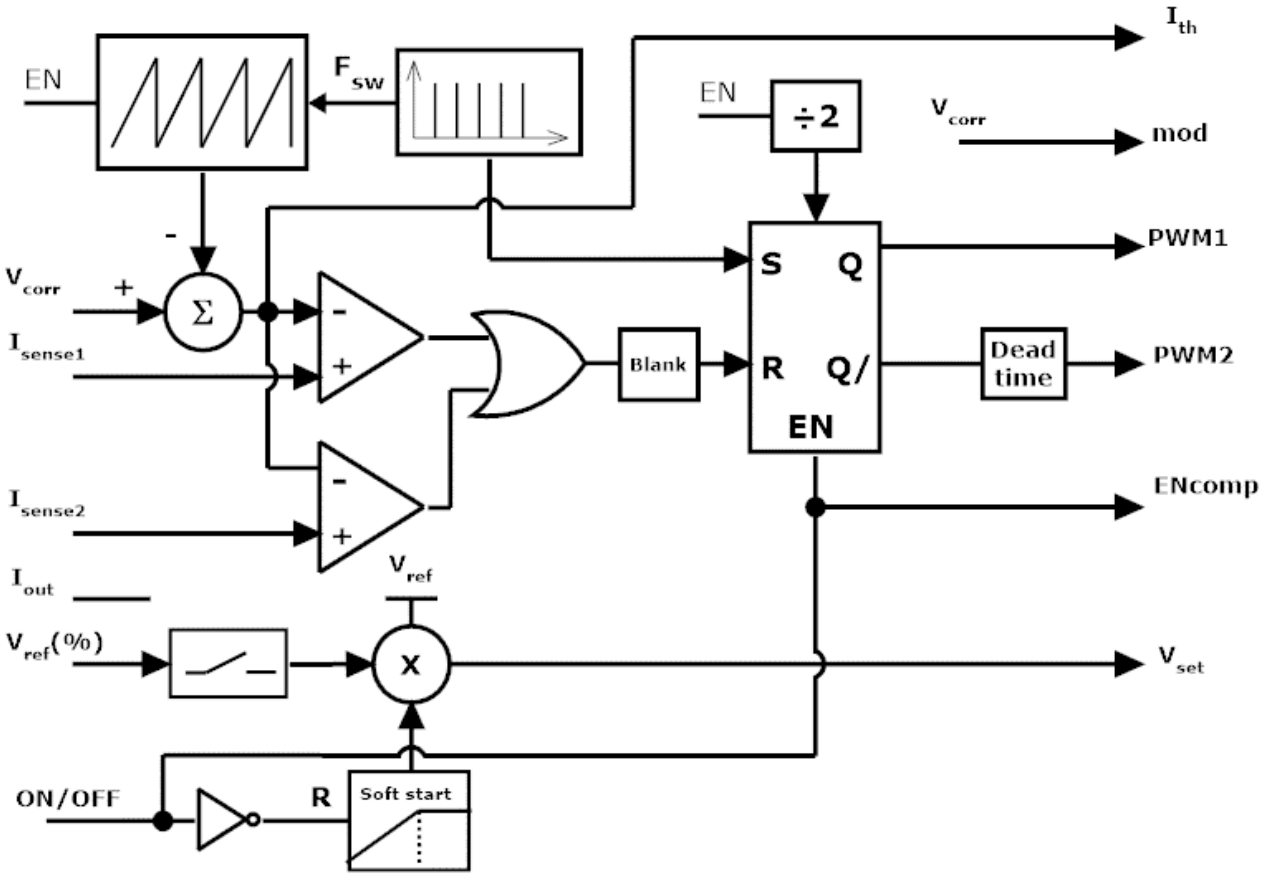
Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

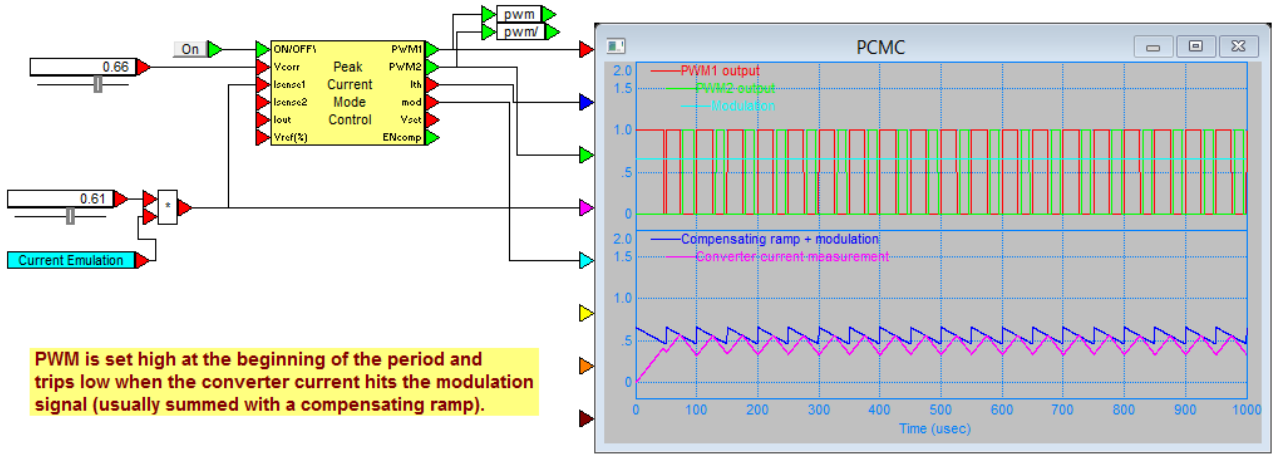
Use Vref profile:

Check this box to enable the use of the Vref% input pin.

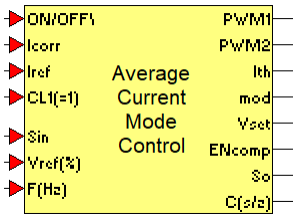
The following figure is a functional block diagram of the peak current-mode controller detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.



The following figure demonstrates the peak current mode controller and the corresponding Embed example diagram can be found under Digital Power > Examples > Simulation > Controllers > VMC-PCMC.vsm:



Contents - Simulation



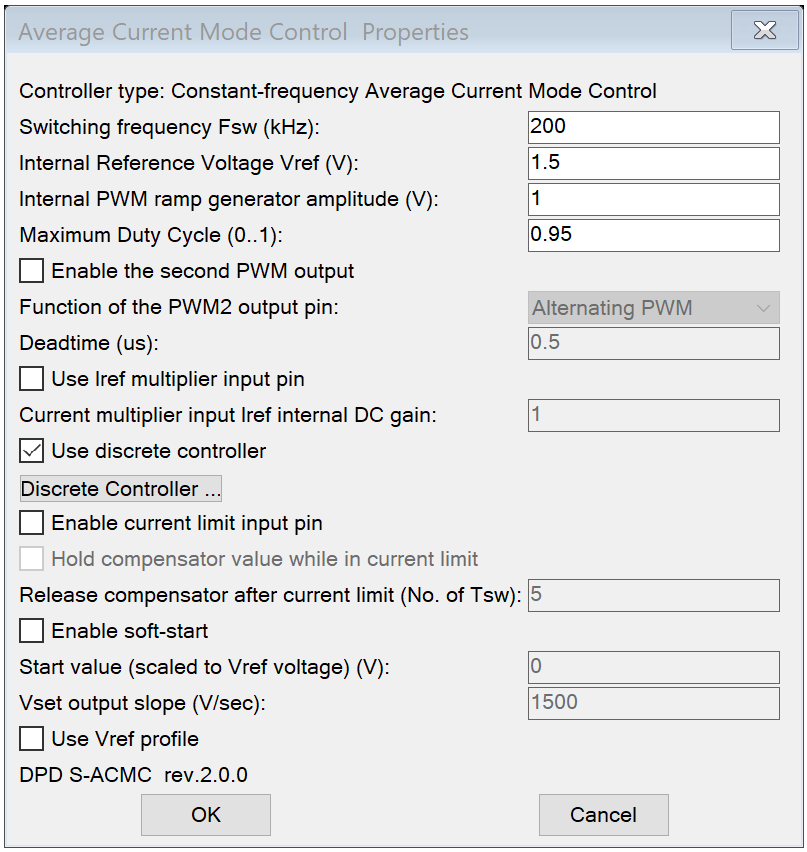
Average current mode controller (ACMC)

Average current mode control generally consists of two control loops; an inner current loop regulating the average current and an outer voltage control loop. The switching frequency is constant in this case.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the voltage mode controller.
	Icorr	Input pin usually from the output of a compensator.
	Iref	A reference current input to be multiplied by the modulation for current shaping.
	CL (=1)	Current limit trigger input. A value ≥ 1 activates the current limit, switching off the output PWM to be reset on the next switching cycle – a cycle-by-cycle (CBC) current limit.
	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and "Sample the controller on the Sin pin" is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if "Use Vref profile" is checked.
	F (Hz)	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output pins:	**PWM1**	The pulse-width modulated (PWM) output which can be connected to a power converter SW input.
	PWM2	A second pulse-width modulated (PWM) output which can be connected to a power converter SWS input for synchronous converters or the SW input for converters with two control switches such as the half-bridge, full-bridge and push-pull converters. Note that this pin is only active when the "Enable the second PWM output" option is checked.
	Ith	Current threshold.
	mod	The internal modulation which along with the ramp determines the duty cycle of the PWM output.
	Vset	This is the set point voltage sent out to this pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.
	ENcomp	This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.
	So	When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).
	C(s/z)	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The voltage mode controller block properties menu is shown in the following box which appears when right-clicking on the block.



Switching frequency:

Enter the required switching frequency of the power converter to be controlled. This will set the output PWM frequency.

Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Internal PWM ramp generator amplitude (V):

Enter the peak voltage of the internal up ramp generator (usually = 1 but can be any value > 0).

Maximum duty cycle:

Enter the maximum duty cycle. This will limit the duty cycle so that it cannot exceed this given value. If not used, the value should be equal to 1.

Enable second PWM output:

If this box is checked, the second PWM output will be activated.

Function of the PWM2 output:

The choices are:

1. Inversion of first PWM
2. Alternating PWM (F = Fsw/2).

In case 1, the second PWM output will be a direct inversion of the first PWM output. In this case, the dead-time is applied to the leading edge and rising edge of the second PWM output, maintaining the set duty cycle. The second PWM output in this case is applicable for synchronous converters.

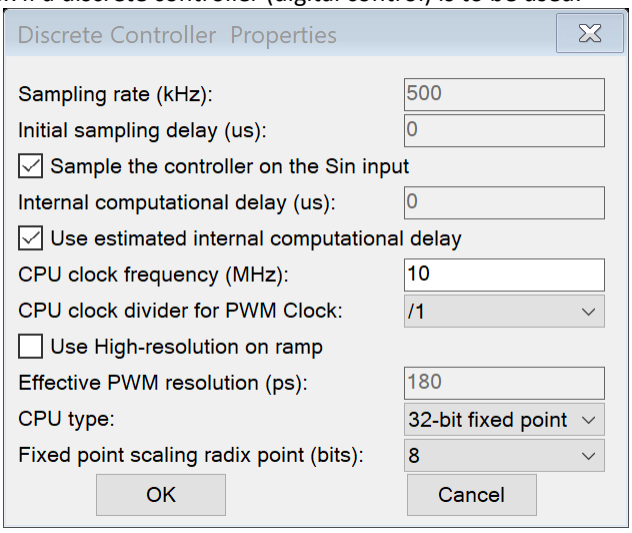
In case 2, the two PWM outputs will alternate and be modulated with a 180° phase shift. The switching frequency will be half the given frequency (for each PWM output). In this case, the dead-time is applied to the rising edge of each PWM output, reducing the duty cycle according to the ratio of the dead-time to the switching period. This PWM scheme is useful for controlling converters with dual, alternate control switches or combinations of switches such as the half-bridge, full-bridge and push-pull converters.

Dead-time:

Enter the desired dead-time in microseconds.

Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

CPU clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

Use high resolution on period:

Select this if the default resolution of the PWM period is not used and a higher resolution is required. The high-resolution will be implemented internally to calculate the period of the switching PWM.

Effective PWM resolution (ps):

Enter the effective resolution of the output PWM in picoseconds. This will be implemented into the period resolution.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

Enable current limit input pin:

Check this box to enable current limiting of the PWM output (determined by the input pin CL).

Hold compensator value while in current limit:

If this box is checked, the compensator is disabled with its internal values “frozen” while the current limitation persists. The compensator will be released when the current limitation is removed.

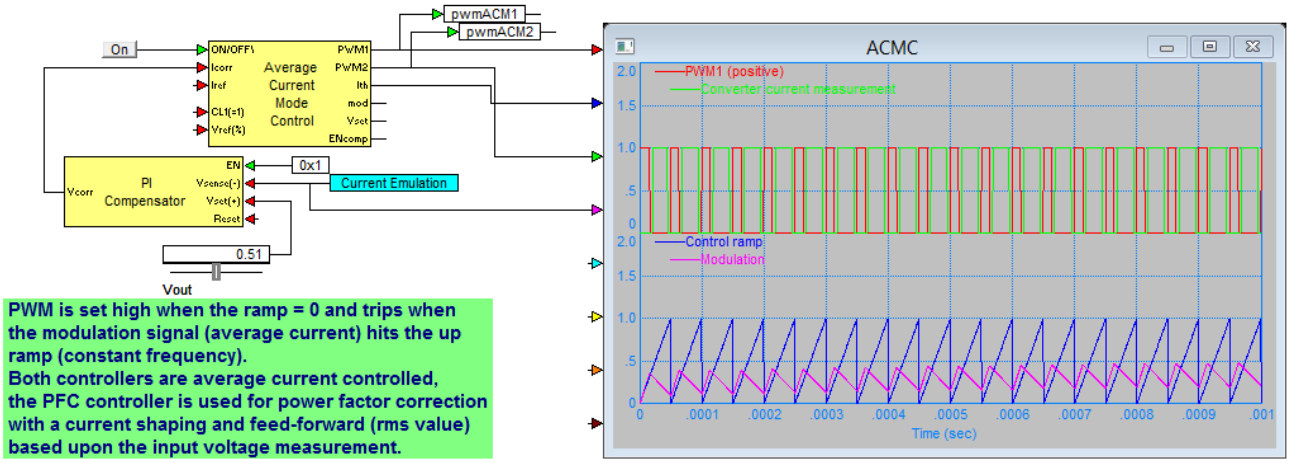
Release compensator after current limit:

Enter the number of switching cycles that the compensator is to remain frozen after the removal of the current limitation. The minimum amount of cycles for the control feature to remain active is two, while in practise this would be longer due to filtering of a noisy measurement.

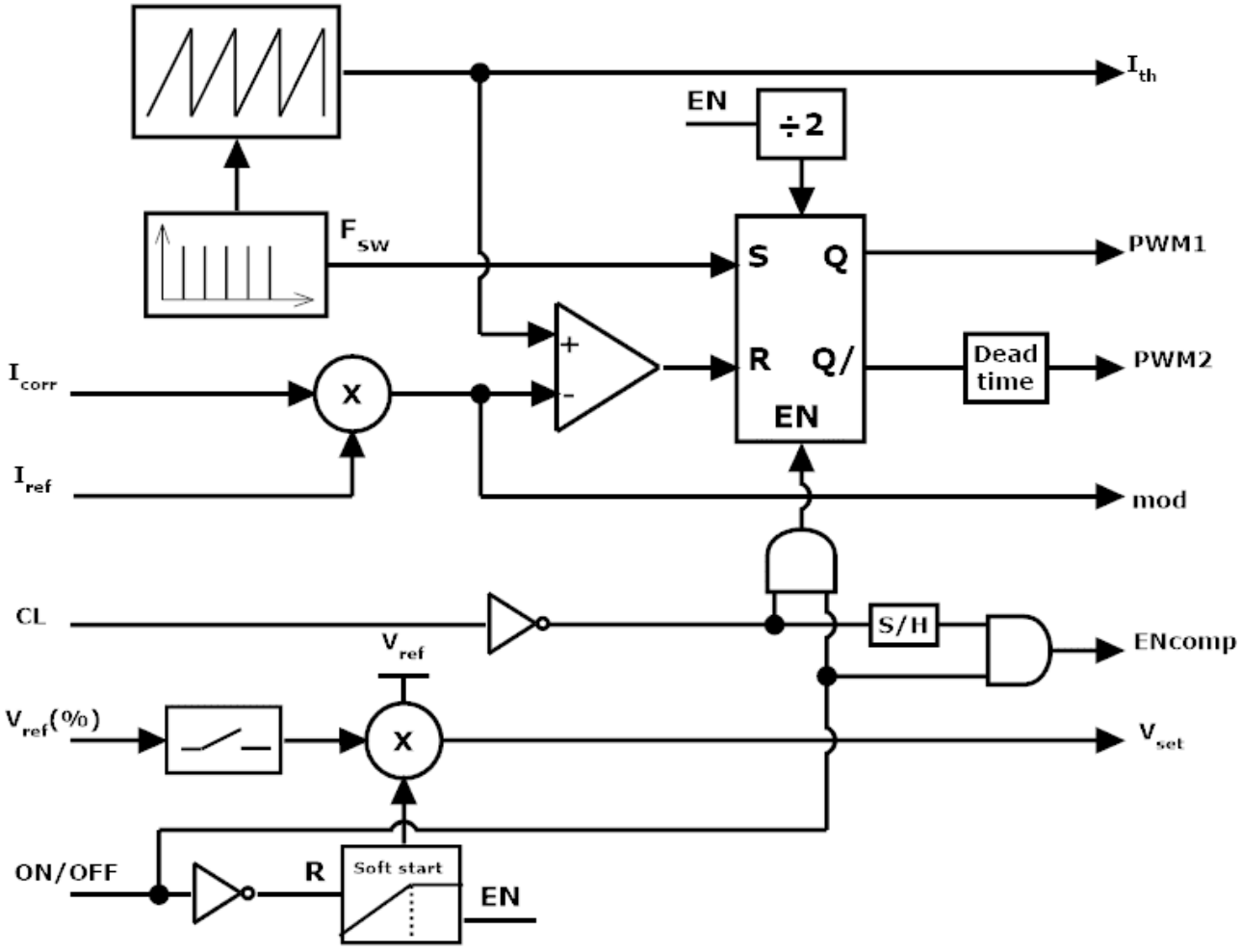
Use Vref profile:

Check this box to enable the use of the input Vref% pin.

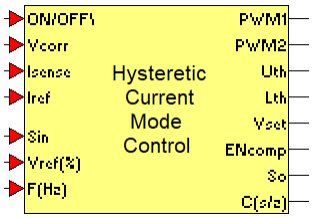
The following figure demonstrates the average current mode controller and the corresponding Embed example diagram can be found under Digital Power > Examples > Simulation > Controllers >ACMC – PFCC.vsm:



The following figure is a functional block diagram of the average current-mode controller detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.



Contents - Simulation



Hysteretic current mode controller (HCMC)

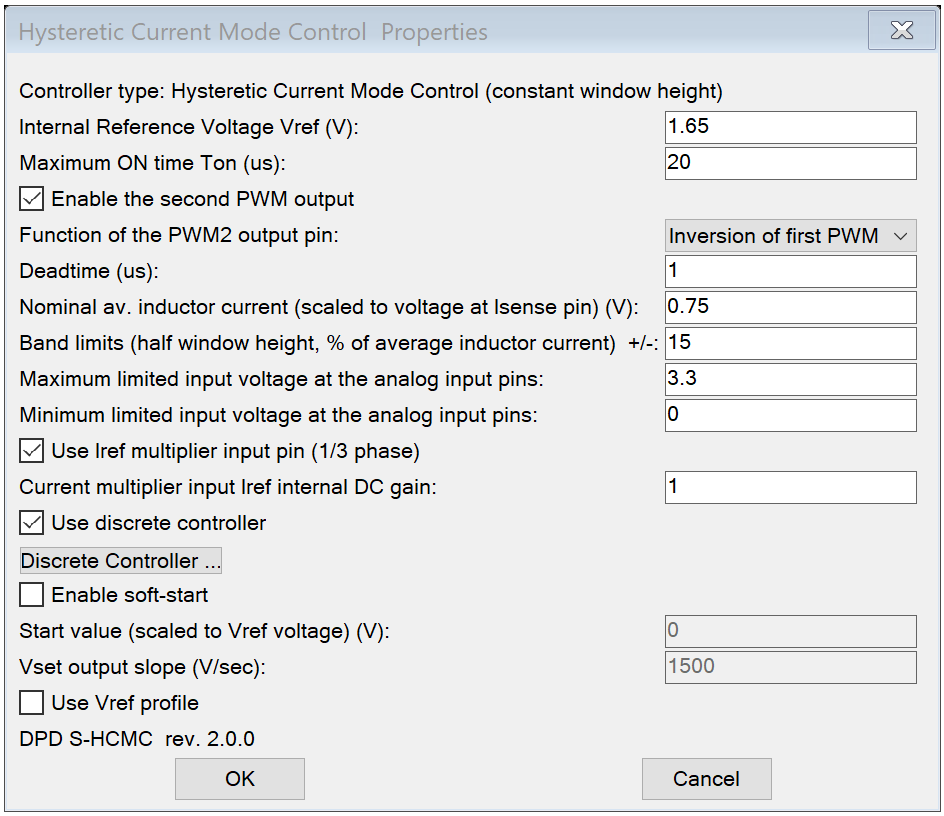
Hysteretic current mode control generates upper and lower bands which limit the peak current on the upper limit and the valley current on the lower limit. This control is generally much easier to compensate for but results in a variable switching frequency.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the voltage mode controller.
	Vcorr	Input pin usually from the output of a compensator.
	Isense	Current sense measurement input.
	Iref	Current reference input (the hysteresis bands follow this input).
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if "Use Vref profile" is checked.

	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and “Sample the controller on the Sin pin” is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if “Use Vref profile” is checked.
	F (Hz)	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output pins:	**PWM1**	The pulse-width modulated (PWM) output which can be connected to a power converter SW input.
	PWM2	A second pulse-width modulated (PWM) output which can be connected to a power converter SWS input for synchronous converters or the SW input for converters with two control switches such as the half-bridge, full-bridge and push-pull converters. Note that this pin is only active when the “Enable the second PWM output” option is checked.
	Uth	The upper band threshold.
	Lth	The lower band threshold.
	Vset	This is the set point voltage sent out to this pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.
	ENcomp	This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.
	So	When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).
	C(s/z)	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The hysteretic current mode controller block properties menu is shown in the following box which appears when right-clicking on the block.



Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Maximum ON time, Ton:

Enter the maximum ON time in microseconds. This will limit the time that the first PWM output remains high (=1) or the switch on time of the power converter switch.

Enable second PWM output:

If this box is checked, the second PWM output will be activated.

Function of the PWM2 output:

The choices are:

1. Inversion of first PWM
2. Alternating PWM (F = Fsw/2).

In case 1, the second PWM output will be a direct inversion of the first PWM output. In this case, the dead-time is applied to the leading edge and rising edge of the second PWM output, maintaining the set duty cycle. The second PWM output in this case is applicable for synchronous converters.

In case 2, the two PWM outputs will alternate and be modulated with a 180° phase shift. The switching frequency will be half the given frequency (for each PWM output). In this case, the dead-time is applied to the rising edge of each PWM output, reducing the duty cycle according to the ratio of the dead-time to the switching period. This PWM scheme is useful for controlling converters with dual, alternate control switches or combinations of switches such as the half-bridge, full-bridge and push-pull converters.

Dead-time:

Enter the desired dead-time in microseconds.

Nominal average inductor current:

Enter the nominal average inductor current (equal to the output current for a buck, the input current for a boost configuration or the output plus input current for a buck-boost configuration).

Band limits (half window height):

Enter the band limit as a percentage of the average inductor current given above. The bands will be ± this value with respect to the average current value.

Maximum limited input voltage at the analog input pins:

This value sets the upper limit on the input measurements of the block particularly at the Iref input.

Minimum limited input voltage at the analog input pins:

This value sets the lower limit on the input measurements of the block.

Use Iref multiplier pin:

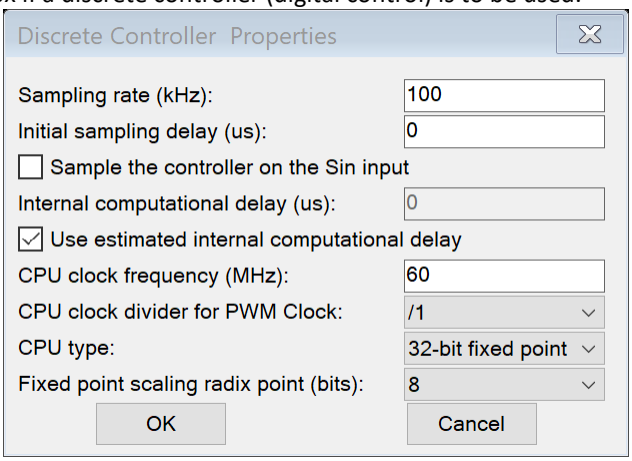
A multiplier signal can be used to form the current regulation waveform (usually input current for PFC converters).

Current multiplier input Iref internal DC gain:

Enter the internal DC gain of the current reference multiplier.

Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay

time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

CPU clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

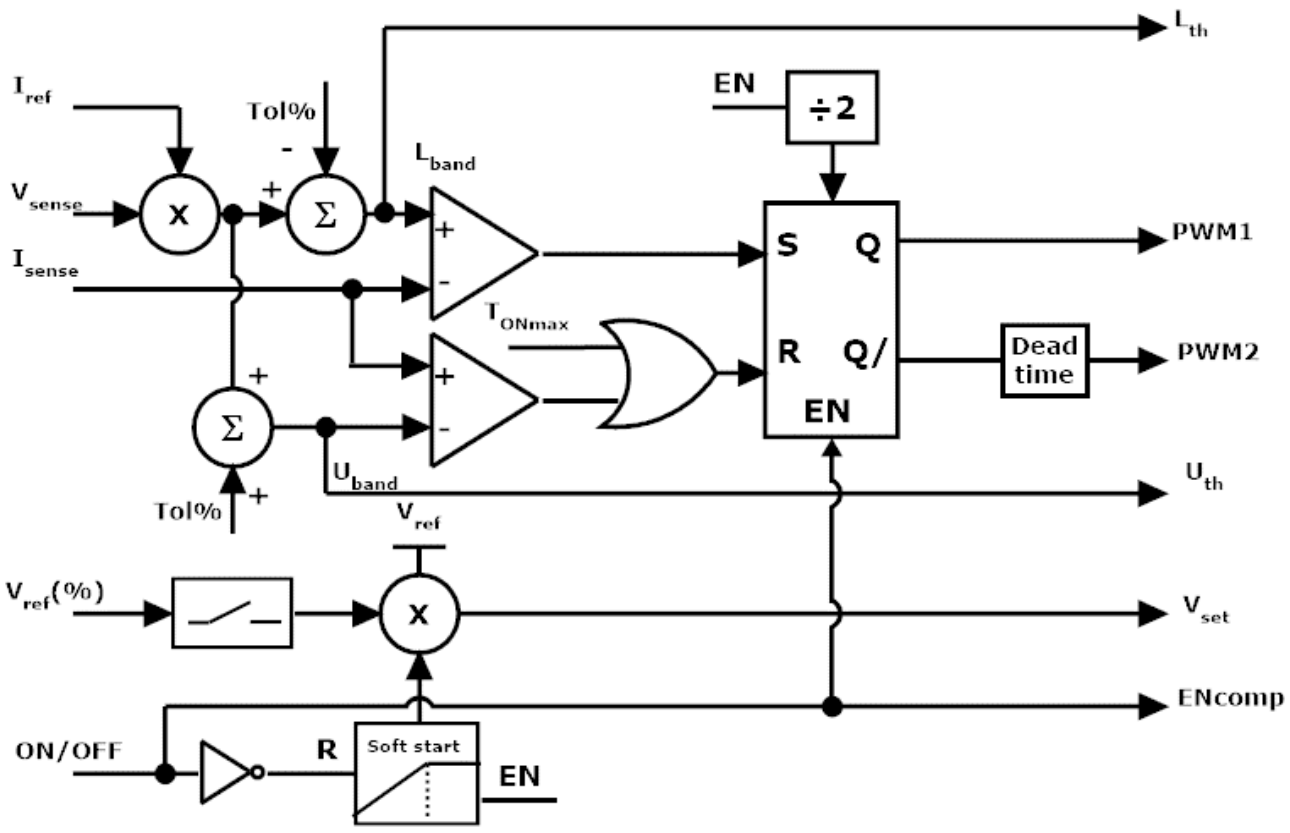
Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

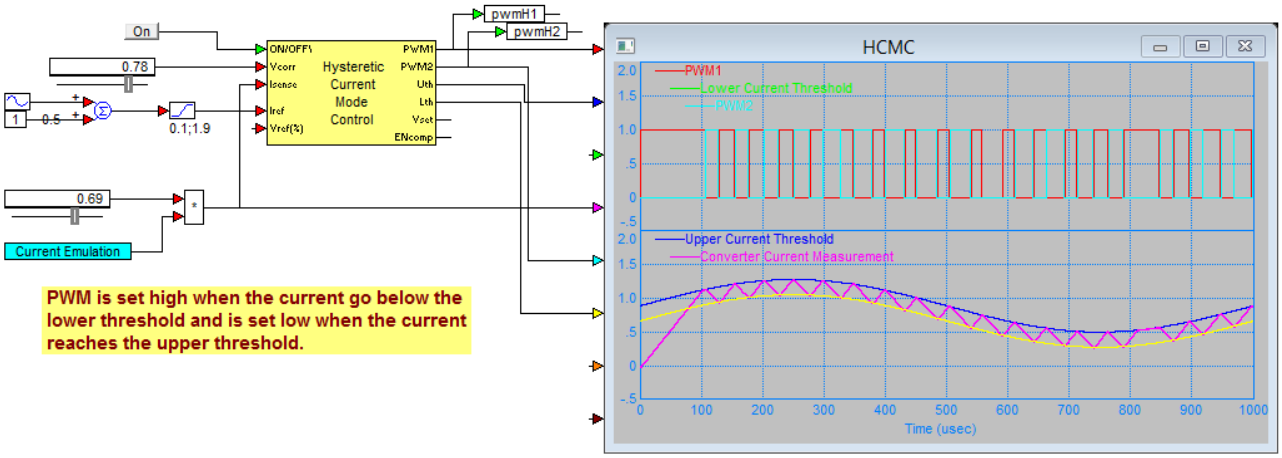
Use Vref profile:

Check this box to enable the use of the input Vref% pin.

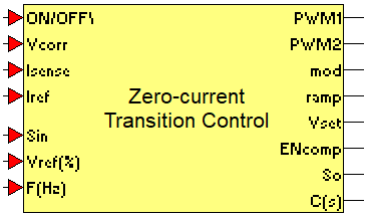
The following figure is a functional block diagram of the hysteretic current-mode controller detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.



The following figure demonstrates the hysteretic current mode controller and the corresponding Embed example diagram can be found under [Digital Power > Examples > Simulation > Controllers >HCMC – ZCMC.vsm]():



[Contents - Simulation]()



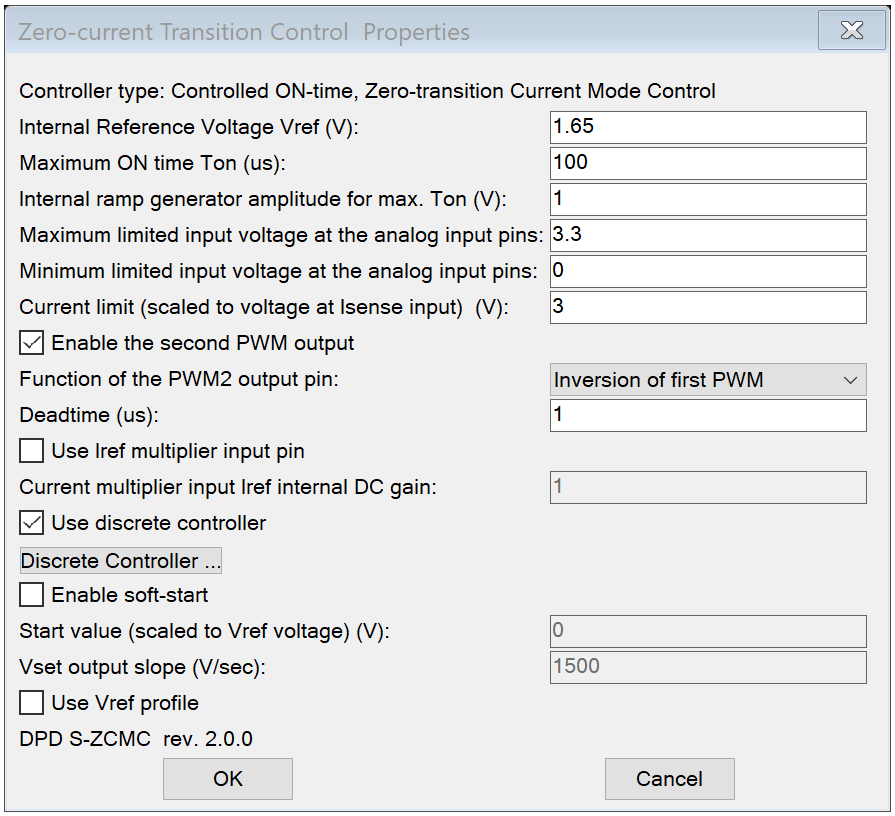
Zero-transition current mode controller (ZCMC)

Zero-transition current mode control generates an upper band which limit the peak current. The lower limit of the current is the zero level. This control method therefore forces the converter to operate in boundary conduction mode. This control is generally easier to compensate for but results in a variable switching frequency.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the voltage mode controller.
	Vcorr	Input pin usually from the output of a compensator.
	Isense	Current sense measurement pin. This measurement is required for zero transition control of the current.
	Iref	Current reference input. This input is multiplied with the internal correction signal in order for the current to follow a particular form e.g in PFC applications.
	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and “Sample the controller on the Sin pin” is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if “Use Vref profile” is checked.
	F (Hz)	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output pins:	**PWM1**	The pulse-width modulated (PWM) output which can be connected to a power converter SW input.
	PWM2	A second pulse-width modulated (PWM) output which can be connected to a power converter SWS input for synchronous converters or the SW input for converters with two control switches such as the half-bridge, full-bridge and push-pull converters. Note that this pin is only active when the “Enable the second PWM output” option is checked.
	mod	The internal modulation which along with the ramp determines the duty cycle of the PWM output.
	Ramp	The internal control ramp at the PWM frequency.
	Vset	This is the set point voltage sent out to this pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.
	ENcomp	This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.
	So	When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).
	C(s/z)	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The voltage mode controller block properties menu is shown in the following box which appears when right-clicking on the block.



Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Maximum ON time, Ton:

Enter the maximum ON time to limit the turn on period of the main switch.

Internal PWM ramp generator amplitude for max. Ton (V):

Enter the peak voltage of the internal up ramp generator used to determine the maximum ON time.

Maximum limited input voltage at the analog input pins:

This value sets the upper limit on the input measurements of the block particularly at the Iref input.

Minimum limited input voltage at the analog input pins:

This value sets the lower limit on the input measurements of the block.

Current limit (scaled to voltage at Isense input):

A current limit value can be set here with the appropriate scaling as seen by the input Isense pin. The peak current in zero transition control is twice the average current however there is no control limiting this value and therefore the additional current limitation is required.

Enable second PWM output:

If this box is checked, the second PWM output will be activated.

Function of the PWM2 output:

The choices are:

1. Inversion of first PWM
2. Alternating PWM (F = Fsw/2).

In case 1, the second PWM output will be a direct inversion of the first PWM output. In this case, the dead-time is applied to the leading edge and rising edge of the second PWM output, maintaining the set duty cycle. The second PWM output in this case is applicable for synchronous converters.

In case 2, the two PWM outputs will alternate and be modulated with a 180° phase shift. The switching frequency will be half the given frequency (for each PWM output). In this case, the dead-time is applied to the rising edge of each PWM output, reducing the duty cycle according to the ratio of the dead-time to the switching period. This PWM scheme is useful for controlling converters with dual, alternate control switches or combinations of switches such as the half-bridge, full-bridge and push-pull converters.

Dead-time:

Enter the desired dead-time in microseconds.

Use Iref multiplier pin:

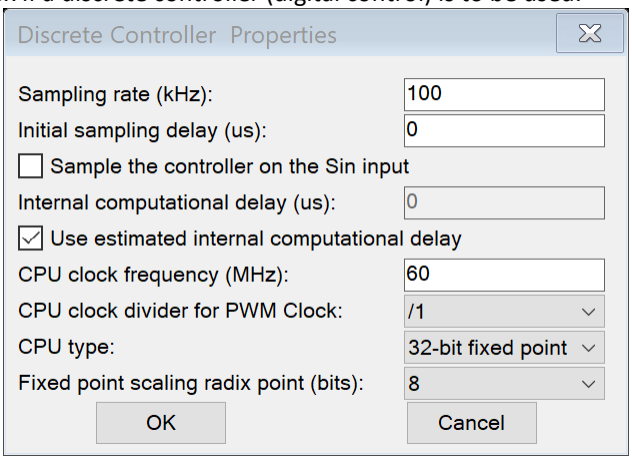
A multiplier signal can be used to form the current regulation waveform (usually input current for PFC converters).

Current multiplier input Iref internal DC gain:

Enter the internal DC gain of the current reference multiplier.

Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay

time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

CPU clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.
e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

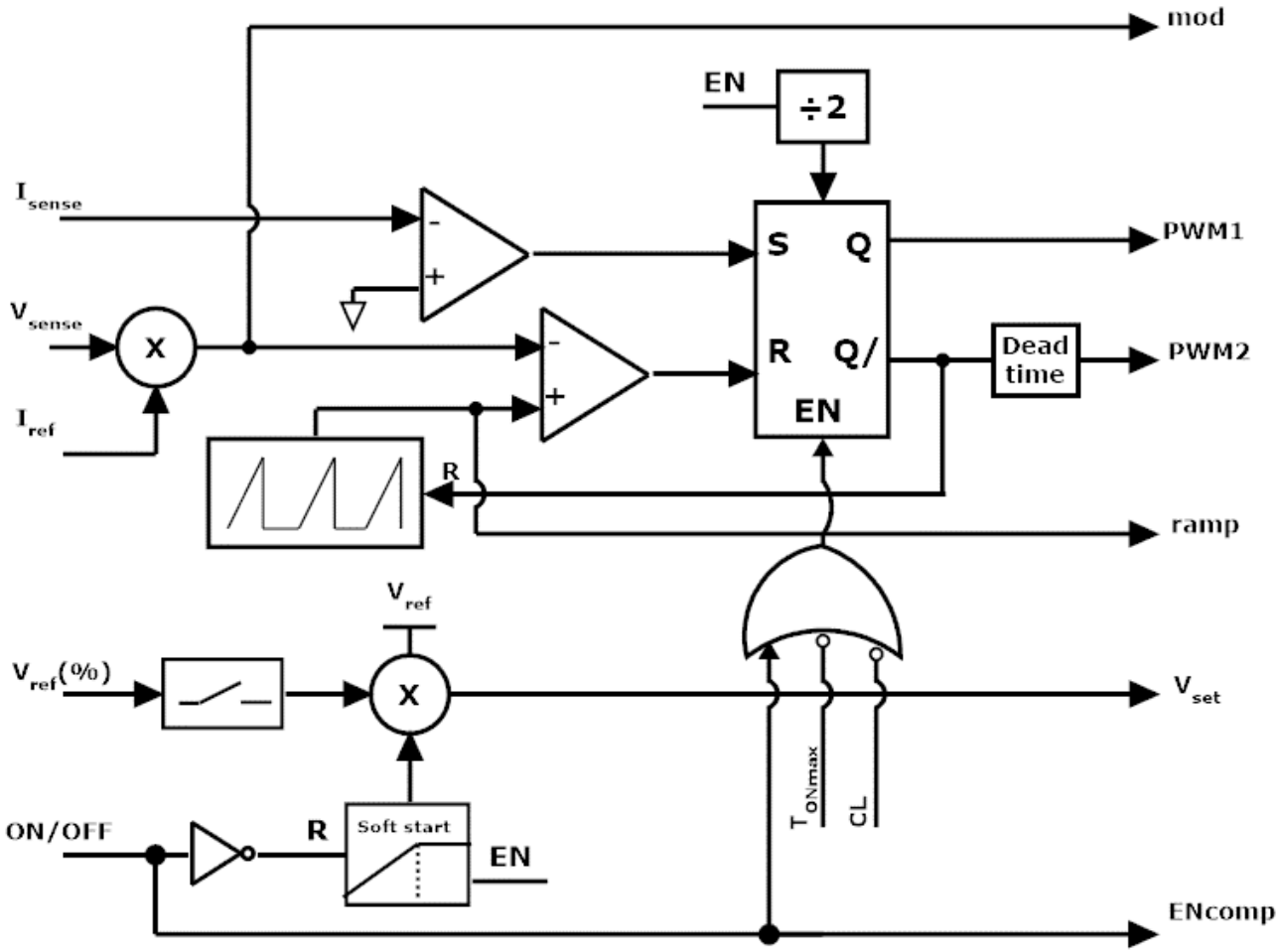
Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

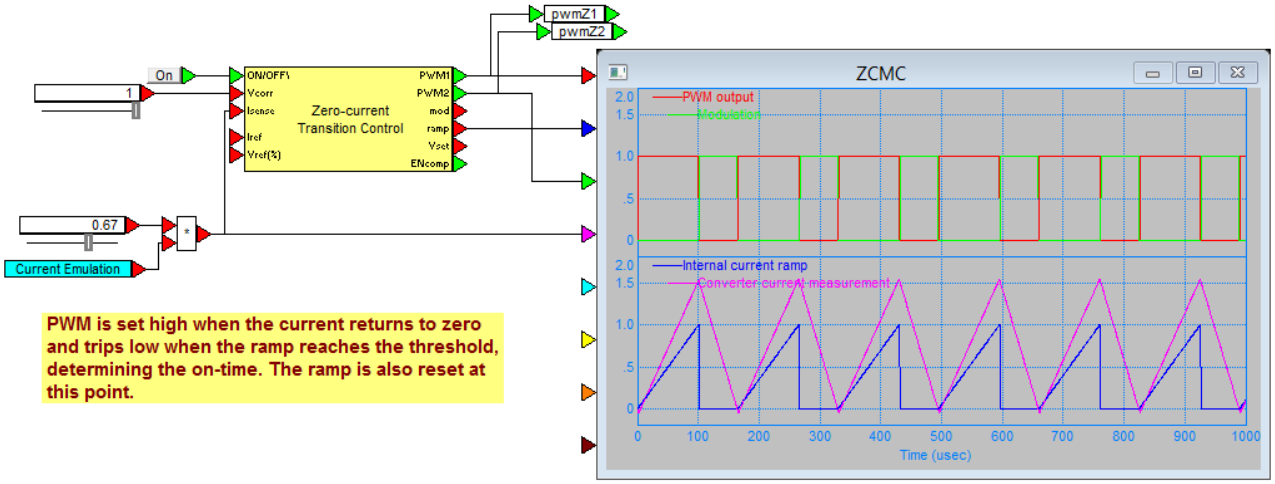
Use Vref profile:

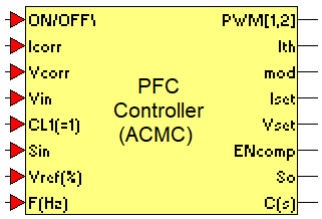
Check this box to enable the use of the input Vref% pin.

The following figure is a functional block diagram of the zero-transition current-mode controller detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.



The following figure demonstrates the operation of the zero-transition current mode controller and the corresponding Embed example diagram can be found under [Digital Power > Examples > Simulation > Controllers >HCMC – ZCMC.vsm]():





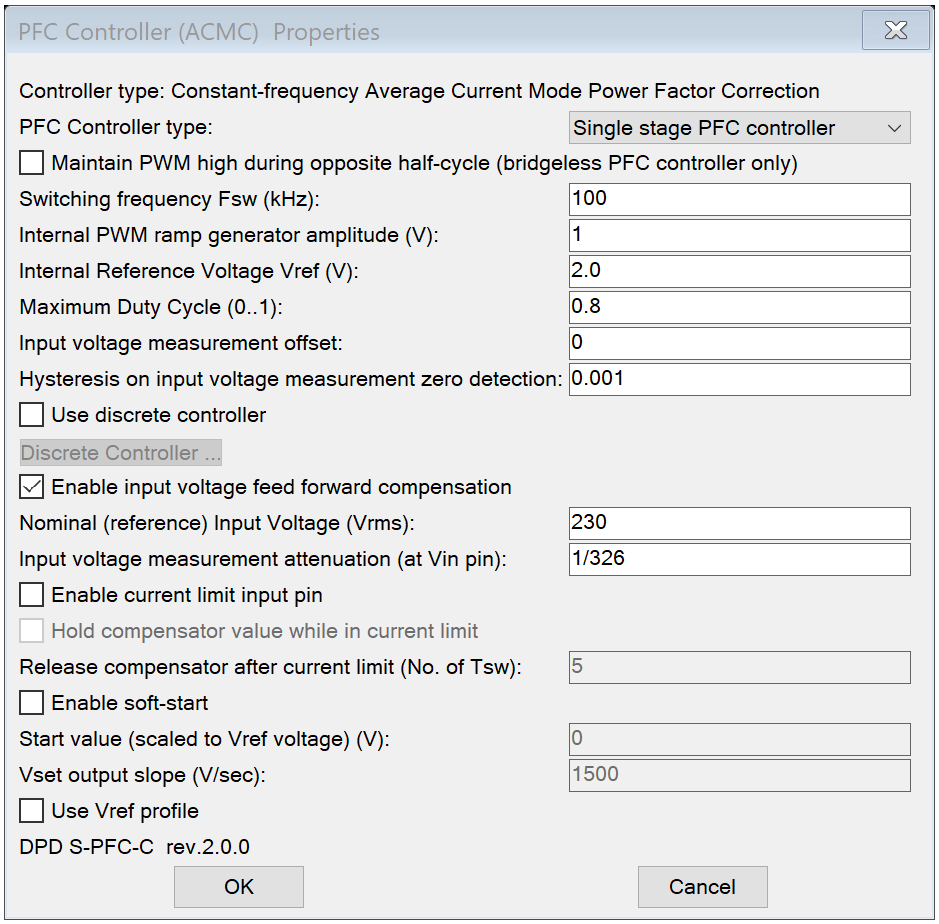
Power Factor Correction Controller (PFC)

This controller uses average mode control to implement a power factor correction controller.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the PFC controller.
	Icorr	Input pin from the input current compensator for PFC current correction.
	Vcorr	Input pin from the output voltage compensator for output voltage regulation.
	Vin	Converter input voltage measurement.
	CL (=1)	Current limit trigger input. A value ≥ 1 activates the current limit, switching off the output PWM to be reset on the next switching cycle – a cycle-by-cycle (CBC) current limit.
	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and "Sample the controller on the Sin pin" is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if "Use Vref profile" is checked.
	F (Hz)	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output pins:	**PWM[1,2]**	The pulse-width modulated (PWM) output which can be connected to the PFC converter SW inputs; vector, rows = 1, columns = 2.
	Vth	Internal voltage threshold (ramp).
	mod	The internal modulation which along with the ramp determines the duty cycle of the PWM output.
	Iset	This is the set point voltage sent out to the current compensator input reference pin.
	Vset	This is the set point voltage sent out to the voltage compensator input reference pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.
	ENcomp	This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.
	So	When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).
	C(s/z)	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The PFC controller block properties menu is shown in the following box which appears when right-clicking on the block.



PFC Controller type:

The choices here are:

1. Single stage PFC controller (PWM1 controlled, PWM2 = 0)
2. Dual-interleaved PFC controller (PWM2 slaved to PWM1 at 180°).
3. PWM bridge PFC controller (PWM1 an PWM2 on alternately).
4. Bridgeless PFC controller (PWM1 and PWM2 individually controlled).

Maintain PWM high during opposite half-cycle:

For the bridgeless PFC controller only, the second PWM switch for the return current can be maintained on during the opposing half cycle of the mains input.

Switching frequency:

Enter the required switching frequency of the power converter to be controlled. This will set the output PWM frequency.

Internal PWM ramp generator amplitude (V):

Enter the peak voltage of the internal up ramp generator (usually = 1 but can be any value > 0).

Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Maximum duty cycle:

Enter the maximum duty cycle. This will limit the duty cycle so that it cannot exceed this given value. If not used, the value should be equal to 1.

Input voltage measurement offset:

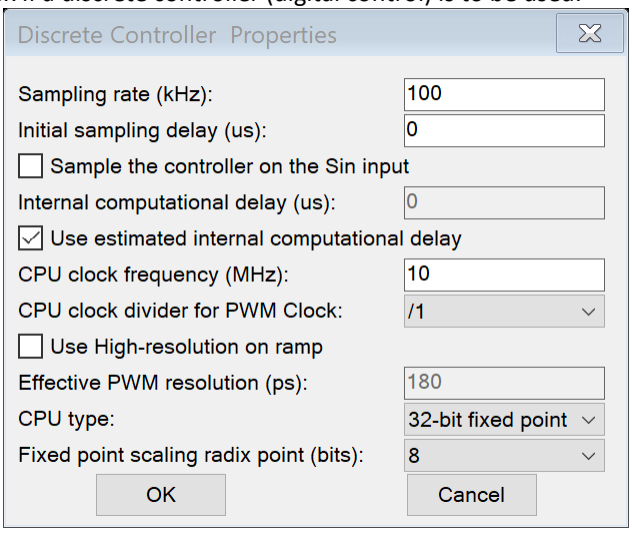
The input AC voltage maybe offset to allow it to be measured by a sensor that does not accept negative voltages. In that case, enter the voltage of the input voltage measurement offset here.

Hysteresis on input voltage measurement zero detection:

For noisy input AC voltages it may be advantageous to include a hysteresis on the detection of the zero crossings of the input AC mains voltages. This is mainly used for the bridgeless PFC controller where the positive and negative halves must be detected. The hysteresis will be ±half of the given value.

Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

CPU clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

Use high resolution on ramp:

Select this if the default resolution of the PWM is not used and a higher resolution is required. The high-resolution will be implemented internally on the ramp.

Effective PWM resolution (ps):

In the case of high-resolution, enter the effective resolution of the output PWM in picoseconds. This will be implemented into the ramp resolution. Note that this option can be used for any value of resolution.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

Enable input voltage feed forward compensation:

Check this box to enable input voltage feed-forward compensation.

Nominal input (reference) voltage Vrms:

Enter the nominal rms input voltage in volts.

Input voltage measurement attenuation:

Enter the attenuation on the input voltage measurement seen at the Vin input pin of the controller.

Enable current limit input pin:

Check this box to enable current limiting of the PWM output (determined by the input pin CL).

Hold compensator value while in current limit:

If this box is checked, the compensator is disabled with its internal values “frozen” while the current limitation persists. The compensator will be released when the current limitation is removed.

Release compensator after current limit:

Enter the number of switching cycles that the compensator is to remain frozen after the removal of the current limitation. The minimum amount of cycles for the control feature to remain active is two, while in practise this would be longer due to filtering of a noisy measurement.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

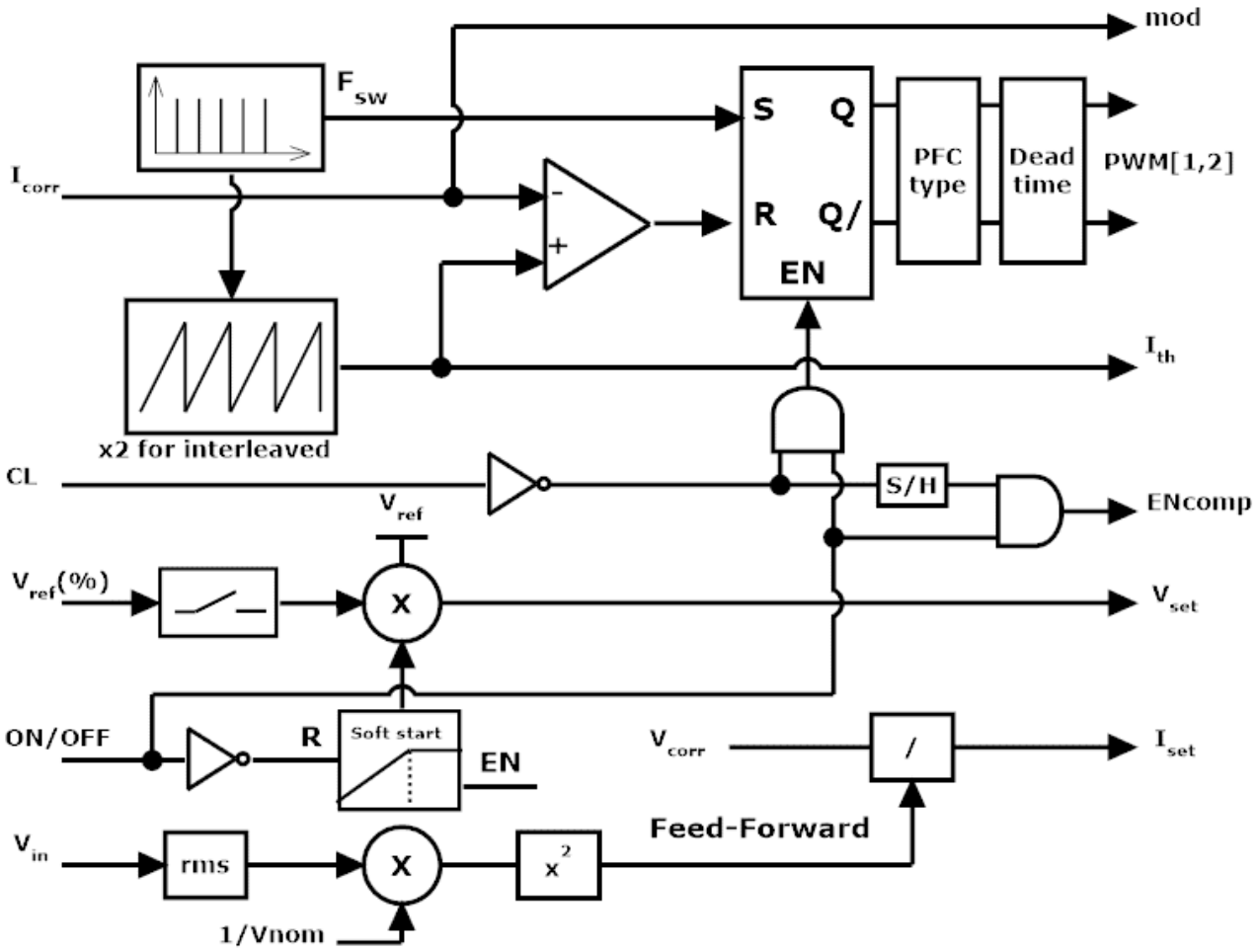
Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

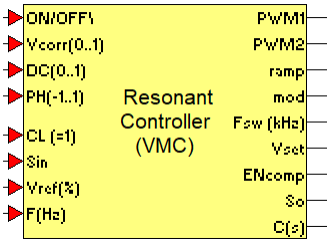
Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

Use Vref profile:

Check this box to enable the use of the input Vref% pin.
The following figure is a functional block diagram of the power factor correction (PFC) average current-mode controller detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.





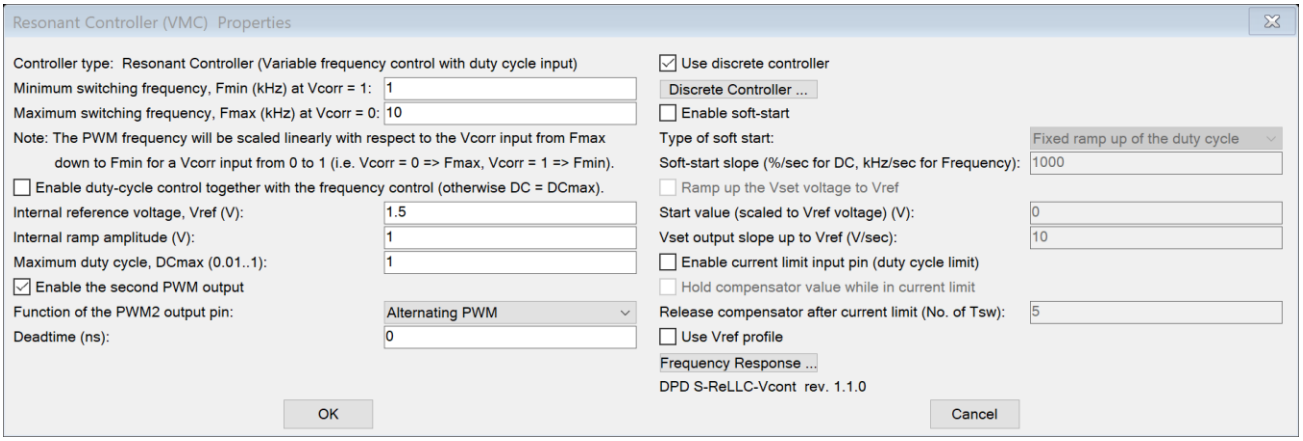
Resonant Converter Controller (VMC)

The resonant converter controller can be used to control resonant converters in voltage mode control by varying the switching frequency.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the resonant converter controller.
	Vcorr	Correction input for regulation which will control the switching frequency.
	DC	Input duty cycle control pin.
	PH	Converter input phase control pin.
	CL (=1)	Current limit trigger input. A value ≥ 1 activates the current limit, switching off the output PWM to be reset on the next switching cycle – a cycle-by-cycle (CBC) current limit.
	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and "Sample the controller on the Sin pin" is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if "Use Vref profile" is checked.
	F(Hz)	Frequency input pin for frequency domain analysis.
Output pins:	**PWM1,2**	The pulse-width modulated (PWM) outputs which can be connected to a resonant converter SW inputs.
	ramp	Internal voltage ramp generated by the controller.
	mod	The internal modulation which along with the ramp determines the duty cycle of the PWM output.
	Fsw (kHz)	This is the current set switching frequency within the controller in kHz.
	Vset	This is the set point voltage sent out to the voltage compensator input reference pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.
	ENcomp	This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.
	So	When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).
	C(s/z)	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The resonant controller block properties menu is shown in the following box which appears when right-clicking on the block.



Minimum switching frequency, Fmin:

Enter the minimum allowable switching frequency of the controller in kHz.

Maximum switching frequency, Fmax:

Enter the maximum allowable switching frequency of the controller in kHz.

The PWM switching frequency will be scaled linearly from Fmin to Fmax for the control input Vcorr over a range of 0 (Fmax) to 1(Fmin).

Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Internal ramp amplitude:

Enter the amplitude of the ramp voltage used to create the PWM output.

Maximum duty cycle:

Enter the maximum duty cycle. This will limit the duty cycle so that it cannot exceed this given value. If not used, the value should be equal to 1.

Enable second PWM output:

If this box is checked, the second PWM output will be activated.

Function of the PWM2 output:

The choices are:

1. Inversion of first PWM
2. Alternating PWM (F = Fsw/2).

In case 1, the second PWM output will be a direct inversion of the first PWM output. In this case, the dead-time is applied to the leading edge and rising edge of the second PWM output, maintaining the set duty cycle. The second PWM output in this case is applicable for synchronous converters.

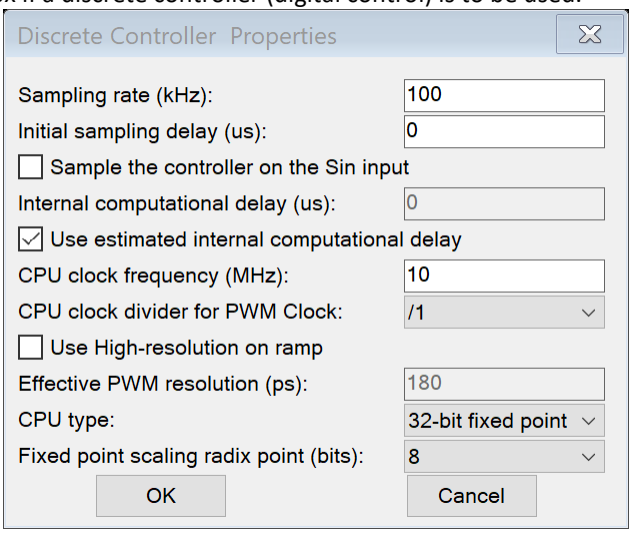
In case 2, the two PWM outputs will alternate and be modulated with a 180° phase shift. The switching frequency will be half the given frequency (for each PWM output). In this case, the dead-time is applied to the rising edge of each PWM output, reducing the duty cycle according to the ratio of the dead-time to the switching period. This PWM scheme is useful for controlling converters with dual, alternate control switches or combinations of switches such as the half-bridge, full-bridge and push-pull converters.

Dead-time:

Enter the desired dead-time in micro-seconds

Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

CPU clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

Use high resolution on ramp:

Select this if the default resolution of the PWM is not used and a higher resolution is required. The high-resolution will be implemented internally on the ramp.

Effective PWM resolution (ps):

In the case of high-resolution, enter the effective resolution of the output PWM in picoseconds. This will be implemented into the ramp resolution. Note that this option can be used for any value of resolution.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Type of soft start:

The choices hare are:

1. Fixed ramp up of the duty cycle
2. Fixed ramp down of the frequency

Soft-start slope :

This value will be in % of duty cycle / second for case 1 or kHz / second for case 2.

Ramp up the Vset voltage to Vref:

Select this if none of the first two soft-start types are to be used and the Vset voltage is ramped up instead as in a traditional soft-start method.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

Enable current limit input pin:

Check this box to enable current limiting of the PWM output (determined by the input pin CL).

Hold compensator value while in current limit:

If this box is checked, the compensator is disabled with its internal values “frozen” while the current limitation persists. The compensator will be released when the current limitation is removed.

Release compensator after current limit:

Enter the number of switching cycles that the compensator is to remain frozen after the removal of the current limitation. The minimum amount of cycles for the

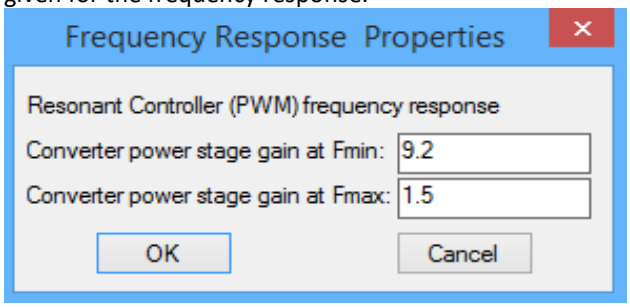
control feature to remain active is two, while in practise this would be longer due to filtering of a noisy measurement.

Use Vref profile:

Check this box to enable the use of the input Vref% pin.

Frequency response:

The converter power stage gain at the minimum and maximum frequencies can be given for the frequency response.



The following two parameters are used to determine the frequency response of the resonant controller when used together with the resonant converter and the model-based frequency response tool in a diagram.

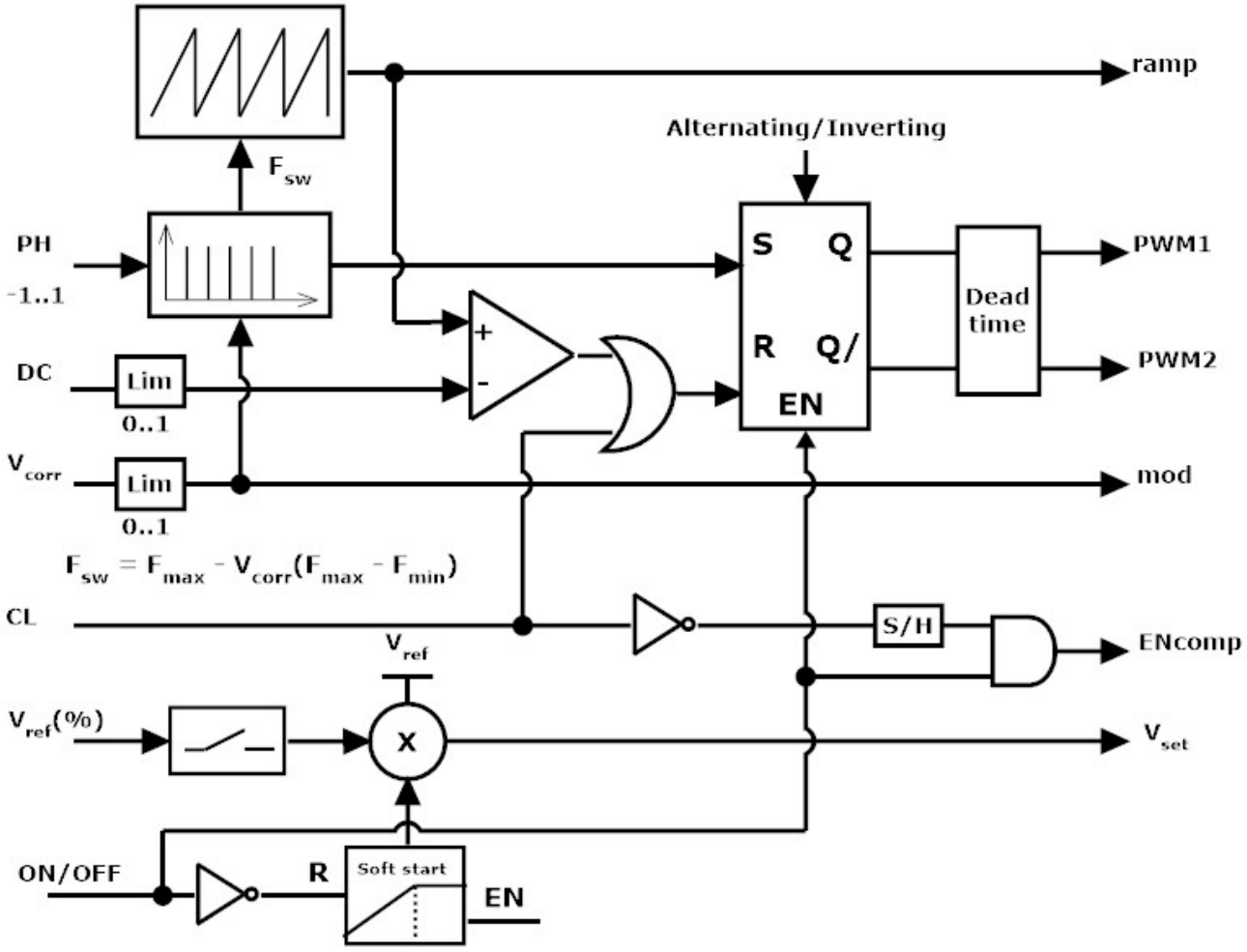
Converter power stage gain at Fmin:

Enter the expected power stage gain at the minimum switching frequency.

Converter power stage gain at Fmax:

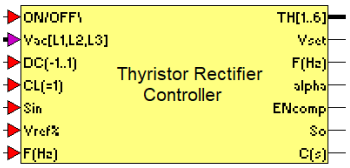
Enter the expected power stage gain at the maximum switching frequency.

The following figure is a functional block diagram of the resonant converter controller (voltage-mode) detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.



An example on the resonant converter controller can be found at: Digital Power > Examples > Simulation > Controllers >Resonant Controller

Contents - Simulation



Thyristor Rectifier Controller

The thyristor rectifier controller is suitable for driving controlled rectifiers using thyristor switches. It can drive single-phase and three-phase controlled-rectifiers, both half-wave and full-wave.

Input Pins:

Vac — Input AC voltage pin (V); vector, rows = 1, columns = 3. For single-phase, only the first phase is considered.

DC — The control input expressed as a duty cycle from 0 to 1. Note that the DC input will not be linearly proportional to the output voltage but rather inversely proportional to the firing angle. An input of DC = 0 corresponds to an alpha of 90°, while a DC = 1 input corresponds to an alpha of 0°.

CL (=1) — Current limit trigger input. A value ≥ 1 activates the current limit, switching off the output PWM to be reset on the next switching cycle – a cycle-by-cycle (CBC) current limit.

Sin — Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and "Sample the controller on the Sin pin" is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.

Vref% — The input to this pin (in percent) will vary the internally set Vref voltage (only active if "Use Vref profile" is checked.

F (Hz) — Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.

Output pins:

TH[1..6] — The thyristor control output pulses which can be connected to a thyrsitor rectifier TH inputs; vector, rows = 1, columns = 6. Only the first four are active for a single-phase controller.

Vset — This is the set point voltage sent out to the voltage compensator input reference pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.

F (Hz) — The internally measured mains frequency in Hertz.

alpha — The firing angle in degrees.

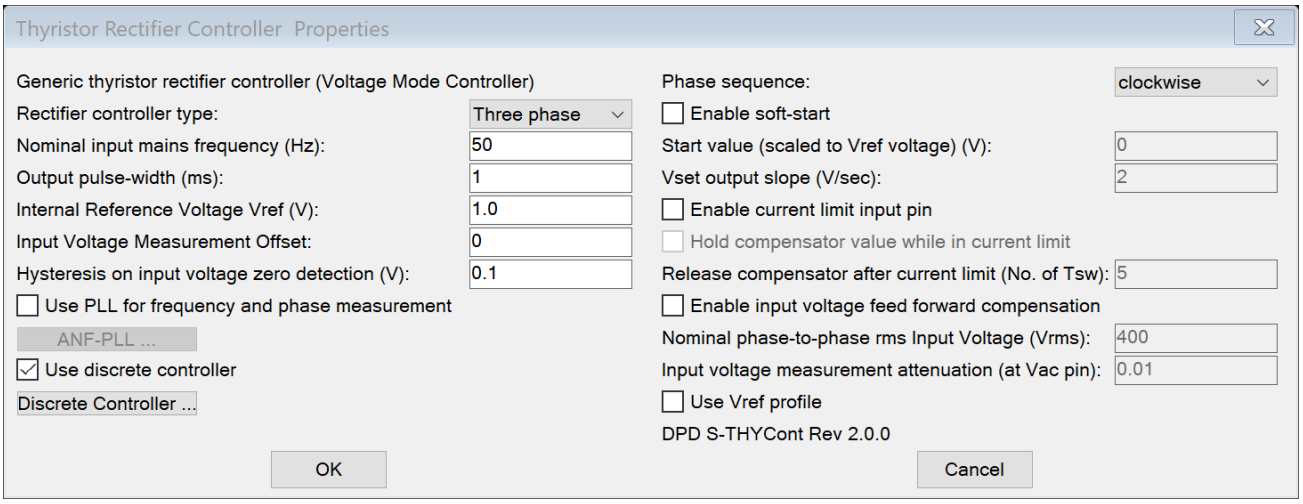
ENcomp — An enable output which is typically connected to a compensator block.

So — When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).

C(s/z) — When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The thyristor rectifier controller block properties menu is shown in the following box which appears when right-clicking on the block.



Rectifier Controller type:

The choices here are:

1. Single-phase rectifier controller (4 controller outputs active)
2. Three-phase rectifier controller (6 controller outputs active).

Nominal mains frequency:

Enter the nominal mains frequency of the input voltage in Hertz.

Output pulse width:

The pulse-width of the thyristor output control vector pin can be set here in milli-seconds. A small pulse is in general sufficient to switch on a thyristor.

Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Input voltage measurement offset:

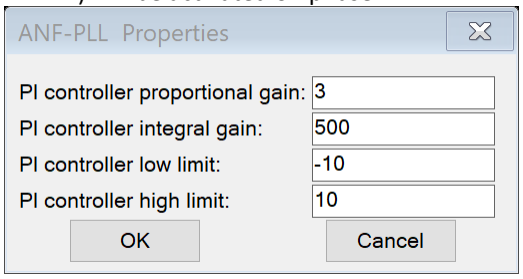
The input AC voltage maybe offset to allow it to be measured by a sensor that does not accept negative voltages. In that case, enter the voltage of the input voltage measurement offset here.

Hysteresis on input voltage measurement zero detection:

For noisy input AC voltages (or those affected by thyristor commutation) , it may be advantageous to include a hysteresis on the detection of the zero crossings of the input AC mains voltages. The hysteresis will be ±half of the given value. This is not active if a PLL is used.

Use PLL for frequency and phase measurement:

Select this option if a PLL is desired to perform the frequency measurement (for the regulating phase delay) and the phase synchronisation. An adaptive notch filter phase lock loop (ANF-PLL) will be activated on phase L1.



PI controller proportional gain:

Insert the value of the proportional gain of the PI controller used to regulate the PLL output.

PI controller integral gain:

Insert the value of the integral gain of the PI controller used to regulate the PLL output.

PI controller low limit:

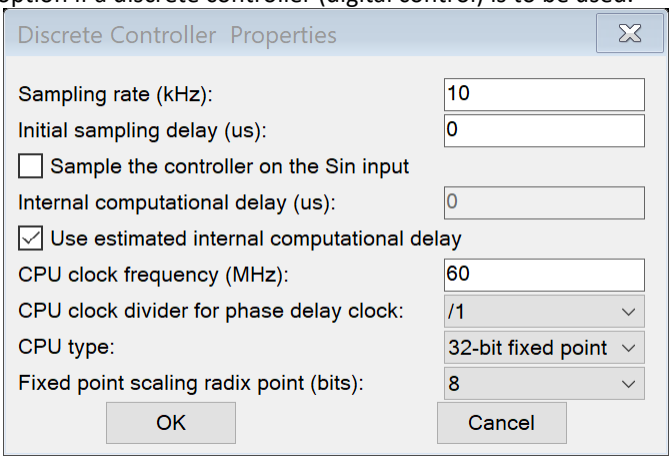
Insert the value of the low limit of the PI controller used to regulate the PLL output.

PI controller high limit:

Insert the value of the high limit of the PI controller used to regulate the PLL output.

Use discrete controller:

Select this option if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

CPU clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

Phase sequence:

Select the phase sequence of the input voltage waveforms for three-phase systems, either clockwise or anti-clockwise.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

Enable current limit input pin:

Check this box to enable current limiting (enables the input pin CL).

Hold compensator value while in current limit:

If this box is checked, the connected compensator will be disabled with its internal values “frozen” while the current limitation persists. The compensator will be released when the current limitation is removed (ENcomp output pin).

Release compensator after current limit:

Enter the number of switching cycles that the compensator is to remain frozen after the removal of the current limitation. The minimum amount of cycles for the control feature to remain active is two, while in practise this would be longer due to filtering of a noisy measurement.

Enable input voltage feed forward compensation:

Check this box to enable input voltage feed-forward compensation.

Nominal phase-to-phase rms input voltage Vrms:

Enter the nominal phase-to-phase rms input voltage in volts for a three-phase controller or the nominal phase-to-neutral rms input voltage for a single-phase controller.

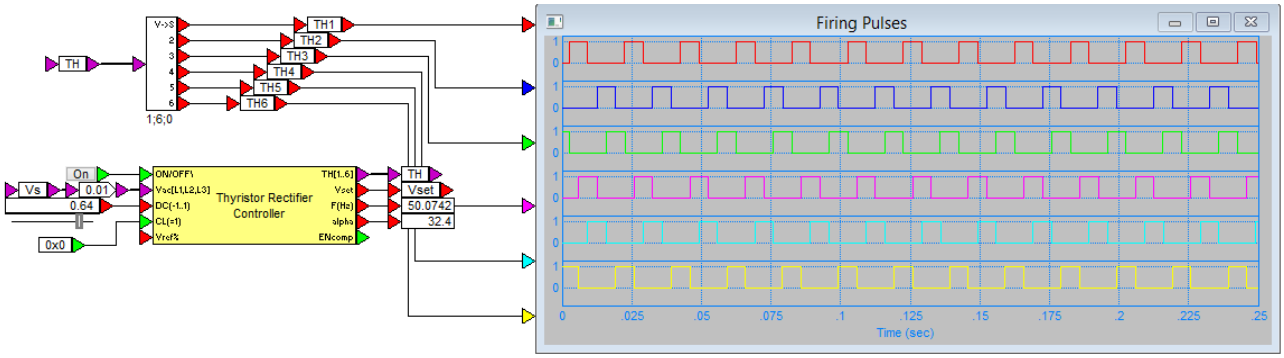
Input voltage measurement attenuation (at Vac input pin):

Enter the attenuation on the input voltage measurement seen at the Vac input pin of the controller.

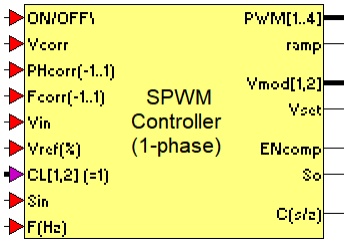
Use Vref profile:

Check this box to enable the use of the input Vref% pin.

The following figure demonstrates the thyristor rectifier controller and the corresponding Embed example diagram can be found under Digital Power > Examples > Simulation > Controllers >Thyristor Rectifier Controller.vsm:



Contents - Simulation



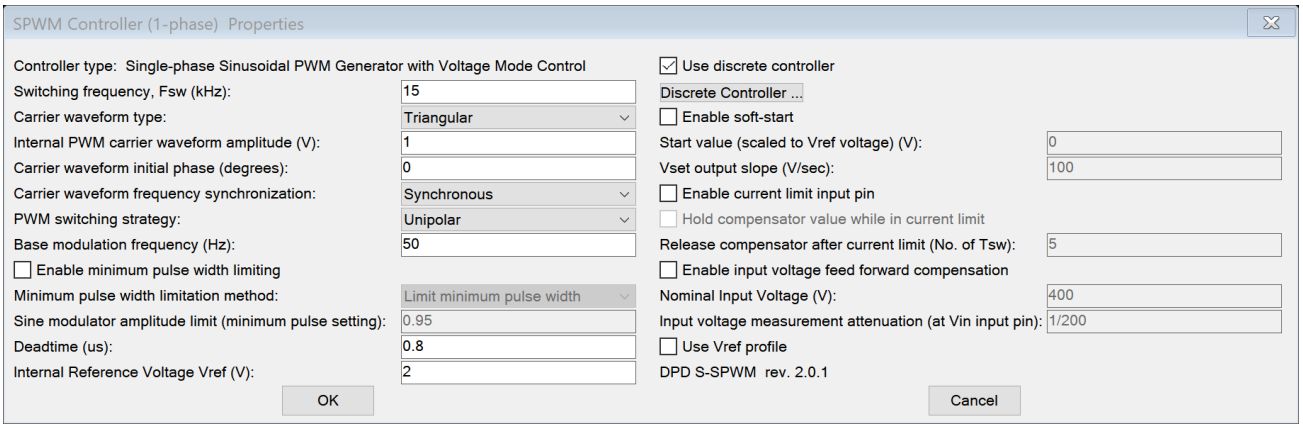
SPWM Voltage mode controller (1-phase)

This block models single-phase sinusoidal-modulator pulse width modulation used for AC-DC rectifier control or DC-AC inverters. Several different types of modulation strategies are selectable and described in this section.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the voltage mode controller.
	Vcorr	Input pin usually from the output of a compensator.
	PHcorr (-1..1)	Input pin to control the phase of the modulator waveform (sinusoidal).
	Fcorr (-1..1)	Input pin to control the frequency of the modulator waveform.
	Vin	Input voltage (DC) measurement pin. This measurement is used for feed-forward compensation in VMC.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if "Use Vref profile" is checked.
	CL (=1)	Current limit trigger input vector. A value ≥ 1 activates the current limit, switching off the respective PWM outputs to be reset on the next switching cycle – a cycle-by-cycle (CBC) current limit.
	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and "Sample the controller on the Sin pin" is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	F (Hz)	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output pins:	**PWM[1..4]**	The pulse-width modulated (PWM) output which can be connected to a single-phase power inverter SW input.
	Ramp	The internal control ramp at the PWM frequency.
	Vmod[1,2]	The internal modulation which along with the ramp determines the duty cycle of the PWM output. This can be one or two separate modulators depending upon the PWM switching strategy selected.
	Vset	This is the set point voltage sent out to this pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.
	ENcomp	This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.
	So	When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).
	C(s/z)	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The SPWM voltage mode controller block properties menu is shown in the following box which appears when right-clicking on the block.



Switching frequency:

Enter the required switching frequency in kHz of the power converter to be controlled. This will set the ramp frequency and therefore the output PWM frequency.

Carrier waveform type:

The choices are:

1. Sawtooth rising (leading-edge modulation)
2. Sawtooth falling (falling-edge modulation)
3. Triangular (dual-edge modulation)

The carrier waveform can be selected as desired. A triangular carrier waveform is normally selected due to better symmetry and less harmonic content in the resultant PWM waveform.

Internal Carrier waveform amplitude:

Insert the carrier waveform amplitude to correspond with the modulation (Vcorr input).

Carrier waveform initial phase (degrees):

The initial phase of the carrier waveform can be entered. This phase is then relative to the modulator waveform. Also, interleaving can be achieved with multiple controllers / inverter stages.

Carrier waveform frequency synchronisation:

The choices are:

1. Asynchronous
2. Synchronous

For an asynchronous carrier waveform the carrier frequency is not locked to the modulation frequency and asymmetries may be present in the resulting PWM waveform. If a synchronous carrier waveform is selected, the initial ratio of the carrier (switching) frequency to the modulator frequency is set to an integer and is maintained with variations of the modulator frequency. The switching frequency will therefore vary with time with respect to the modulator frequency.

PWM switching strategy:

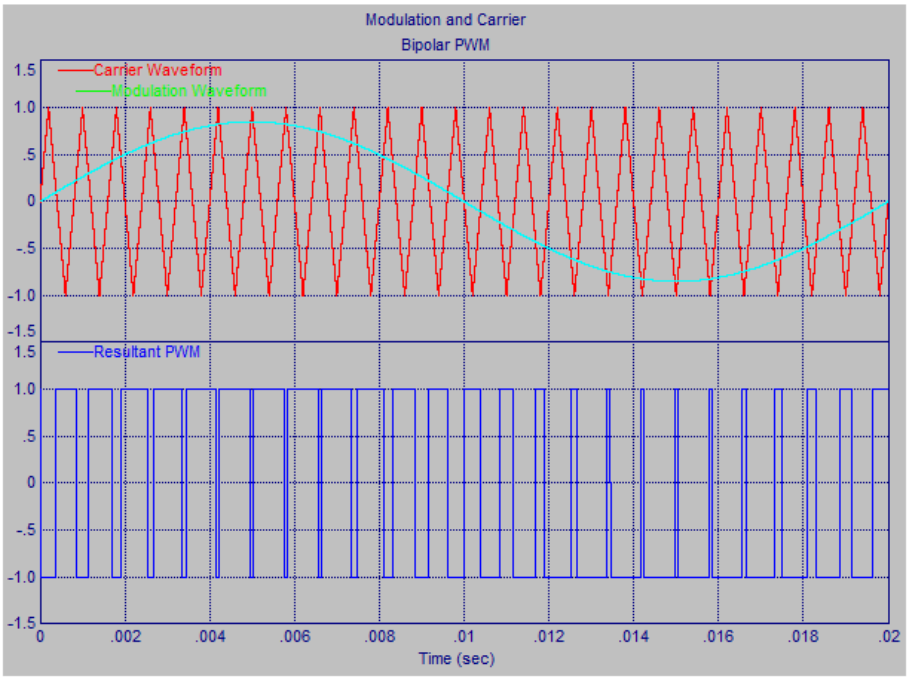
The choices are:

1. Bipolar
2. Unipolar
3. Hybrid
4. Hybrid (alternating inverted carrier)

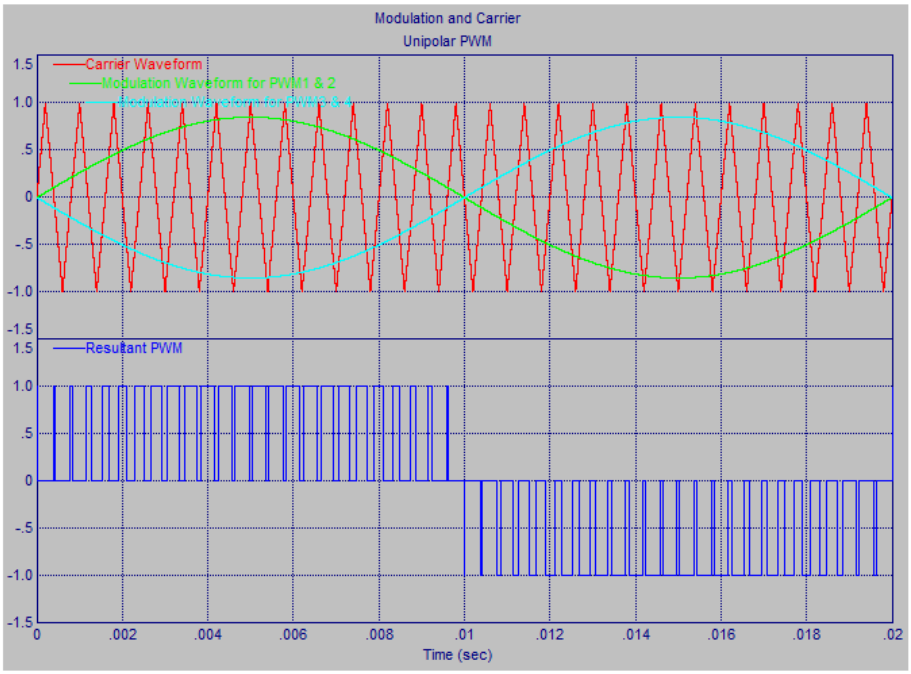
5. Distributed hybrid

The following is a summary of the five PWM strategies available. All plots are with a carrier frequency (triangle) of 1.25 kHz and a modulator frequency (generally a sinusoid) of 50 Hz.

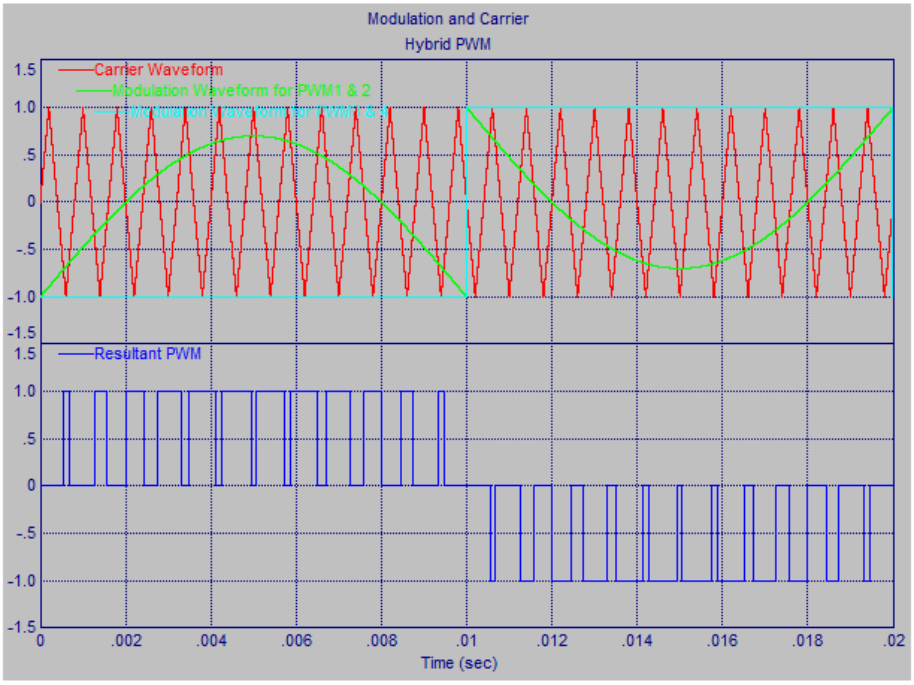
1. Bipolar PWM uses one sine modulator with PWM1 and PWM4 being switched together while PWM2 and PWM3 are switched together and opposed to the first pair.



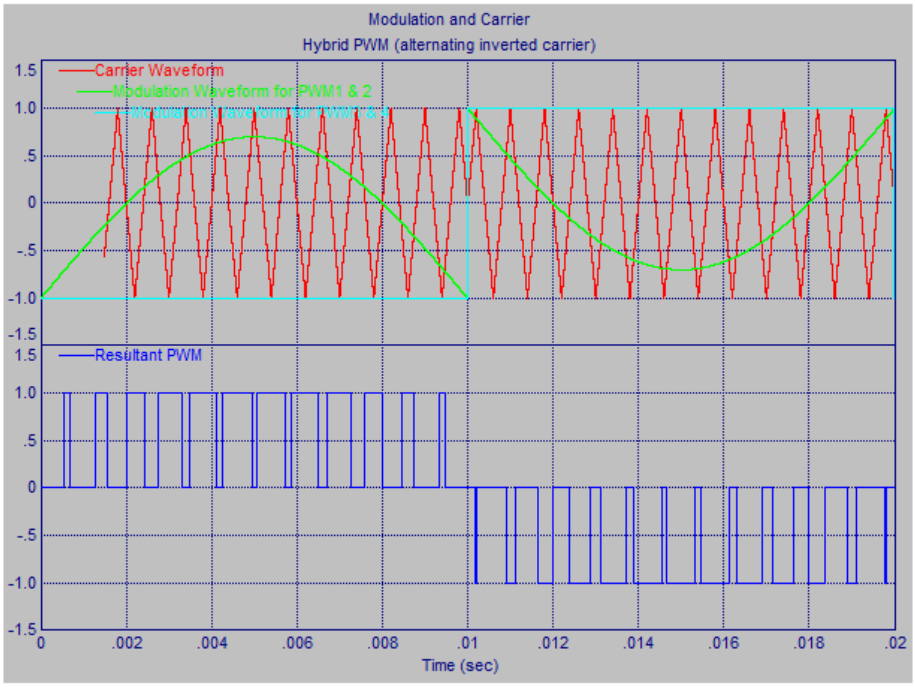
2. Unipolar PWM uses two sine modulators, the second carrier 180° phase shifted with respect to the first sine modulator. Note that the effective PWM output frequency is twice that of the switching frequency.



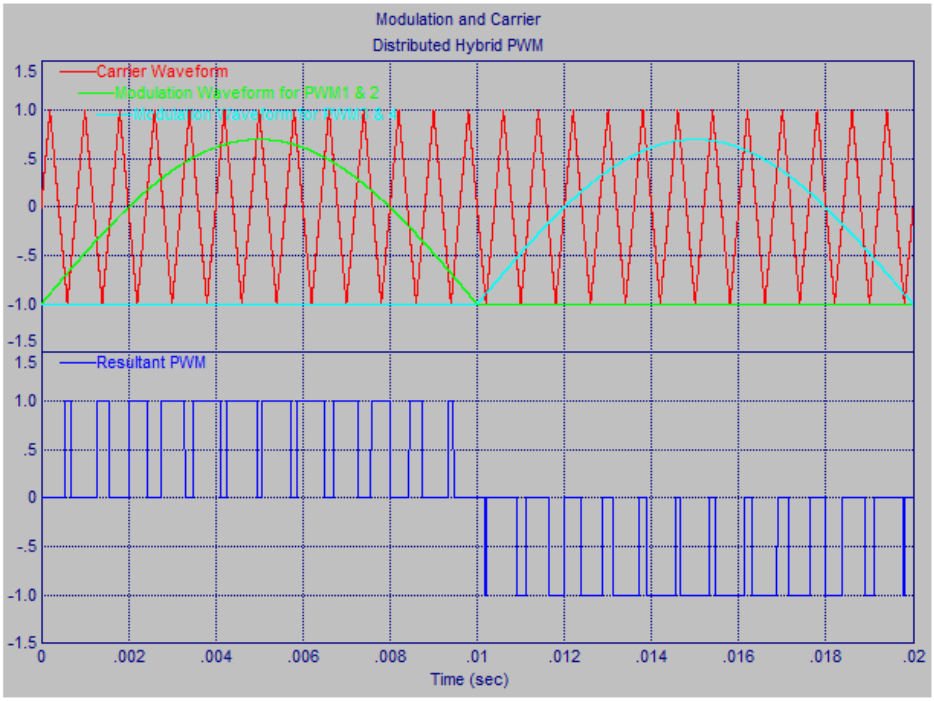
3. Hybrid PWM uses two modulators, the first with a full-amplitude offset over alternate half periods and the second a square wave at the modulator frequency. With this strategy, one leg of the inverter bridge switches at the switching frequency while the other leg switches at the modulator frequency.



4. Hybrid PWM (with an alternating inverted carrier waveform) is identical to the hybrid PWM technique in 3 above, except that the carrier waveform is inverted at each half modulator period in order to maintain the symmetry of each half cycle of the resultant output PWM.



5. Distributed Hybrid PWM has two modulators, each a half sine-wave so that one leg of the inverter bridge will switch at the switching frequency while the other leg switches at the modulator frequency as in the hybrid PWM technique, except that in this case the two legs will alternately switch at the switching frequency and therefore distributing the switching losses over all four switches.



Base modulation frequency:

Enter the frequency of the modulating waveform. This can be held constant or varied by connecting a control signal to the Fcorr input pin.

Enable minimum pulse-width limiting:

Check this box to enable minimum pulse-width limiting

Minimum pulse-width limitation method:

The choices are:

1. Limit minimum pulse-width
2. Use pulse skipping

Due to practical limitations, there is a minimum practical pulse-width of the PWM, due to the finite switch-on time of the inverter switching devices so that switching on a power switch for a period less than this minimum would not affect the output voltage but would however increase converter losses due to switches not being completely turned on and not being utilized in this brief interval. For the first selection, the pulse width is limited to a minimum value; in the second selection, the pulses are skipped if they are determined to be below the minimum limit.

Sine modulator amplitude limit:

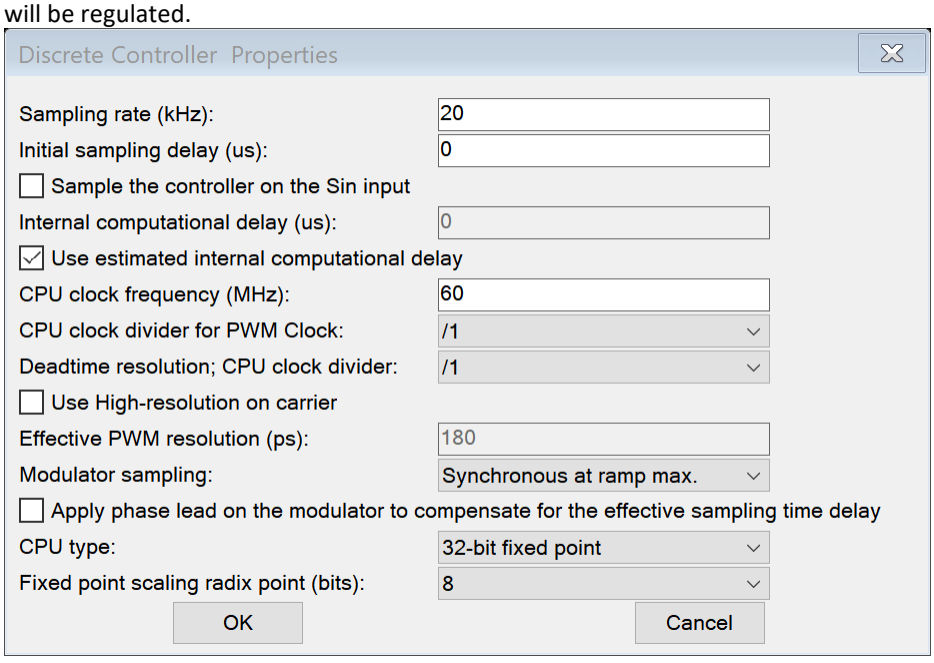
Enter a value less than 1 to limit the minimum pulse-width of the output PWM.

Dead-time:

Enter the desired dead-time in microseconds.

Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.



Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.

Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

Clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

Dead-time resolution; counter frequency (MHz):

Set the resolution of the dead-time period by entering the frequency of the dead-time counter in Mega-Hertz.

Use high resolution on carrier:

Select this if the default resolution of the PWM is not used and a higher resolution is required. The high-resolution will be implemented internally on the carrier waveforms.

Effective PWM resolution (ps):

Enter the effective resolution of the output PWM in picoseconds. This will be implemented into the ramp resolution.

Modulator sampling:

The choices are:

1. Asynchronous (at the given sampling frequency rate)
2. Synchronous at the minimum of the ramp (zero)
3. Synchronous at the maximum of the ramp (period)
4. Synchronous at the minimum and maximum ramp

This selection determines the moment at which the modulator is sampled with respect to the carrier waveform.

Apply phase lead on the modulator to compensate for the effective sampling delay:

Check this box to anticipate the modulator sine-wave to exactly the value to compensate for the sampling delay of the modulator.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

Enable current limit input pin:

Check this box to enable current limiting of the PWM output (determined by the input pin CL).

Hold compensator value while in current limit:

If this box is checked, the compensator is disabled with its internal values “frozen” while the current limitation persists. The compensator will be released when the current limitation is removed.

Release compensator after current limit:

Enter the number of switching cycles that the compensator is to remain frozen after the removal of the current limitation. The minimum amount of cycles for the control feature to remain active is two, while in practise this would be longer due to filtering of a noisy measurement.

Enable input voltage feed forward compensation:

Check this box to enable input voltage feed-forward compensation to improve the converter response on changes of the input voltage.

Nominal input voltage:

Enter the nominal input voltage in volts.

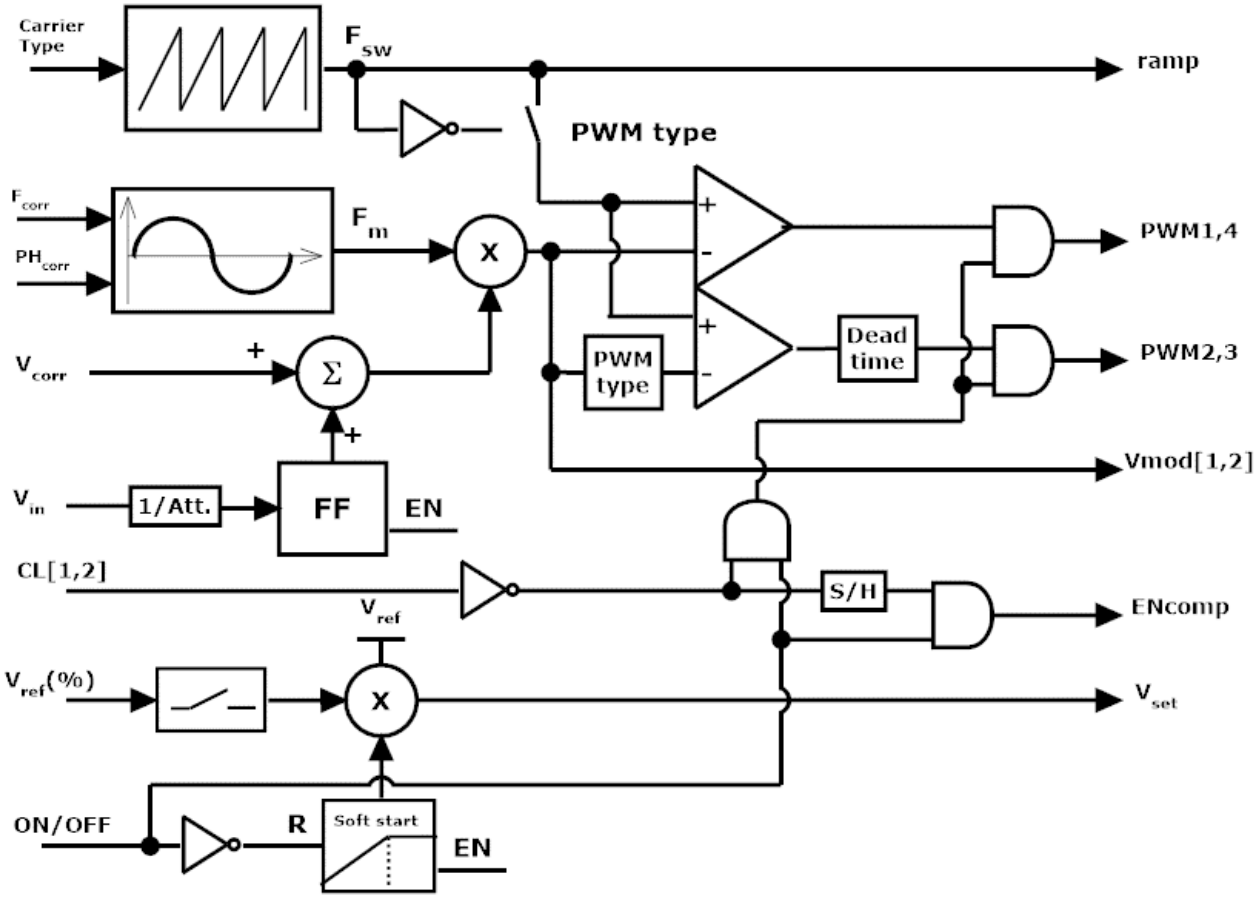
Input voltage measurement attenuation:

Enter the attenuation on the input DC voltage measurement seen at the Vin input pin of the controller.

Use Vref profile:

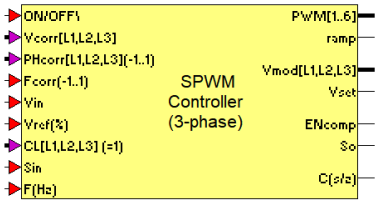
Check this box to enable the use of the input Vref% pin.

The following figure is a functional block diagram of the voltage-mode controller detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.



An example on the single-phase SPWM controller can be found at: Digital Power > Examples > Simulation > Controllers >VMC-SPWM 1-phase.vsm

Contents - Simulation



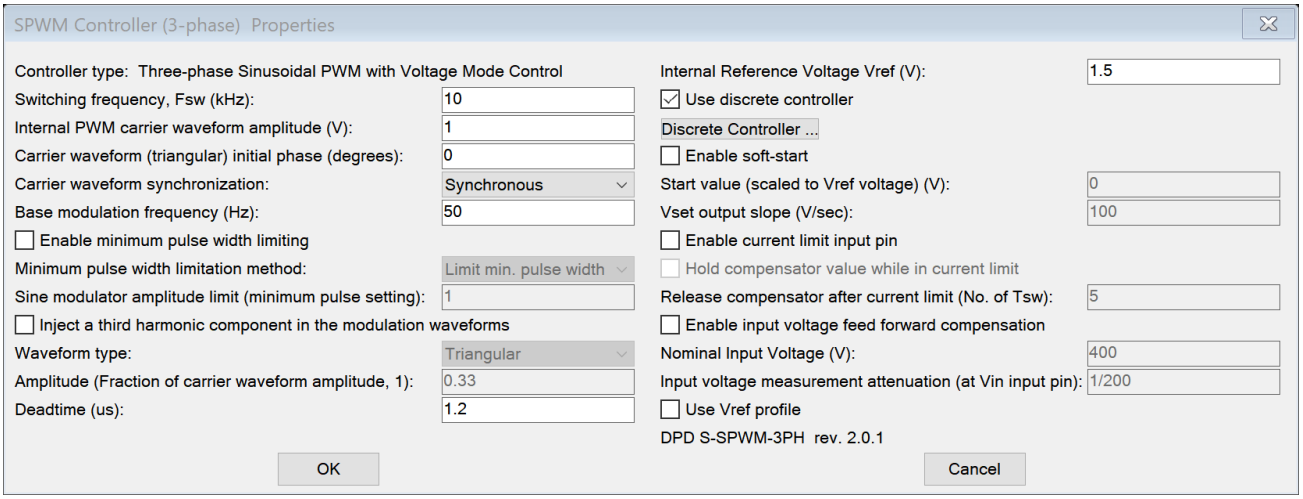
SPWM Voltage mode controller (3-phase)

This block is the 3-phase version of the sinusoidal PWM voltage-mode controller. The carrier waveform in this block is as a default triangular. The block can be used in analog or digital simulations.

Input Pins:	**ON/OFF**	Enable pin (ON ≥ 1, OFF < 1) of the voltage mode controller.
	Vcorr[L1,L2,L3]	Input pin usually from the output of a compensator. Each phase can be individually controlled.
	PHcorr[](-1..1)	Input pin to control the phase of the modulator waveforms (sinusoidal).
	Fcorr (-1..1)	Input pin to control the frequency of the modulator waveforms.
	Vin	Input voltage (DC) measurement pin. This measurement is used for feed-forward compensation in VMC.
	Vref%	The input to this pin (in percent) will vary the internally set Vref voltage (only active if "Use Vref profile" is checked.
	CL[L1,L2,L3]	Current limit trigger input vector. A value ≥ 1 activates the current limit, switching off the respective PWM outputs of the given phase leg to be reset on the next switching cycle – a cycle-by-cycle (CBC) current limit.
	Sin	Sampling input pin. If the controller is enabled in the block dialog as a discrete controller and "Sample the controller on the Sin pin" is selected, then the controller will wait for a rising edge at this pin to perform each sample. Usually connected in this case from the So output pin of the compensator.
	F (Hz)	Frequency input pin. If the value at the pin input is greater than zero, then the frequency analysis will be enabled. Requires a model-based frequency analyser block from the Tools section in the diagram.
Output pins:	**PWM[1..6]**	The pulse-width modulated (PWM) outputs which can be connected to a three-phase power inverter SW input.
	Ramp	The internal control ramp at the switching frequency.
	Vmod[L1,L2,L3]	The internal modulation which along with the ramp determines the duty cycle of the PWM outputs. There are three modulators, one for each phase.
	Vset	This is the set point voltage sent out to this pin. This voltage will normally be the internal Vref voltage however it will vary during soft start.
	ENcomp	This is an enable output which is typically connected to a compensator block. This pin can disable the compensator during current limit for example.
	So	When a discrete controller is selected, this is the output sample pulse after the internal controller delay (after the controller has calculated its new value).
	C(s/z)	When the frequency analysis is enabled (F(Hz) input > 0), this is a complex value proportional to the frequency response of the internal PWM and delays.

Dialog properties:

The three-phase SPWM voltage mode controller block properties menu is shown in the following box which appears when right-clicking on the block.



Switching frequency:

Enter the required switching frequency of the power converter to be controlled. This will set the ramp frequency and therefore the output PWM frequency.

The carrier waveform is triangular as default.

Carrier waveform initial phase:

The initial phase of the carrier waveform can be entered. This phase is then relative to the modulator waveform. Also, interleaving can be achieved with multiple controllers / inverter stages.

Carrier waveform frequency synchronisation:

The choices are:

1. Asynchronous
2. Synchronous

For an asynchronous carrier waveform the carrier frequency is not locked to the modulation frequency and asymmetries may be present in the resulting PWM waveform. If a synchronous carrier waveform is selected, the initial ratio of the carrier (switching) frequency to the modulator frequency is set to an integer and is maintained with variations of the modulator frequency. The switching frequency will therefore vary with time with respect to the modulator frequency.

Base modulation frequency:

Enter the frequency of the modulating waveform. This can be held constant or varied by connecting a control signal to the Fcorr input pin.

Enable minimum pulse-width limiting:

Check this box to enable minimum pulse-width limiting

Minimum pulse-width limitation method:

The choices are:

1. Limit minimum pulse-width
2. Use pulse skipping

Due to practical limitations, there is a minimum practical pulse-width of the PWM, where switching on a power switch for a period less than this minimum will not affect the output voltage but will however increase converter losses due to switches not completely turned. For the first selection, the pulse width is limited to a minimum value; in the second selection, the pulses are skipped if they are determined to be below the minimum limit.

Sine modulator amplitude limit:

Enter a value less than 1 to limit the minimum pulse-width of the output PWM.

Inject a third harmonic component into the modulation waveforms:

Check this box to add a third harmonic component in the modulator waveforms

Waveform type:

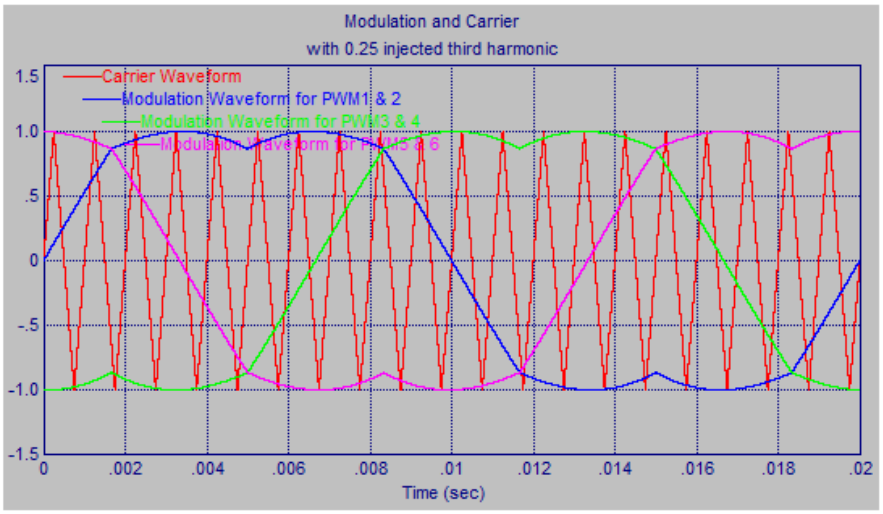
The choices are:

1. Sinusoidal
2. Triangular

Either a sinusoidal or a triangular waveform can be injected into the modulator sine wave. This injected waveform will have three times the modulator frequency (third harmonic). This type of waveform injection allows the emulation of carrier-based Space Vector PWM.

Amplitude (fraction of carrier waveform amplitude):

Enter an amplitude value of the injected waveform as a fraction of the carrier waveform amplitude which is 1. The diagram below shows the resultant three-phase modulators with an injected triangular wave at the third harmonic frequency. This modulation strategy will give maximum output voltage for a given input voltage.



Dead-time:

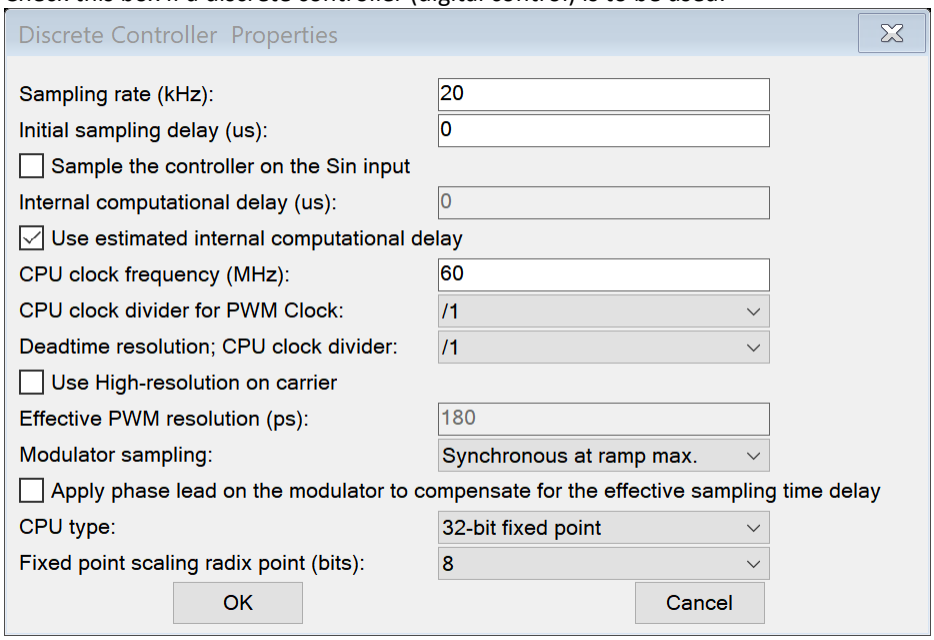
Enter the desired dead-time in microseconds.

Internal reference voltage:

Enter the reference voltage at which the scaled parameter (usually output voltage) will be regulated.

Use discrete controller:

Check this box if a discrete controller (digital control) is to be used.



Sampling rate:

Enter the sampling rate of the controller in kilohertz. This is often the same as the switching frequency but can be set at any other frequency.

Initial sampling delay:

Enter the initial sampling delay in microseconds. The controller will then be sampled at each sampling instant effectively delaying the sampling with respect to a previous action.

Sample the controller on the Sin input:

Select this option if the controller is to be sampled at specific instances. The controller will be sampled on the rising edge of this input, after the given delay time. The sampling instant input will be typically after a previous function has been performed such as a compensator calculation delay. The initial sampling delay above will be ignored in this case.

Internal computational delay:

Enter the delay for computation within the voltage mode controller. The time delays can be adjusted to simulate any computation and sampling delay within the digital controller. The sampling instant within the controller will occur after the given delay, also if sampled at the Sin input, so that by entering the delay, the actual sampling instant is effectively controlled.

Use estimated internal computational delay:

If this is selected, the internal computational delay value above will be ignored and an internal delay value used based upon the current selections of the controller and the given CPU clock frequency.

CPU clock frequency (MHz):

Enter the frequency at which the CPU is clocked in MHz. This is not the sampling frequency of the controller.

Clock divider for PWM clock:

The PWM clock can be reduced in frequency for low-frequency PWM generation.

Dead-time resolution; counter frequency (MHz):

Set the resolution of the dead-time period by entering the frequency of the dead-time counter in Mega-Hertz.

Use high resolution on carrier:

Select this if the default resolution of the PWM is not used and a higher resolution is required. The high-resolution will be implemented internally on the carrier waveforms.

Effective PWM resolution (ps):

Enter the effective resolution of the output PWM in picoseconds. This will be implemented into the ramp resolution.

Modulator sampling:

The choices are:

1. Asynchronous (at the given sampling frequency rate)
2. Synchronous at the minimum of the ramp (zero)
3. Synchronous at the maximum of the ramp (period)
4. Synchronous at the minimum and maximum ramp

This selection determines the moment at which the modulator is sampled with respect to the carrier waveform.

Apply phase lead on the modulator to compensate for the effective sampling delay:

Check this box to anticipate the modulator sine-wave to exactly the value to compensate for the sampling delay of the modulator.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

Enable soft start:

Check this box to enable a soft start which will be active when the controller is first switched on at the ON\OFF/ input or at the start of a simulation.

Start value (V):

Enter the soft start initial value of the output voltage scaled with respect to Vref or the measurement attenuation.

Vset output slope (V/s):

Enter the desired slope (rise time) of the soft start in Volt / second.

Enable current limit input pin:

Check this box to enable current limiting of the PWM output (determined by the input pin CL).

Hold compensator value while in current limit:

If this box is checked, the compensator is disabled with its internal values “frozen” while the current limitation persists. The compensator will be released when the current limitation is removed.

Release compensator after current limit:

Enter the number of switching cycles that the compensator is to remain frozen after the removal of the current limitation. The minimum amount of cycles for the control feature to remain active is two, while in practise this would be longer due to filtering of a noisy measurement.

Enable input voltage feed forward compensation:

Check this box to enable input voltage feed-forward compensation to improve the converter response on changes of the input voltage.

Nominal input voltage:

Enter the nominal DC input voltage in volts.

Input voltage measurement attenuation:

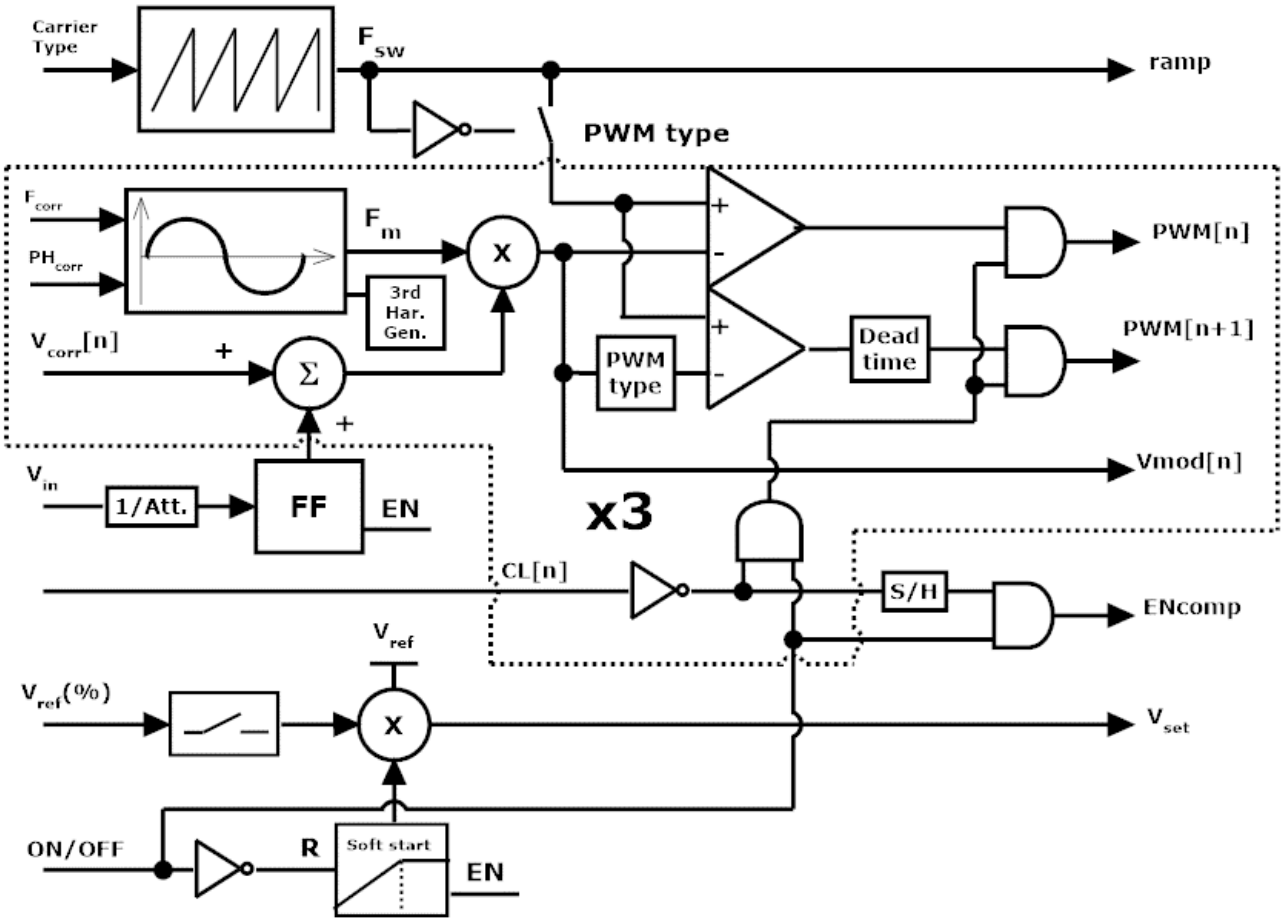
Enter the attenuation on the input voltage measurement seen at the Vin input pin of the controller.

Use Vref profile:

Check this box to enable the use of the input Vref% pin.

An example on the single-phase SPWM controller can be found at: Digital Power > Examples > Simulation > Controllers >VMC-SPWM 3-phase.vsm

The following figure is a functional block diagram of the three-phase sinusoidal voltage-mode controller detailing its function in a graphical format. The corresponding input and output pins are shown, their function and connections detailed.



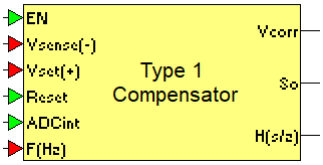
Contents - Simulation

Compensators

The aim of a compensator as used in power converter control loops (digital or analog) is to provide as much DC gain as possible in order to eliminate any steady state error in the control loop regulation, to provide the required poles and zeros to compensate for those present within the power converter and control technique, ensure sufficient closed-loop attenuation at the switching frequency and attenuate any line or input frequency. There are 7 different compensators available in the simulation section of the digital power designer, all with a pole at the origin to provide a high DC gain and each with a different number of poles and zeros.

The type 1, 2, 3 and 3p3z compensators can be applied by directly entering the required poles and zeros, while the PI and PID compensators can be applied using the familiar Proportional-Integral-Differential gains.

Conversion between the PID gains and the compensator poles and zeros can be performed using the compensator tools in the tools section of the digital power designer.



Type 1 compensator

The type 1 compensator is basically an I-compensator which only has an integral part. It is a first order compensator which only has one pole at the origin and no zero. It is rarely used in digital control because adding additional poles or zeros do not complicate things too much and the additional poles and zeros allow better performance. The type 1 compensator can be used successfully in cruder analog current mode control if the ESR zero is chosen appropriately (the output capacitor type).

This compensator has the transfer function:

$$H_1(s) = \frac{\omega_{p0}}{s}$$

Or expressed as a discrete compensator (when selected):

$$H_1(z) = \omega_{p0} \cdot T_s \cdot \left(\frac{z}{z-1} \right)$$

where $\omega p0$ is the pole at the origin and Ts is the compensator sampling time.

Input pins:

EN — Enables the compensator for execution. A value < 1 at this pin will hold the current values within the compensator until the EN pin returns to ≥ 1.

Vsense(-) — The voltage sensing input (negative input to the compensator) in Volts.

Vset(+) — The set point voltage (positive input) in Volts.

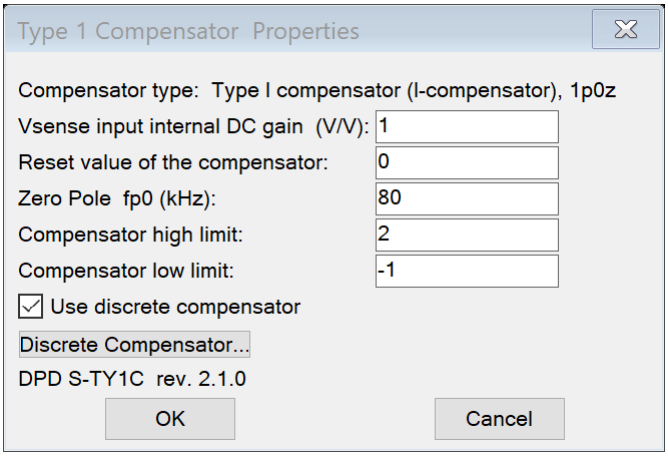
Reset — A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to zero.

ADCint — If enabled in the dialog, the digital compensator will be sampled at the rising edge of this pin. Usually connected from the ADC SOC output or from any prior computational delay block output.

	F(Hz)	If this pin is > 0, the frequency response will be enabled. Usually connected from the output of the model-based frequency response analysis block.
Output pins:	**Vcorr**	The output of the compensator.
	So	An output pulse at the instant after the internal computation of the controller has been executed at every sample (used in digital control).
	H(s/z)	The frequency response output in complex form either in the s-domain (analog compensator or in the z-domain (digital compensator).

Dialog properties:

The type 1 compensator block properties menu is shown in the following box which appears when right-clicking on the block.



Vsense input internal DC gain:

Enter the DC gain adjustment (if none = 1) before the error voltage is calculated and the voltage sensed is fed to the internal compensator input.

Internally:

$$Verr = Vset - Vsense*DCgain.$$

Reset value of the compensator:

Enter the value to which the compensator will initiate on a reset at the reset input pin.

Zero pole Fp0:

Enter the value of the compensator pole at the origin in kilohertz.

Compensator high limit:

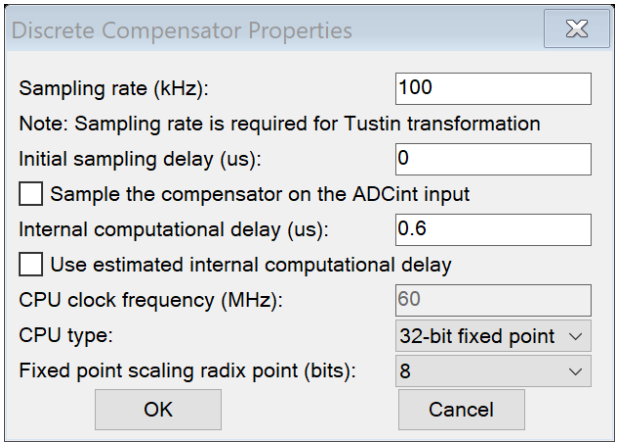
Enter the high level limit of the compensator.

Compensator low limit:

Enter the low-level limit of the compensator. NOTE that these limits are anti-windup limits.

Use discrete compensator:

Check this box if a discrete compensator is to be used in a simulation (digital control).



Sampling rate:

Enter the discrete compensator sampling rate in kHz.

NOTE: The sampling rate used to generate the z-coefficients using the Tustin transformation. If the poles and zeros are entered manually, the discrete compensator coefficients will be generated for the entered sample. For this reason, the sample rate is necessary even if the compensator is sampled at the ADCint input pin. If the sample rate at the ADCint input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (usually the sampling time of an ADC). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the ADCint input pin:

When enabled, the compensator will be sampled on the rising edge of the ADCint input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the internal compensator computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz in order to calculate the internal computational delay.

CPU type:

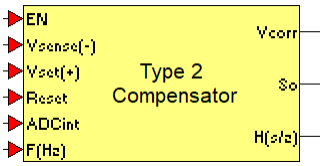
Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16-bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

Fixed point scaling radix point:

Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.
e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.



Type 2 compensator

The type 2 compensator is a second order compensator with two poles (one at the origin) and a zero. This compensator is typically used in peak current mode control.

This compensator has the transfer function:

$$H_2(s) = \frac{\omega_{p0}}{s} \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right)}{\left(\frac{s}{\omega_{p1}} + 1\right)}$$

Or expressed as a discrete compensator (when selected):

$$H_2(z) = K_z \cdot \frac{z^2 + B_1 \cdot z + B_0}{z^2 + A_1 \cdot z + A_0}$$

where the coefficients Kz, Bn and An are calculated internally in the compensator block using the bi-linear (Tustin) transform or can be imported from an external file.

Input pins:

EN — Enables the compensator for execution. A value < 1 at this pin will hold the current values within the compensator until the EN pin returns to ≥ 1.

Vsense(-) — The voltage sensing input (negative input to the compensator) in Volts.

Vset(+) — The set point voltage (positive input) in Volts.

Reset — A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to zero.

ADCint — If enabled in the dialog, the digital compensator will be sampled at the rising edge of this pin. Usually connected from the ADC SOC output or from any prior computational delay block output.

F(Hz) — If this pin is > 0, the frequency response will be enabled. Usually connected from the output of the model-based frequency response analysis block.

Output pins:

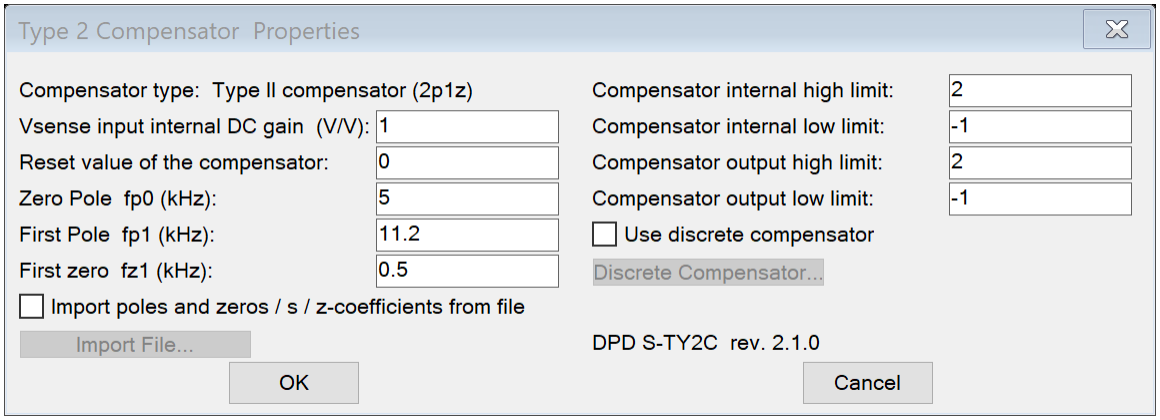
Vcorr — The output of the compensator.

So — An output pulse at the instant after the internal computation of the controller has been executed at every sample (used in digital control).

H(s/z) — The frequency response output in complex form either in the s-domain (analog compensator or in the z-domain (digital compensator).

Dialog properties:

The type 2 compensator block properties menu is shown in the following box which appears when right-clicking on the block.



Vsense input internal DC gain:

Enter the DC gain adjustment (if none = 1) before the error voltage is calculated and the voltage sensed is fed to the internal compensator input.

Internally:

$$Verr = Vset - Vsense*DCgain.$$

Reset value of the compensator:

Enter the value to which the compensator will initiate on a reset at the reset input pin.

Zero pole Fp0:

Enter the value of the compensator pole at the origin in kilohertz.

First pole Fp1:

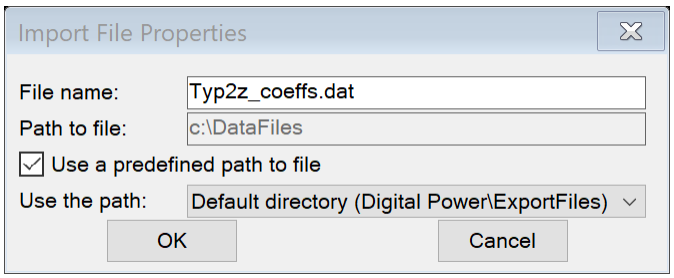
Enter the value of the first pole of the compensator in kilohertz.

First zero Fz1:

Enter the value of the first zero of the compensator in kilohertz.

Import poles and zeros / z-coefficients from file:

If selected, the following sub-dialog will become available:



Check this box if the compensator poles and zeros are to be read from a file. This file can be typically generated by the compensator tools within the Tools section of the digital power designer or by other methods.

Note that if a discrete compensator is NOT selected then the compensator block will look for a poles and zeros format or s-coefficients within the file. If a discrete compensator is selected then the compensator block will look for a discrete coefficient format (z-coefficients) within the file.

If an incorrect file is selected, the compensator block will signal an error at the start of a simulation run and the block will turn red.

Compensator internal high limit:

Enter the high level internal limit of the compensator which is applied internally on the integrator of the compensator.

Compensator internal low limit:

Enter the low-level internal limit of the compensator.
NOTE that these limits are anti-windup limits.

Compensator external high limit:

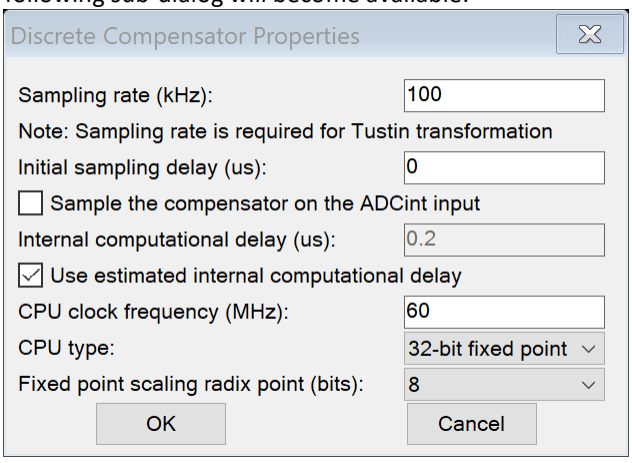
Enter the high level external limit of the compensator which is applied at the compensator output.

Compensator external low limit:

Enter the low-level external limit of the compensator which is applied at the compensator output.

Use discrete compensator:

Check this box if a discrete compensator is to be used in a simulation (digital control). The following sub-dialog will become available:



Sampling rate:

Enter the discrete compensator sampling rate in kHz.

NOTE: If an external file is used for the discrete coefficients, the sampling rate used to generate those coefficients must be equal to the value entered here. If the poles and zeros are entered manually, the discrete compensator coefficients will be generated for the entered sample rate using the Tustin transformation. For this reason, the sample rate is necessary even if the compensator is sampled at the ADCint input pin. If the sample rate at the ADCint input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (usually the sampling time of an ADC). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the ADCint input pin:

When enabled, the compensator will be sampled on the rising edge of the ADCint input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the internal compensator computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz in order to calculate the internal computational delay.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16.bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

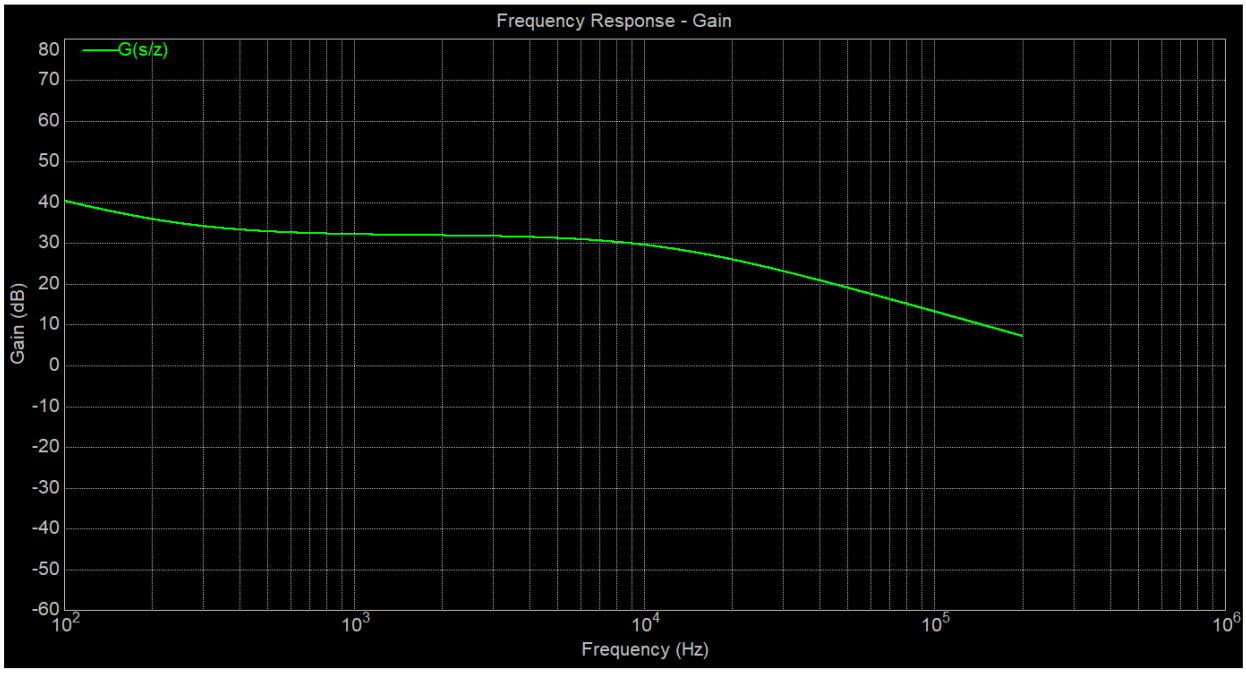
Fixed point scaling radix point:

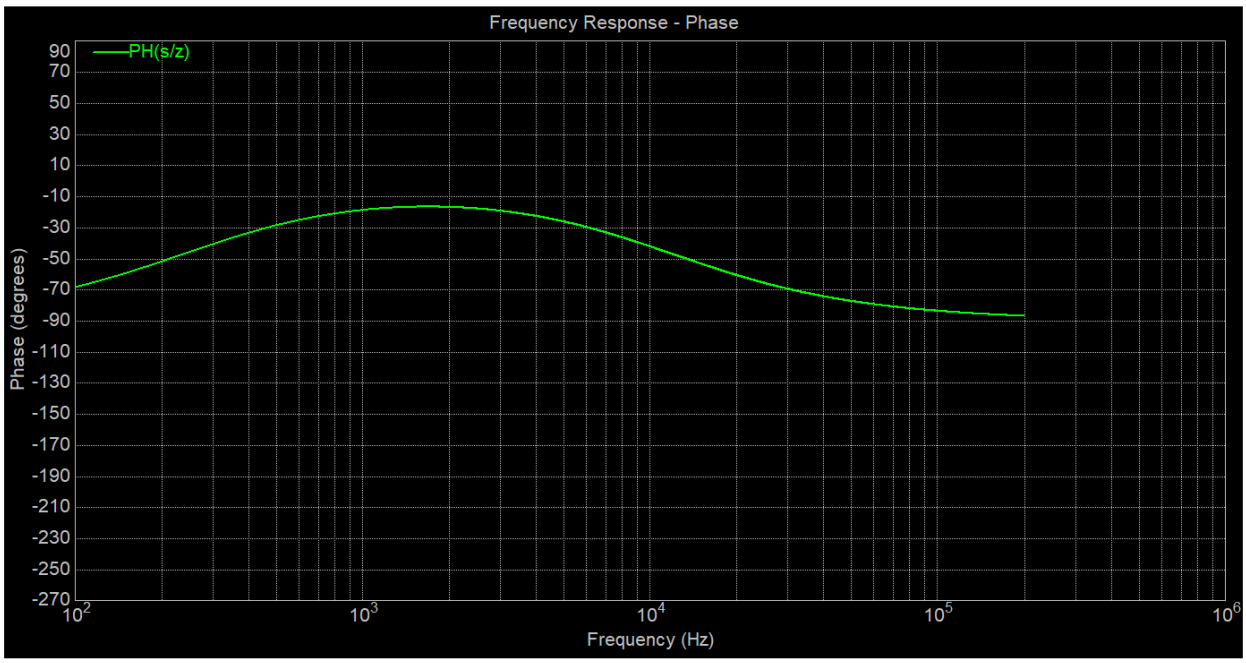
Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

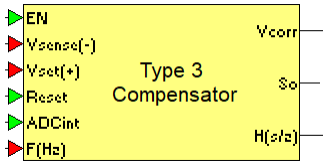
Frequency Response of the compensator can be viewed internally in the type 2 compensator block:

Type 2 Compensator





Contents - Simulation



Type 3 compensator

The type 3 compensator is a third order compensator with three poles (one at the origin) and two zeros. This compensator is typically used in voltage mode control.

This compensator has the transfer function:

$$H_3(s) = \frac{\omega_{p0}}{s} \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right) \cdot \left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_{p1}} + 1\right) \cdot \left(\frac{s}{\omega_{p2}} + 1\right)}$$

Or expressed as a discrete compensator (when selected):

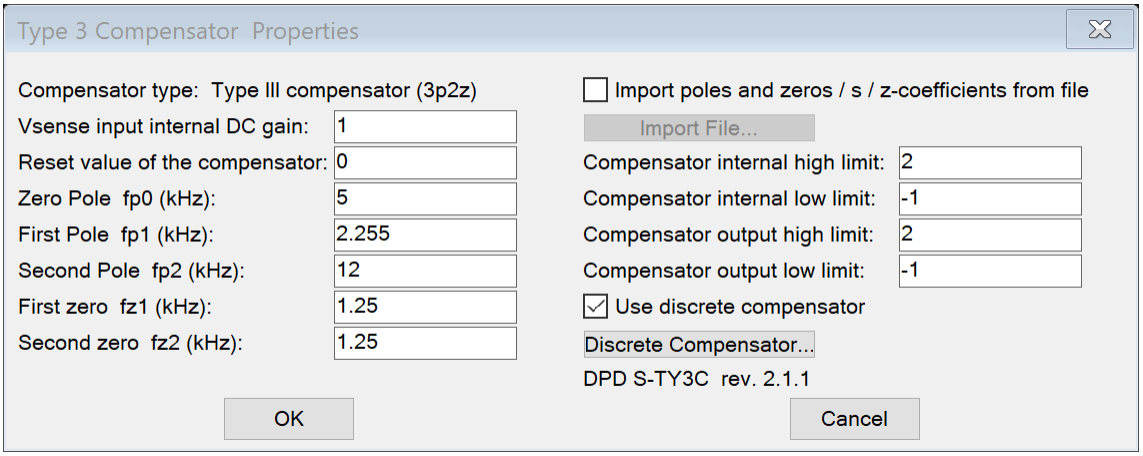
$$H_3(z) = K_z \cdot \frac{z^3 + B_2 \cdot z^2 + B_1 \cdot z + B_0}{z^3 + A_2 \cdot z^2 + A_1 \cdot z + A_0}$$

where the coefficients Kz, Bn and An are calculated internally in the compensator block using the bi-linear (Tustin) transform or can be imported from an external file.

Input pins:	**EN**	Enables the compensator for execution. A value < 1 at this pin will hold the current values within the compensator until the EN pin returns to ≥ 1.
	Vsense(-)	The voltage sensing input (negative input to the compensator) in Volts.
	Vset(+)	The set point voltage (positive input) in Volts.
	Reset	A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to zero.
	ADCint	If enabled in the dialog, the digital compensator will be sampled at the rising edge of this pin. Usually connected from the ADC SOC output or from any prior computational delay block output.
	F(Hz)	If this pin is > 0, the frequency response will be enabled. Usually connected from the output of the model-based frequency response analysis block.
Output pins:	**Vcorr**	The output of the compensator.
	So	An output pulse at the instant after the internal computation of the controller has been executed at every sample (used in digital control).
	H(s/z)	The frequency response output in complex form either in the s-domain (analog compensator or in the z-domain (digital compensator).

Dialog properties:

The type 3 compensator block properties menu is shown in the following box which appears when right-clicking on the block.



Vsense input internal DC gain:

Enter the DC gain adjustment (if none = 1) before the error voltage is calculated and the voltage sensed is fed to the internal compensator input.

Internally:

$$Verr = Vset - Vsense*DCgain.$$

Reset value of the compensator:

Enter the value to which the compensator will initiate on a reset at the reset input pin.

Zero pole Fp0:

Enter the value of the compensator pole at the origin in kilohertz.

First pole Fp1:

Enter the value of the first pole of the compensator in kilohertz.

Second pole Fp2:

Enter the value of the second pole of the compensator in kilohertz

First zero Fz1:

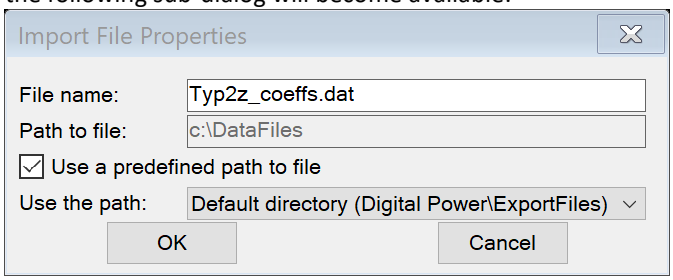
Enter the value of the first zero of the compensator in kilohertz.

Second zero Fz2:

Enter the value of the second zero of the compensator in kilohertz.

Import poles and zeros / s /z-coefficients from file:

If selected, the following sub-dialog will become available:



Check this box if the compensator poles and zeros are to be read from a file. This file can be typically generated by the compensator tools within the Tools section of the digital power designer or by other methods.

Note that if a discrete compensator is NOT selected then the compensator block will look for a poles and zeros format or s-coefficients within the file. If a discrete

compensator is selected then the compensator block will look for a discrete coefficient format (z-coefficients) within the file.

If an incorrect file is selected, the compensator block will signal an error at the start of a simulation run and the block will turn red.

Compensator internal high limit:

Enter the high level internal limit of the compensator which is applied internally on the integrator of the compensator.

Compensator internal low limit:

Enter the low-level internal limit of the compensator.
NOTE that these limits are anti-windup limits.

Compensator external high limit:

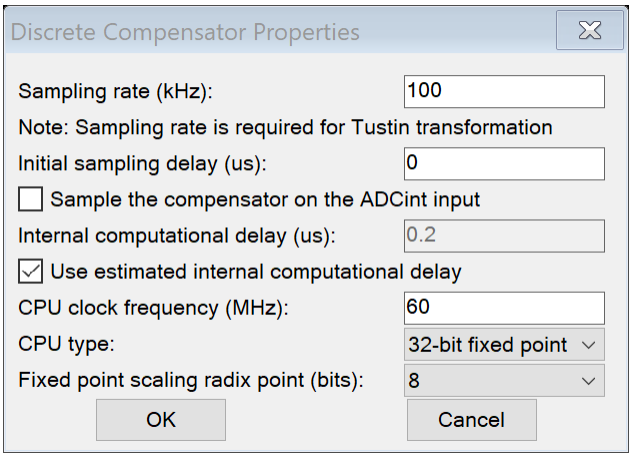
Enter the high level external limit of the compensator which is applied at the compensator output.

Compensator external low limit:

Enter the low-level external limit of the compensator which is applied at the compensator output.

Use discrete compensator:

Check this box if a discrete compensator is to be used in a simulation (digital control).



Sampling rate:

Enter the discrete compensator sampling rate in kHz.

NOTE: If an external file is used for the discrete coefficients, the sampling rate used to generate those coefficients must be equal to the value entered here. If the poles and zeros are entered manually, the discrete compensator coefficients will be generated for the entered sample rate using the Tustin transformation. For this reason, the sample rate is necessary even if the compensator is sampled at the ADCint input pin. If the sample rate at the ADCint input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (usually the sampling time of an ADC). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the ADCint input pin:

When enabled, the compensator will be sampled on the rising edge of the ADCint input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the internal compensator computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz in order to calculate the internal computational delay.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16.bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

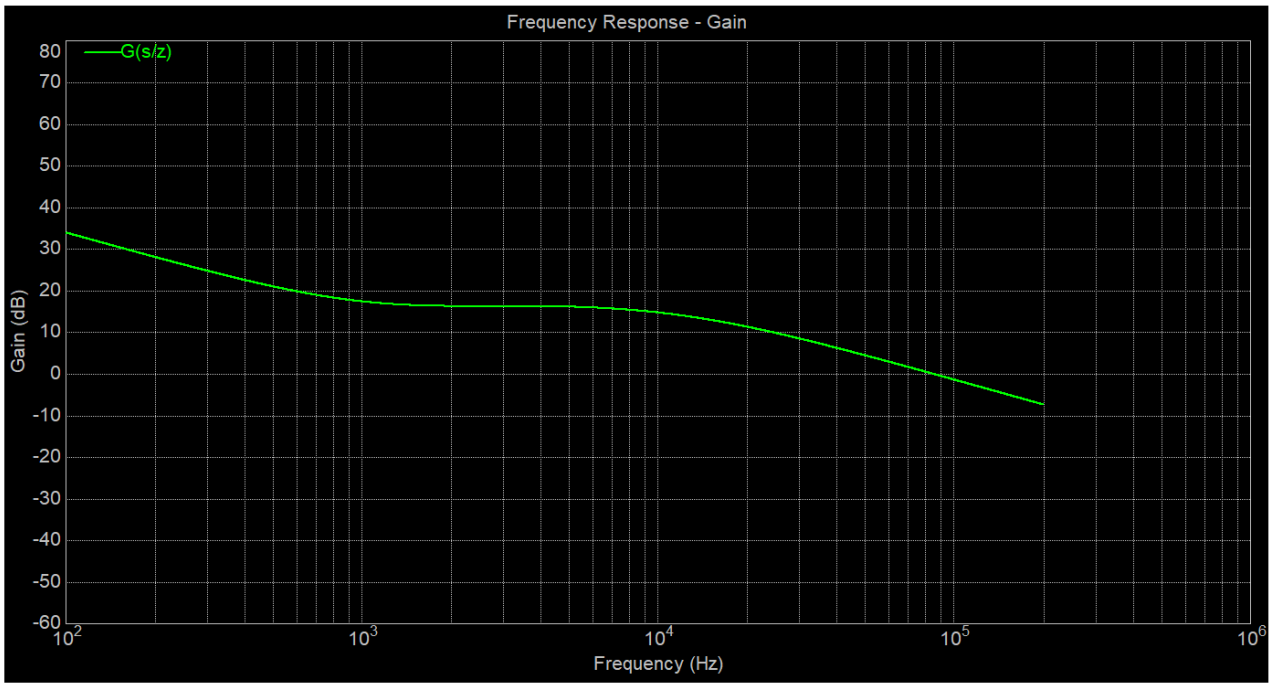
Fixed point scaling radix point:

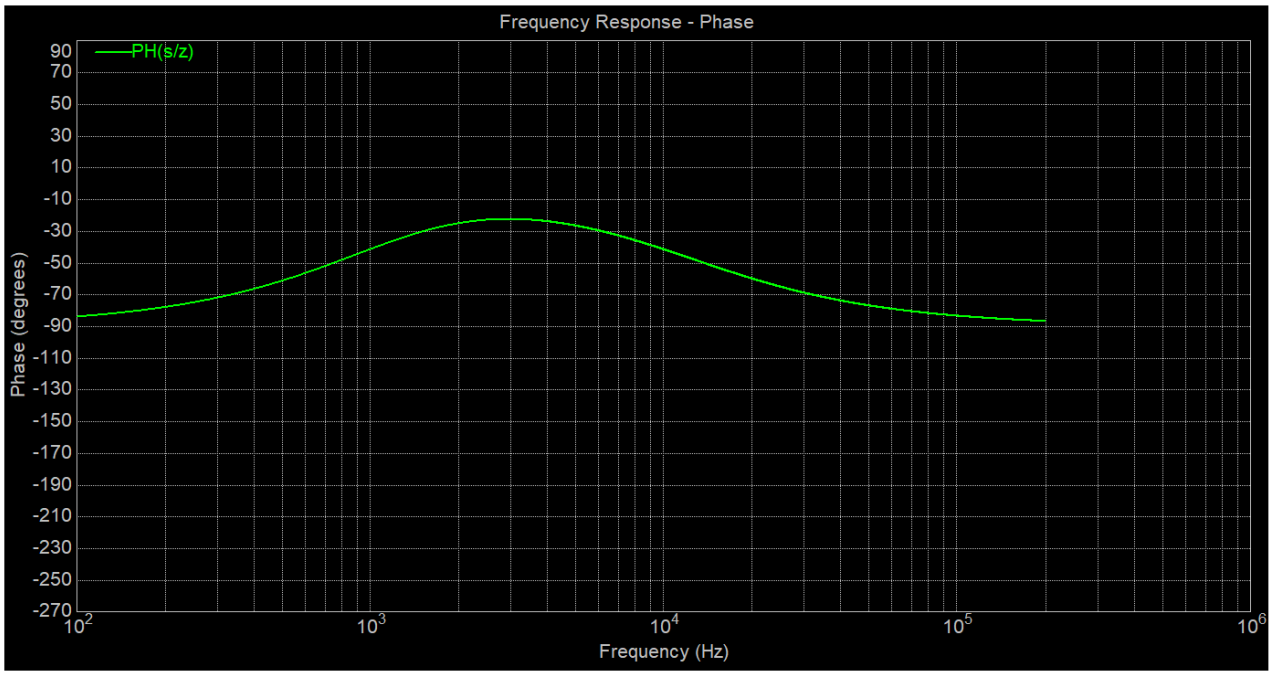
Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

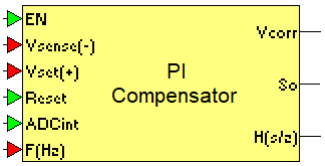
Frequency Response of the compensator can be viewed internally in the type 3 compensator block:

Type 3 Compensator





Contents - Simulation



PI compensator

The PI compensator is a proportional + integral gain compensator. It is a first order compensator with one pole at the origin and one zero. This block enables the setting of the coefficients using the familiar proportional and integral gains rather than the poles and zeros. This type of compensator is popular in certain applications (current mode control or auxiliary loops such as paralleling) due to its simplicity (only two parameters need to be set).

This compensator has the transfer function:

$$H_{pi}(s) = Kp + \frac{Ki}{s}$$

Or expressed as a discrete compensator (when selected):

$$H_{pi}(z) = K_p + K_i \cdot T_s \cdot \left(\frac{z}{z-1} \right)$$

where the coefficients Kp and Ki are the proportional and integral gain coefficients and Ts is the compensator sampling time.

Input pins:

EN — Enables the compensator for execution. A value < 1 at this pin will hold the current values within the compensator until the EN pin returns to ≥ 1.

Vsense(-) — The voltage sensing input (negative input to the compensator) in Volts.

Vset(+) — The set point voltage (positive input) in Volts.

Reset — A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to zero.

ADCint — If enabled in the dialog, the digital compensator will be sampled at the rising edge of this pin. Usually connected from the ADC SOC output or from any prior computational delay block output.

F(Hz) — If this pin is > 0, the frequency response will be enabled. Usually connected from the output of the model-based frequency response analysis block.

Output pins:

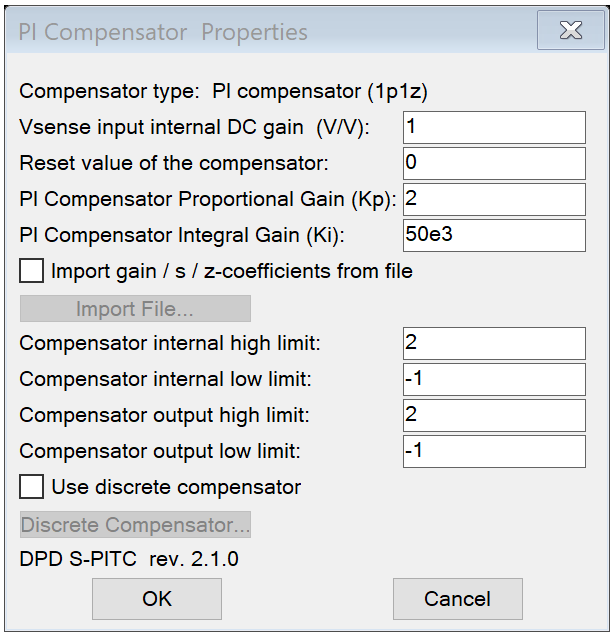
Vcorr — The output of the compensator.

So — An output pulse at the instant after the internal computation of the controller has been executed at every sample (used in digital control).

H(s/z) — The frequency response output in complex form either in the s-domain (analog compensator or in the z-domain (digital compensator).

Dialog properties:

The PI compensator block properties menu is shown in the following box which appears when right-clicking on the block.



Vsense input internal DC gain:

Enter the DC gain adjustment (if none = 1) before the error voltage is calculated and the voltage sensed is fed to the internal compensator input.

Internally:

$$Verr = Vset - Vsense*DCgain.$$

Reset value of the compensator:

Enter the value to which the compensator will initiate on a reset at the reset input pin.

PI compensator proportional gain:

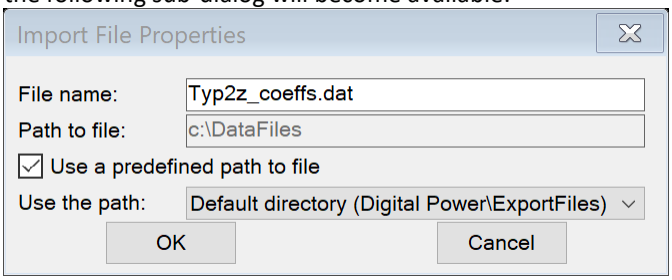
Enter the proportional gain of the compensator.

PI compensator integral gain:

Enter the integral gain of the compensator.

Import poles and zeros / s /z-coefficients from file:

If selected, the following sub-dialog will become available:



Check this box if the compensator poles and zeros are to be read from a file. This file can be typically generated by the compensator tools within the Tools section of the digital power designer or by other methods.

Note that if a discrete compensator is NOT selected then the compensator block will look for a poles and zeros format or s-coefficients within the file. If a discrete compensator is selected then the compensator block will look for a discrete coefficient format (z-coefficients) within the file.

If an incorrect file is selected, the compensator block will signal an error at the start of a simulation run and the block will turn red.

Compensator internal high limit:

Enter the high level internal limit of the compensator which is applied internally on the integrator of the compensator.

Compensator internal low limit:

Enter the low-level internal limit of the compensator.
NOTE that these limits are anti-windup limits.

Compensator external high limit:

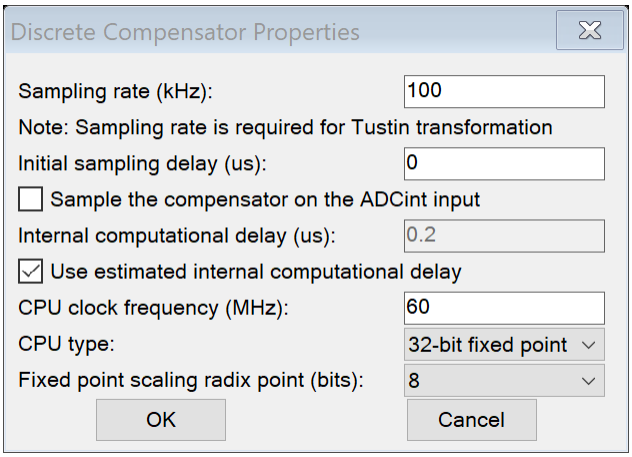
Enter the high level external limit of the compensator which is applied at the compensator output.

Compensator external low limit:

Enter the low-level external limit of the compensator which is applied at the compensator output.

Use discrete compensator:

Check this box if a discrete compensator is to be used in a simulation (digital control).



Sampling rate:

Enter the discrete compensator sampling rate in kHz.

NOTE: If an external file is used for the discrete coefficients, the sampling rate used to generate those coefficients must be equal to the value entered here. If the poles and zeros are entered manually, the discrete compensator coefficients will be generated for the entered sample rate using the Tustin transformation. For this reason, the sample rate is necessary even if the compensator is sampled at the ADCint input pin. If the sample rate at the ADCint input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (usually the sampling time of an ADC). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the ADCint input pin:

When enabled, the compensator will be sampled on the rising edge of the ADCint input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the internal compensator computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz in order to calculate the internal computational delay.

CPU type:

Enter the CPU type. The choices are:

4. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
5. 16.bit fixed-point e.g TI TMS320F240x, MSP430
6. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

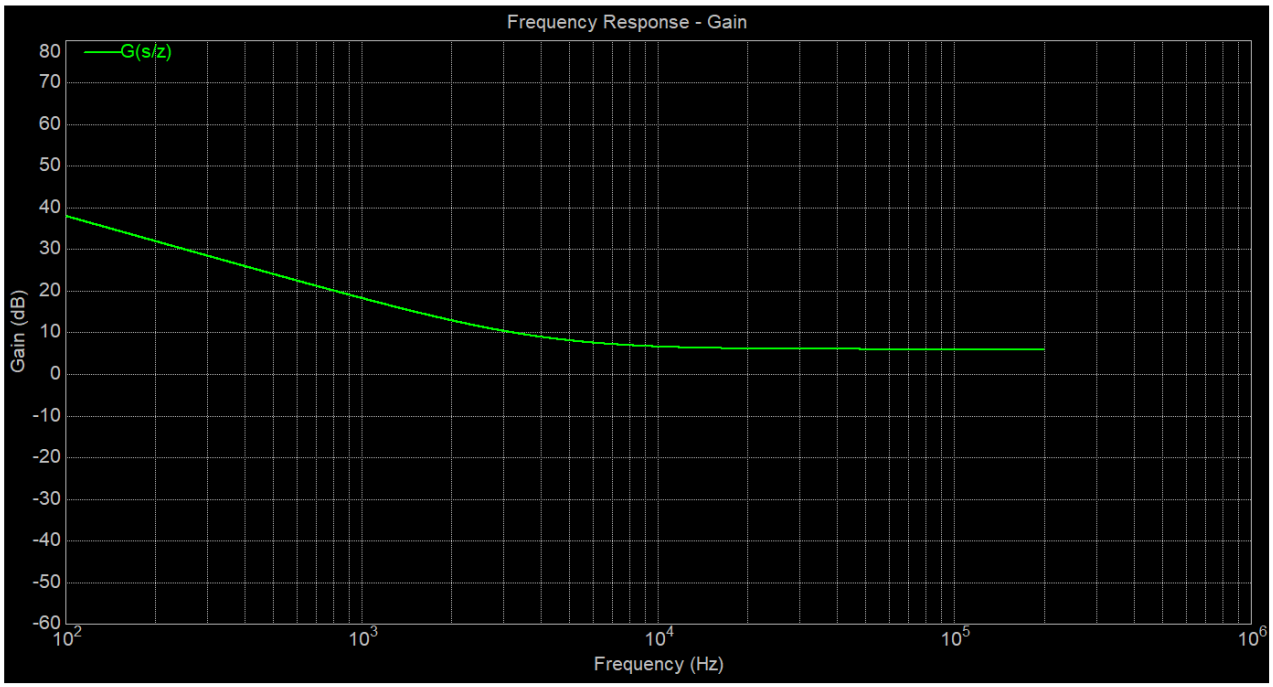
Fixed point scaling radix point:

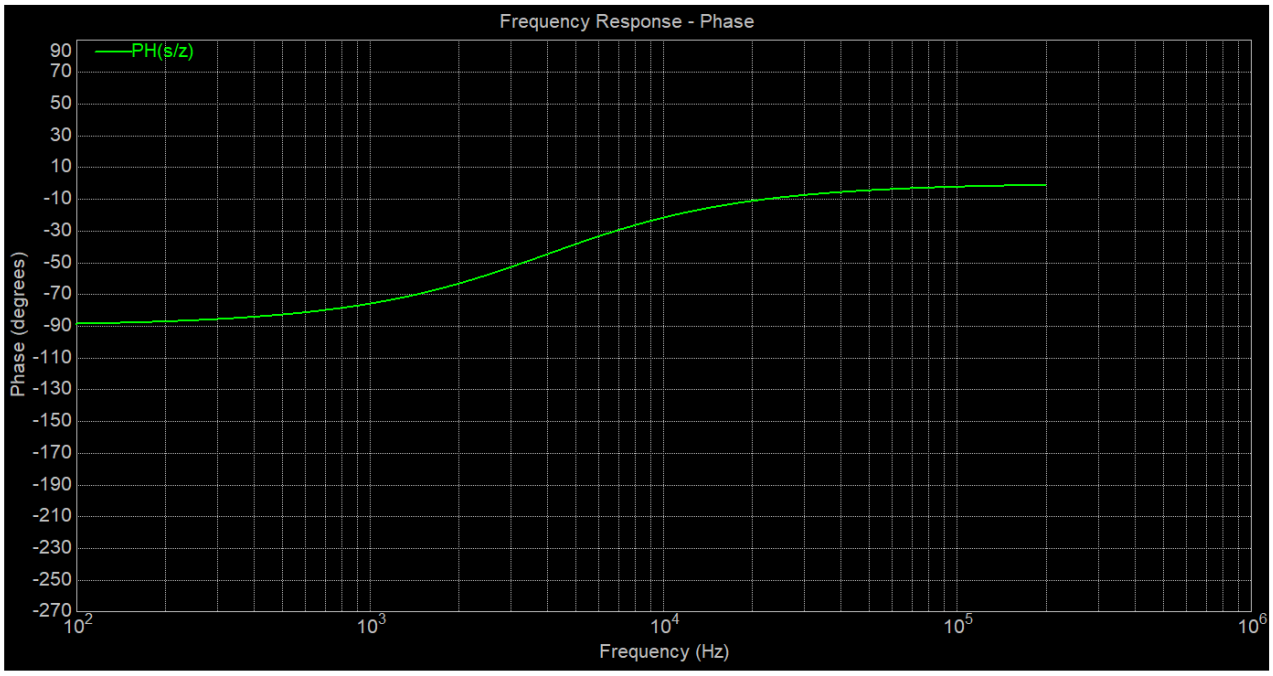
Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

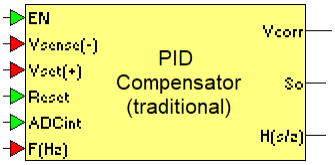
The Frequency Response of the compensator can be viewed internally in the PI compensator block:

PI Compensator





Contents - Simulation



PID compensator (traditional)

This compensator is a second order compensator allowing the setting of the proportional, integral and differential gains. The differential part of the transfer function is approximated to the difference of the input over the last two samples, multiplied by the differential gain. This compensator has two zeros and one pole at the origin and as such cannot be realized in a practical transfer function. This type of compensator is rarely used in digital power due to the sensitivity of the differential part to noise and it is normally replaced by the 2p2z PID compensator.

This compensator has the transfer function:

$$H_{pid}(s) = Kp + \frac{Ki}{s} + Kd \cdot s$$

Or expressed as a discrete compensator (when selected):

$$H_{pid}(z) = K_p + K_i \cdot T_s \cdot \left(\frac{z}{z-1}\right) + \frac{K_d}{T_s} \cdot \left(\frac{z-1}{z}\right)$$

where the coefficients Kp, Ki and Kd are the proportional, integral and differential gain coefficients and Ts is the compensator sampling time.

Input pins:

EN — Enables the compensator for execution. A value < 1 at this pin will hold the current values within the compensator until the EN pin returns to ≥ 1.

Vsense(-) — The voltage sensing input (negative input to the compensator) in Volts.

Vset(+) — The set point voltage (positive input) in Volts.

Reset — A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to zero.

ADCint — If enabled in the dialog, the digital compensator will be sampled at the rising edge of this pin. Usually connected from the ADC SOC output or from any prior computational delay block output.

F(Hz) — If this pin is > 0, the frequency response will be enabled. Usually connected from the output of the model-based frequency response analysis block.

Output pins:

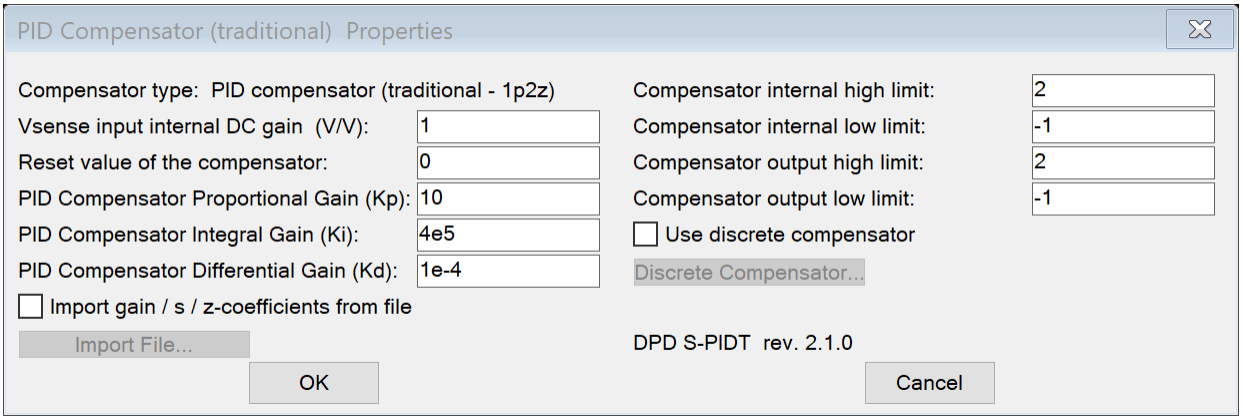
Vcorr — The output of the compensator.

So — An output pulse at the instant after the internal computation of the controller has been executed at every sample (used in digital control).

H(s/z) — The frequency response output in complex form either in the s-domain (analog compensator or in the z-domain (digital compensator).

Dialog properties:

The PID compensator properties menu is shown in the following box which appears when right-clicking on the block.



Vsense input internal DC gain:

Enter the DC gain adjustment (if none = 1) before the error voltage is calculated and the voltage sensed is fed to the internal compensator input.

Internally:

$$Verr = Vset - Vsense*DCgain.$$

Reset value of the compensator:

Enter the value to which the compensator will initiate on a reset at the reset input pin.

PID compensator proportional gain:

Enter the proportional gain of the compensator.

PID compensator integral gain:

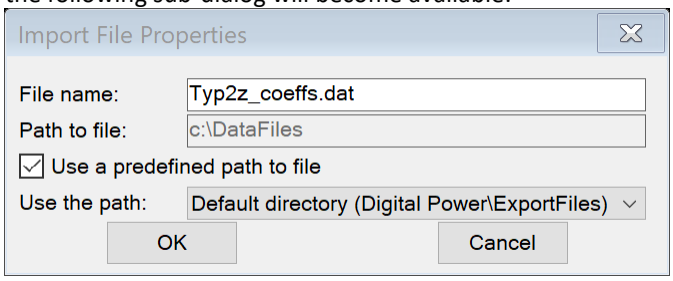
Enter the integral gain of the compensator.

PID compensator differential gain:

Enter the differential gain of the compensator.

Import poles and zeros / s /z-coefficients from file:

If selected, the following sub-dialog will become available:



Check this box if the compensator poles and zeros are to be read from a file. This file can be typically generated by the compensator tools within the Tools section of the digital power designer or by other methods.

Note that if a discrete compensator is NOT selected then the compensator block will look for a poles and zeros format or s-coefficients within the file. If a discrete compensator is selected then the compensator block will look for a discrete coefficient format (z-coefficients) within the file.

If an incorrect file is selected, the compensator block will signal an error at the start of a simulation run and the block will turn red.

Compensator internal high limit:

Enter the high level internal limit of the compensator which is applied internally on the integrator of the compensator.

Compensator internal low limit:

Enter the low-level internal limit of the compensator.
NOTE that these limits are anti-windup limits.

Compensator external high limit:

Enter the high level external limit of the compensator which is applied at the compensator output.

Compensator external low limit:

Enter the low-level external limit of the compensator which is applied at the compensator output.

Use discrete compensator:

Check this box if a discrete compensator is to be used in a simulation (digital control).

Sampling rate:

Enter the discrete compensator sampling rate in kHz.

NOTE: If an external file is used for the discrete coefficients, the sampling rate used to generate those coefficients must be equal to the value entered here. If the poles and zeros are entered manually, the discrete compensator coefficients will be generated for the entered sample rate using the Tustin transformation. For this reason, the sample rate is necessary even if the compensator is sampled at the ADCint input pin. If the sample rate at the ADCint input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (usually the sampling time of an ADC). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the ADCint input pin:

When enabled, the compensator will be sampled on the rising edge of the ADCint input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the internal compensator computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz in order to calculate the internal computational delay.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16.bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

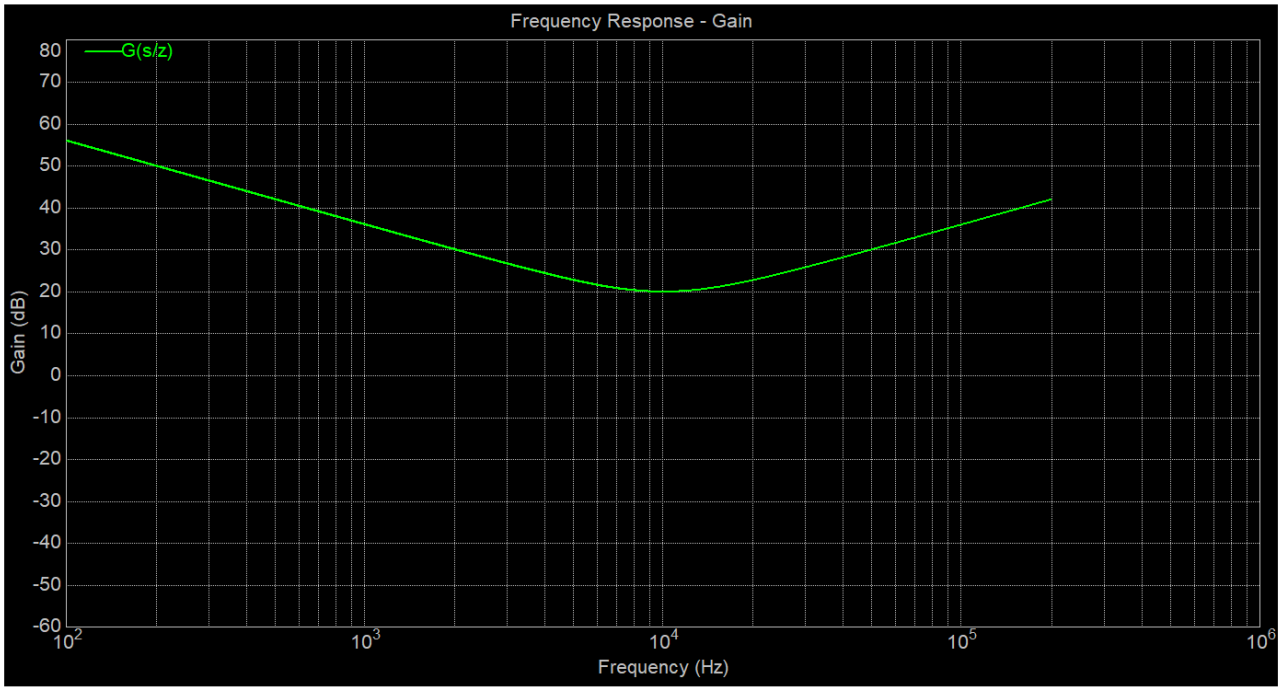
Fixed point scaling radix point:

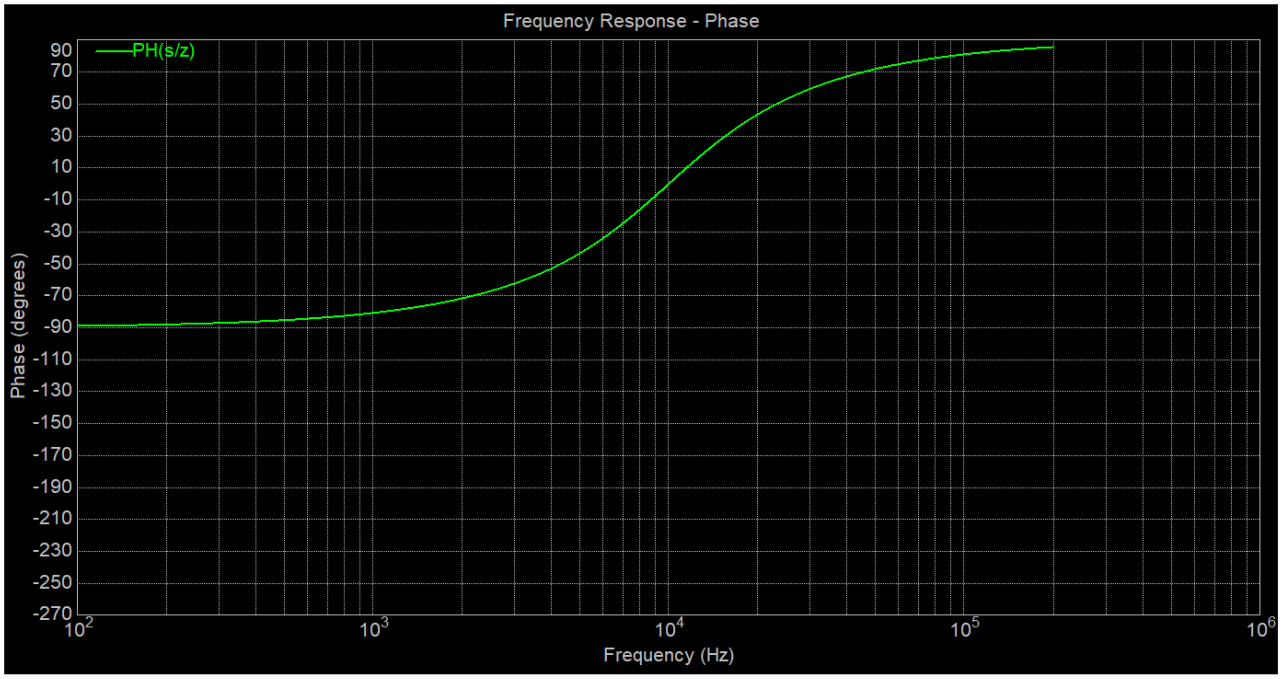
Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

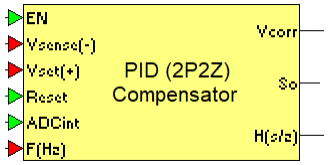
e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

The Frequency Response of the compensator can be viewed internally in the PID compensator block:

PID Compensator







PID compensator (2p2z)

This compensator is a PID compensator where the proportional, integral and differential gain terms can be set along with a fourth parameter which applies a low-pass filter on the differential term. The differential term low-pass filter coefficient is set relative to the differential gain using the value N. The compensator is a second order compensator with two poles (one at the origin) and two zeros. This type of compensator is popular in digital control.

This compensator has the transfer function:

$$H_{pid2}(s) = Kp + \frac{Ki}{s} + \frac{Kd \cdot s}{\left(\frac{Kd}{N} \cdot s + 1\right)}$$

Or expressed as a discrete compensator (when selected):

$$H_{pid}(z) = K_z \cdot \frac{z^2 + B_1 \cdot z + B_0}{z^2 + A_1 \cdot z + A_0}$$

where the coefficients Kz, Bn and An are calculated internally in the compensator block using the bi-linear (Tustin) transform or can be imported from an external file.

Input pins:

EN — Enables the compensator for execution. A value < 1 at this pin will hold the current values within the compensator until the EN pin returns to ≥ 1.

Vsense(-) — The voltage sensing input (negative input to the compensator) in Volts.

Vset(+) — The set point voltage (positive input) in Volts.

Reset — A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to zero.

ADCint — If enabled in the dialog, the digital compensator will be sampled at the rising edge of this pin. Usually connected from the ADC SOC output or from any prior computational delay block output.

F(Hz) — If this pin is > 0, the frequency response will be enabled. Usually connected from the output of the model-based frequency response analysis block.

Output pins:

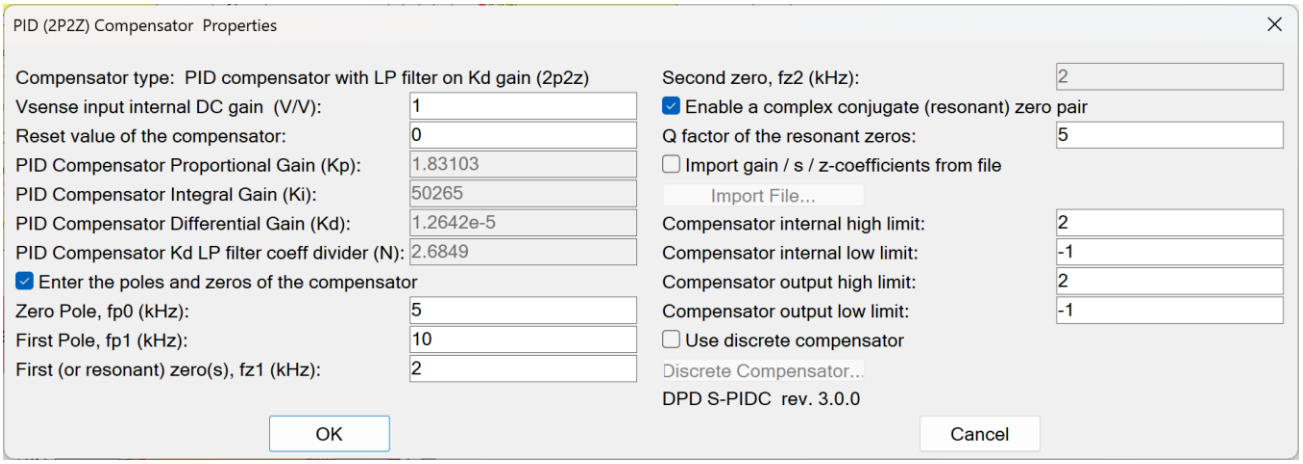
Vcorr — The output of the compensator.

So — An output pulse at the instant after the internal computation of the controller has been executed at every sample (used in digital control).

H(s/z) — The frequency response output in complex form either in the s-domain (analog compensator or in the z-domain (digital compensator).

Dialog properties:

The PID (2p2z) compensator properties menu is shown in the following box which appears when right-clicking on the block.



Vsense input internal DC gain:

Enter the DC gain adjustment (if none = 1) before the error voltage is calculated and the voltage sensed is fed to the internal compensator input.

Internally:

$$Verr = Vset - Vsense*DCgain.$$

Reset value of the compensator:

Enter the value to which the compensator will initiate on a reset at the reset input pin.

PID compensator proportional gain, Kp:

Enter the proportional gain of the compensator, Kp.

PID compensator integral gain, Ki:

Enter the integral gain of the compensator, Ki.

PID compensator differential gain, Kd:

Enter the differential gain of the compensator., Kd.

PID compensator Kd LP filter coeff divider, N:

Enter a value for the low-pass filter differential gain divider, N.

Enter the poles and zeros of the compensator:

Select this box if it is preferred to enter the poles and zeros of the compensator rather than the PID gain coefficients.

Zero pole Fp0:

Enter the value of the compensator pole at the origin in kilohertz.

First pole Fp1:

Enter the value of the first pole of the compensator in kilohertz.

First zero Fz1:

Enter the value of the first zero of the compensator in kilohertz.

Second zero Fz2:

Enter the value of the second zero of the compensator in kilohertz.

Enable a complex conjugate (resonant) zero pair:

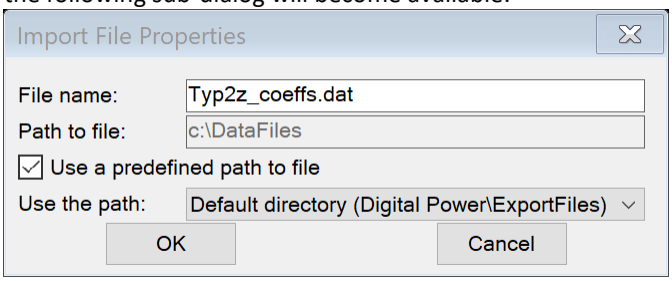
Enable this if the double zero is to be set as a complex conjugate pair (resonant zeros).

Q factor of the resonant zeros:

Enter the resonant Q value of the complex pole pair

Import poles and zeros / s /z-coefficients from file:

If selected, the following sub-dialog will become available:



Check this box if the compensator poles and zeros are to be read from a file. This file can be typically generated by the compensator tools within the Tools section of the digital power designer or by other methods.

Note that if a discrete compensator is NOT selected then the compensator block will look for a poles and zeros format or s-coefficients within the file. If a discrete compensator is selected then the compensator block will look for a discrete coefficient format (z-coefficients) within the file.

If an incorrect file is selected, the compensator block will signal an error at the start of a simulation run and the block will turn red.

Compensator internal high limit:

Enter the high level internal limit of the compensator which is applied internally on the integrator of the compensator.

Compensator internal low limit:

Enter the low-level internal limit of the compensator.
NOTE that these limits are anti-windup limits.

Compensator external high limit:

Enter the high level external limit of the compensator which is applied at the compensator output.

Compensator external low limit:

Enter the low-level external limit of the compensator which is applied at the compensator output.

Use discrete compensator:

Check this box if a discrete compensator is to be used in a simulation (digital control).

Sampling rate:

Enter the discrete compensator sampling rate in kHz.

NOTE: If an external file is used for the discrete coefficients, the sampling rate used to generate those coefficients must be equal to the value entered here. If the poles and zeros are entered manually, the discrete compensator coefficients will be generated for the entered sample rate using the Tustin transformation. For this reason, the sample rate is necessary even if the compensator is sampled at the ADCint input pin. If the sample rate at the ADCint input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (usually the sampling time of an ADC). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the ADCint input pin:

When enabled, the compensator will be sampled on the rising edge of the ADCint input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the internal compensator computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz in order to calculate the internal computational delay.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16.bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

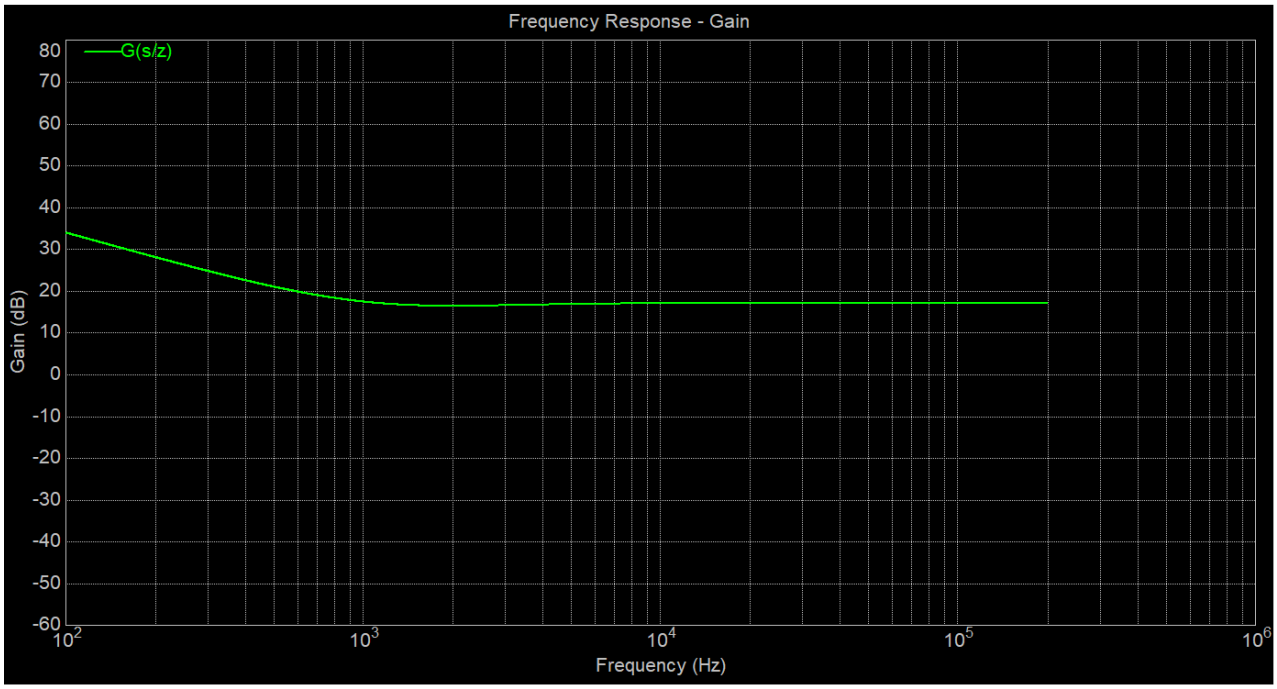
Fixed point scaling radix point:

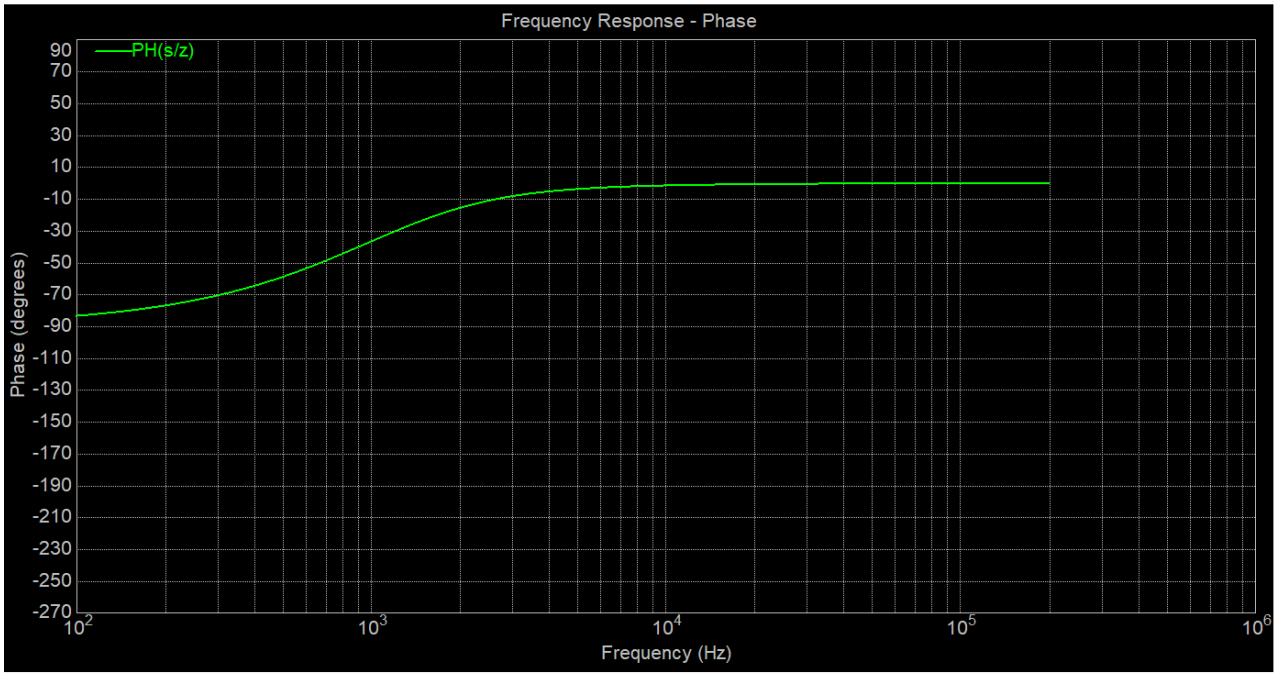
Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

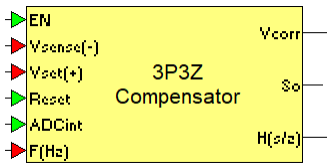
The Frequency Response of the compensator can be viewed internally in the 2p2z (PID) compensator block:

2p2z Compensator





Contents - Simulation



3p3z compensator

The 3p3z compensator is a third order compensator with, as its name implies, three poles and three zeros. This compensator would typically be used in applications where a type 3 compensator would be used but where the extra zero in the transfer function is desired to compensate for a pole in the input voltage sensor, for example.

This compensator has the transfer function:

$$H_{3p3z}(s) = \frac{\omega_{p0}}{s} \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right) \cdot \left(\frac{s}{\omega_{z2}} + 1\right) \cdot \left(\frac{s}{\omega_{z3}} + 1\right)}{\left(\frac{s}{\omega_{p1}} + 1\right) \cdot \left(\frac{s}{\omega_{p2}} + 1\right)}$$

Or expressed as a discrete compensator (when selected):

$$H_3(z) = K_z \cdot \frac{z^3 + B_2 \cdot z^2 + B_1 \cdot z + B_0}{z^3 + A_2 \cdot z^2 + A_1 \cdot z + A_0}$$

where the coefficients Kz, Bn and An are calculated internally in the compensator block using the bi-linear (Tustin) transform or can be imported from an external file.

Input pins:

EN — Enables the compensator for execution. A value < 1 at this pin will hold or freeze the current values within the compensator until the EN pin returns to ≥ 1.

Vsense(-) — The voltage sensing input (negative input to the compensator) in Volts.

Vset(+) — The set point voltage (positive input) in Volts.

Reset — A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to zero.

ADCint — If enabled in the dialog, the digital compensator will be sampled at the rising edge of this pin. Usually connected from the ADC SOC output or from any prior computational delay block output.

F(Hz) — If this pin is > 0, the frequency response will be enabled. Usually connected from the output of the model-based frequency response analysis block.

Output pins:

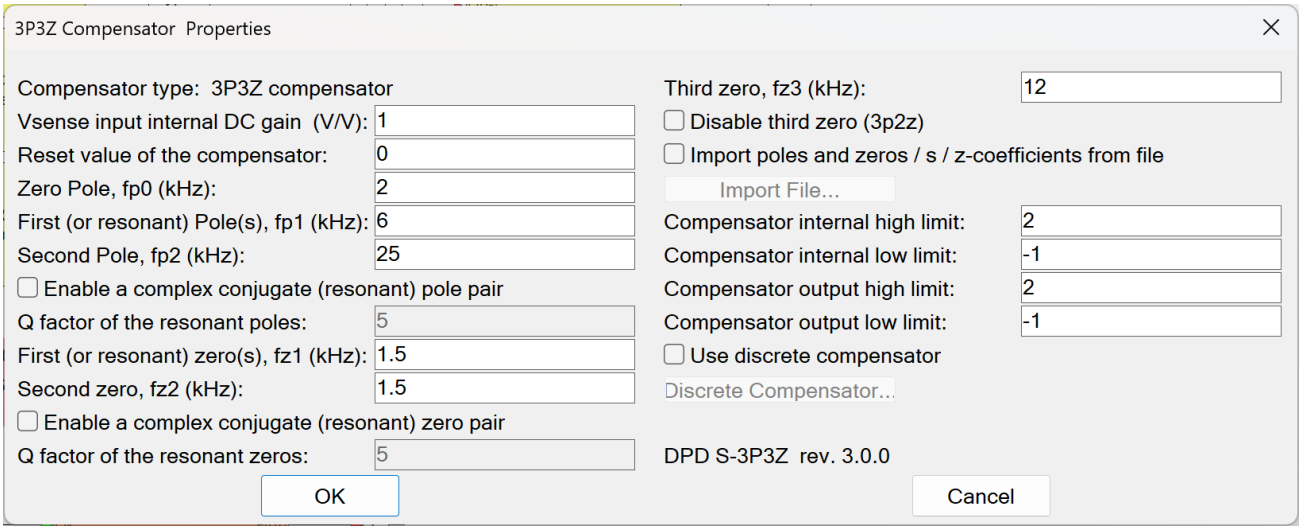
Vcorr — The output of the compensator.

So — An output pulse at the instant after the internal computation of the controller has been executed at every sample (used in digital control).

H(s/z) — The frequency response output in complex form either in the s-domain (analog compensator or in the z-domain (digital compensator).

Dialog properties:

The 3p3z compensator properties menu is shown in the following box which appears when right-clicking on the block.



Vsense input internal DC gain:

Enter the DC gain adjustment (if none = 1) before the error voltage is calculated and the voltage sensed is fed to the internal compensator input.

Internally:

$$Verr = Vset - Vsense*DCgain.$$

Reset value of the compensator:

Enter the value to which the compensator will initiate on a reset at the reset input pin.

Zero pole Fp0:

Enter the value of the compensator pole at the origin in kilohertz.

First pole Fp1:

Enter the value of the first pole of the compensator in kilohertz.

Second pole Fp2:

Enter the value of the second pole of the compensator in kilohertz

Enable a complex conjugate (resonant) pole pair:

Enable this if the double pole is to be set as a complex conjugate pair (resonant poles). Only the high-frequency poles will be affected. The zero pole will remain.

Q factor of the resonant poles:

Enter the resonant Q value of the complex pole pair

First zero Fz1:

Enter the value of the first zero of the compensator in kilohertz.

Second zero Fz2:

Enter the value of the second zero of the compensator in kilohertz.

Enable a complex conjugate (resonant) zero pair:

Enable this if the double zero is to be set as a complex conjugate pair (resonant zeros).

Q factor of the resonant zeros:

Enter the resonant Q value of the complex pole pair

Third zero Fz3:

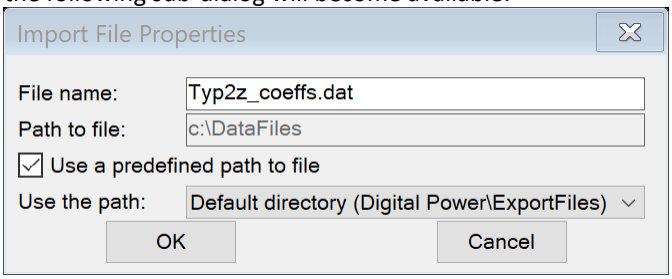
Enter the value of the third zero of the compensator in kilohertz.

Disable the third zero:

If selected, the third zero will be removed from the compensator, effectively creating a 3-pole, 2-zero compensator.

Import poles and zeros / s /z-coefficients from file:

If selected, the following sub-dialog will become available:



Check this box if the compensator poles and zeros are to be read from a file. This file can be typically generated by the compensator tools within the Tools section of the digital power designer or by other methods.

Note that if a discrete compensator is NOT selected then the compensator block will look for a poles and zeros format or s-coefficients within the file. If a discrete compensator is selected then the compensator block will look for a discrete coefficient format (z-coefficients) within the file.

If an incorrect file is selected, the compensator block will signal an error at the start of a simulation run and the block will turn red.

Compensator internal high limit:

Enter the high level internal limit of the compensator which is applied internally on the integrator of the compensator.

Compensator internal low limit:

Enter the low-level internal limit of the compensator.
NOTE that these limits are anti-windup limits.

Compensator external high limit:

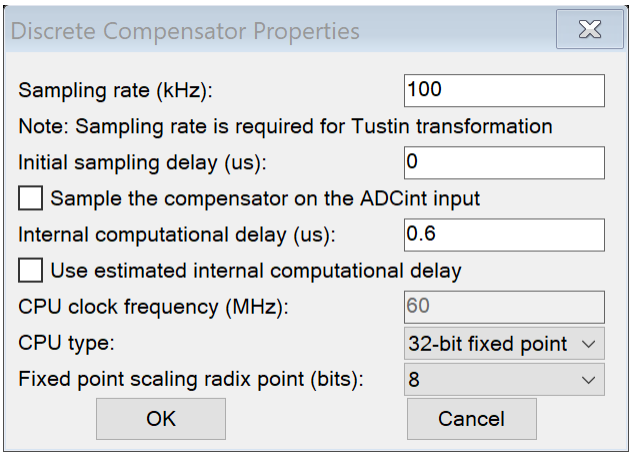
Enter the high level external limit of the compensator which is applied at the compensator output.

Compensator external low limit:

Enter the low-level external limit of the compensator which is applied at the compensator output.

Use discrete compensator:

Check this box if a discrete compensator is to be used in a simulation (digital control).



Sampling rate:

Enter the discrete compensator sampling rate in kHz.

NOTE: If an external file is used for the discrete coefficients, the sampling rate used to generate those coefficients must be equal to the value entered here. If the poles and zeros are entered manually, the discrete compensator coefficients will be generated for the entered sample rate using the Tustin transformation. For this reason, the sample rate is necessary even if the compensator is sampled at the ADCint input pin. If the sample rate at the ADCint input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (usually the sampling time of an ADC). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the ADCint input pin:

When enabled, the compensator will be sampled on the rising edge of the ADCint input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the internal compensator computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz in order to calculate the internal computational delay.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16.bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

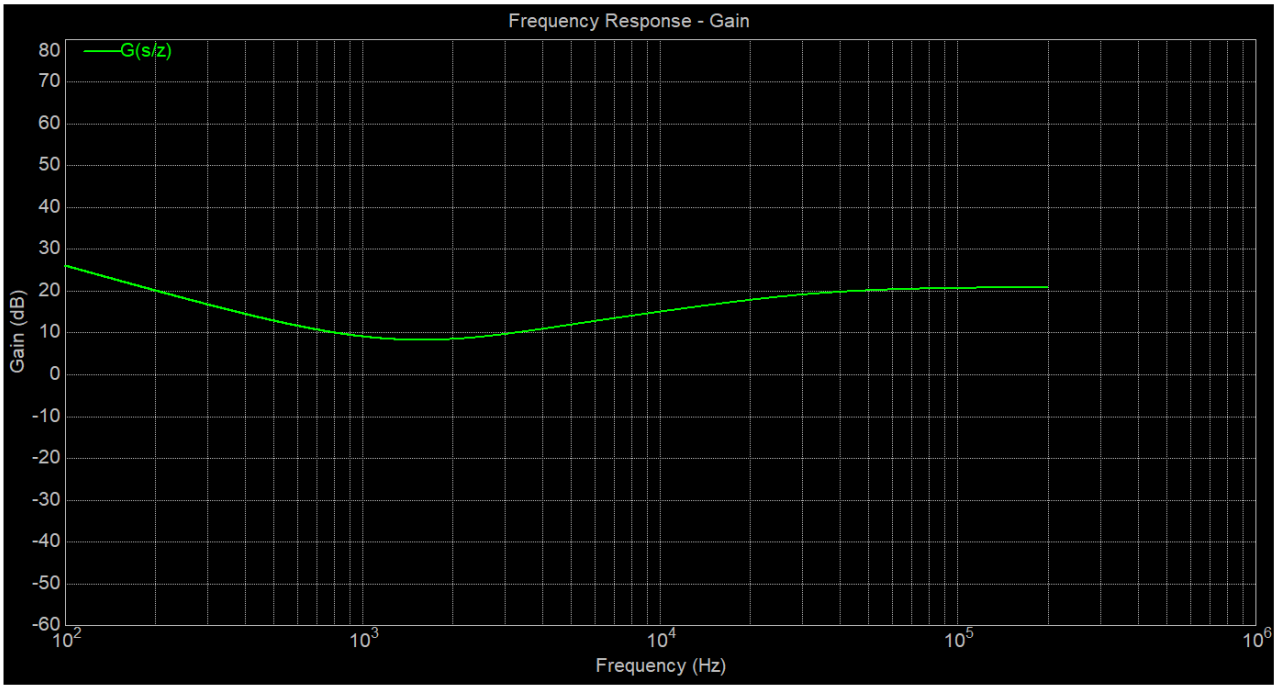
Fixed point scaling radix point:

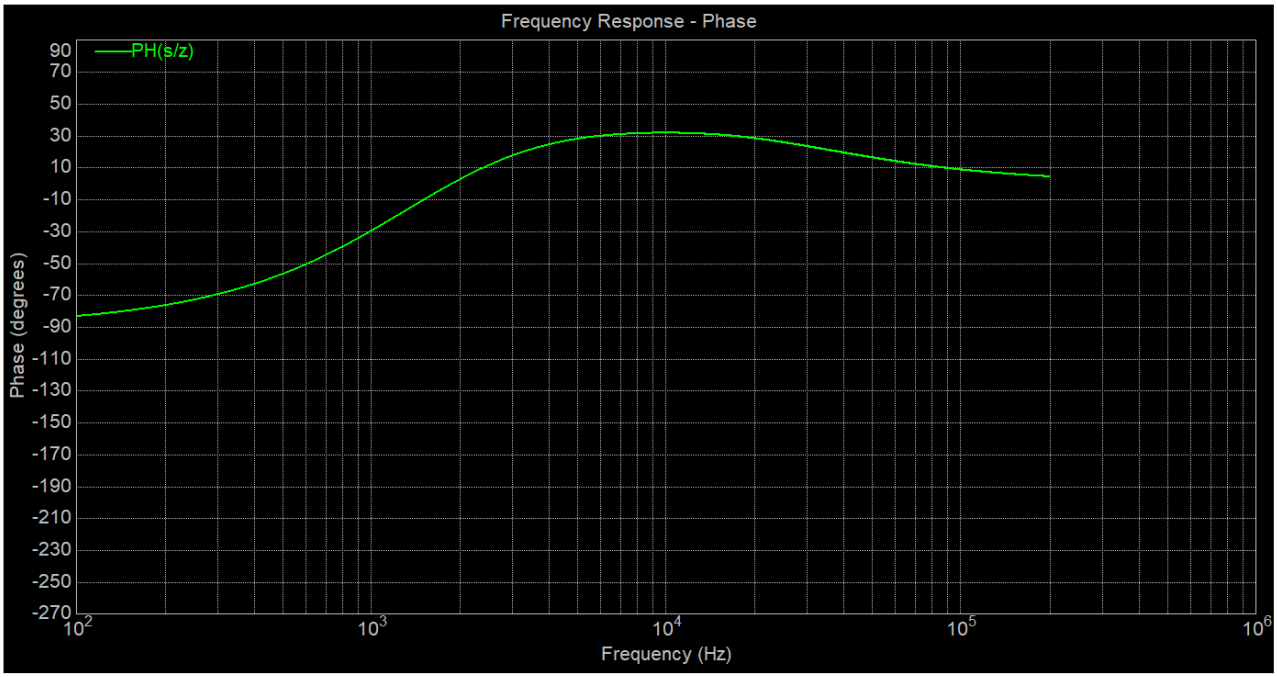
Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

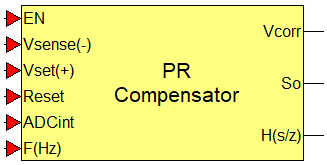
The Frequency Response of the compensator can be viewed internally in the 3p3z compensator block:

3p3z Compensator





Contents - Simulation



PR compensator

The Proportional plus resonant (PR) compensator is a second order compensator with two poles and two zeros. This type of compensator is typically used in a current controller for voltage oriented control of grid converters.

This compensator has the transfer function:

$$H_{PR}(s) = K_p + \frac{K_r \cdot \omega_c \cdot s}{s^2 + \omega_c \cdot s + \omega_0^2}$$

where K_p is the proportional gain, K_r is the resonant gain, ω_0 is the resonant frequency and ω_c is the resonant bandwidth. It is expressed as a discrete compensator (when selected):

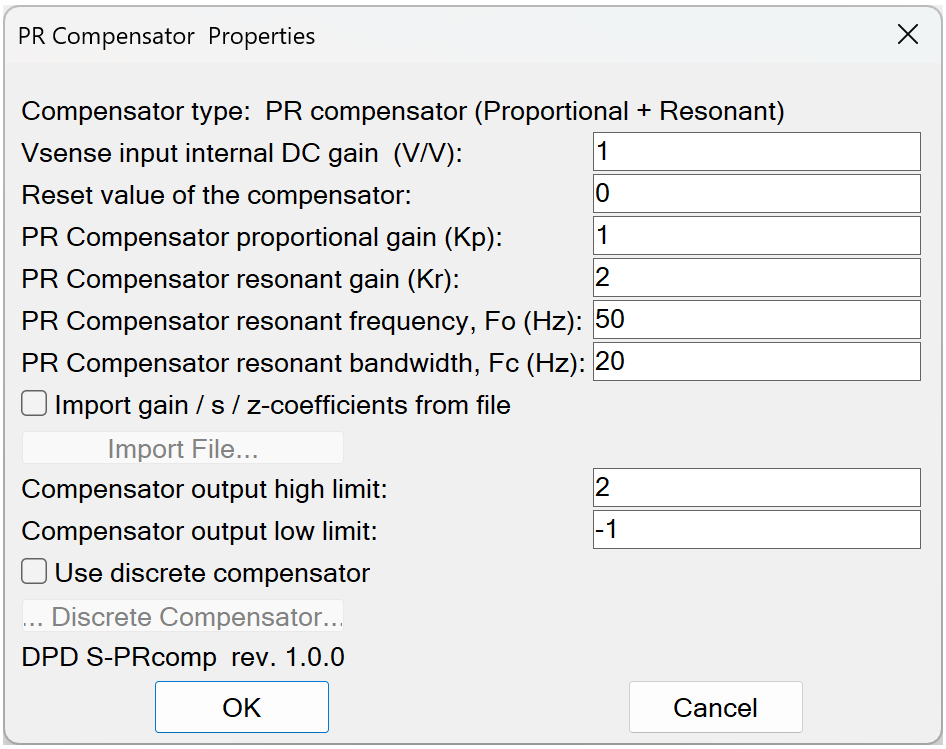
$$H_{2p2z}(z) = K_z \cdot \frac{z^2 + B_1 \cdot z + B_0}{z^2 + A_1 \cdot z + A_0}$$

where the coefficients Kz, Bn and An are calculated internally in the compensator block using the bi-linear (Tustin) transform or can be imported from an external file.

Input pins:	**EN**	Enables the compensator for execution. A value < 1 at this pin will hold or freeze the current values within the compensator until the EN pin returns to ≥ 1.
	Vsense(-)	The voltage sensing input (negative input to the compensator) in Volts.
	Vset(+)	The set point voltage (positive input) in Volts.
	Reset	A value ≥ 1 at this pin will hold the compensator in reset, resetting the internal integrators to zero.
	ADCint	If enabled in the dialog, the digital compensator will be sampled at the rising edge of this pin. Usually connected from the ADC SOC output or from any prior computational delay block output.
	F(Hz)	If this pin is > 0, the frequency response will be enabled. Usually connected from the output of the model-based frequency response analysis block.
Output pins:	**Vcorr**	The output of the compensator.
	So	An output pulse at the instant after the internal computation of the controller has been executed at every sample (used in digital control).
	H(s/z)	The frequency response output in complex form either in the s-domain (analog compensator or in the z-domain (digital compensator).

Dialog properties:

The PR compensator properties menu is shown in the following box which appears when right-clicking on the block.



Vsense input internal DC gain:

Enter the DC gain adjustment (if none = 1) before the error voltage is calculated and the voltage sensed is fed to the internal compensator input.

Internally:

$$Verr = Vset - Vsense*DCgain.$$

Reset value of the compensator:

Enter the value to which the compensator will initiate on a reset at the reset input pin.

PR compensator proportional gain, Kp:

Enter the value of the proportional gain.

PR compensator resonant gain, Kr:

Enter the value of the resonant gain.

PR compensator resonant frequency, Fo:

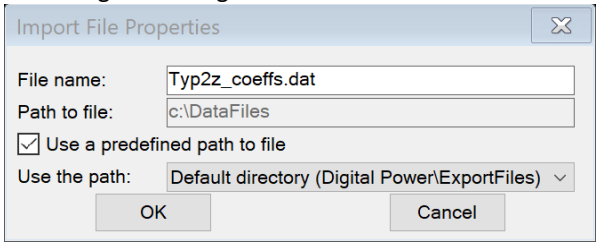
Enter the frequency of the AC resonance in Hertz (typically mains frequency).

PR compensator resonant bandwidth, Fr:

Enter the bandwidth of the resonant peak Hertz (typically a few Hertz).

Import poles and zeros / s /z-coefficients from file:

If selected, the following sub-dialog will become available:



Check this box if the compensator poles and zeros are to be read from a file. This file can be typically generated by the compensator tools within the Tools section of the digital power designer or by other methods.

Note that if a discrete compensator is NOT selected then the compensator block will look for a poles and zeros format or s-coefficients within the file. If a discrete compensator is selected then the compensator block will look for a discrete coefficient format (z-coefficients) within the file.

If an incorrect file is selected, the compensator block will signal an error at the start of a simulation run and the block will turn red.

Compensator high limit:

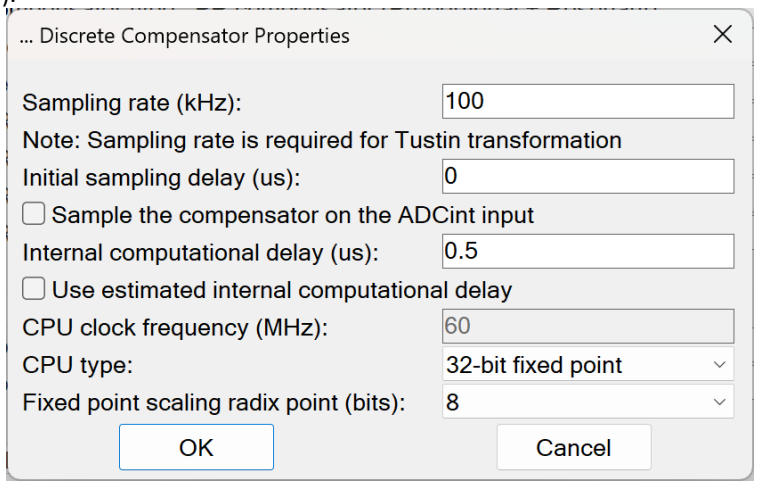
Enter the high level external limit of the compensator which is applied at the compensator output.

Compensator low limit:

Enter the low-level external limit of the compensator which is applied at the compensator output.

Use discrete compensator:

Check this box if a discrete compensator is to be used in a simulation (digital control).



Sampling rate:

Enter the discrete compensator sampling rate in kHz.

NOTE: If an external file is used for the discrete coefficients, the sampling rate used to generate those coefficients must be equal to the value entered here. If the poles and zeros are entered manually, the discrete compensator coefficients will be generated for the entered sample rate using the Tustin transformation. For this reason, the sample rate is necessary even if the compensator is sampled at the ADCint input pin. If the sample rate at the ADCint input pin is significantly different to the given sampling frequency here, a warning message will be generated.

Initial sampling delay:

Enter any prior time delay (usually the sampling time of an ADC). The input values will be sampled after this time delay at each sampling period. The time delay must be less than the sampling period for correct operation.

Sample compensator on the ADCint input pin:

When enabled, the compensator will be sampled on the rising edge of the ADCint input pin and the initial sampling delay above will be ignored.

Internal computational delay:

Enter the estimated delay for the internal compensator computation.

Use estimated internal computational delay:

Select this to use an estimated internal computational delay. The delay given above will be ignored in this case.

CPU clock frequency (MHz):

Enter the CPU clock frequency in MHz in order to calculate the internal computational delay.

CPU type:

Enter the CPU type. The choices are:

1. Floating point (FPU) e.g. TI Delfino, piccolo CLA, piccolo F2806x
2. 16.bit fixed-point e.g TI TMS320F240x, MSP430
3. 32-bit fixed point e.g. TI piccolo A and piccolo B.

NOTE: If the compensator is to be simulated running in the CLA then the sampling rate and entered time delay will reflect this and a FPU should be selected.

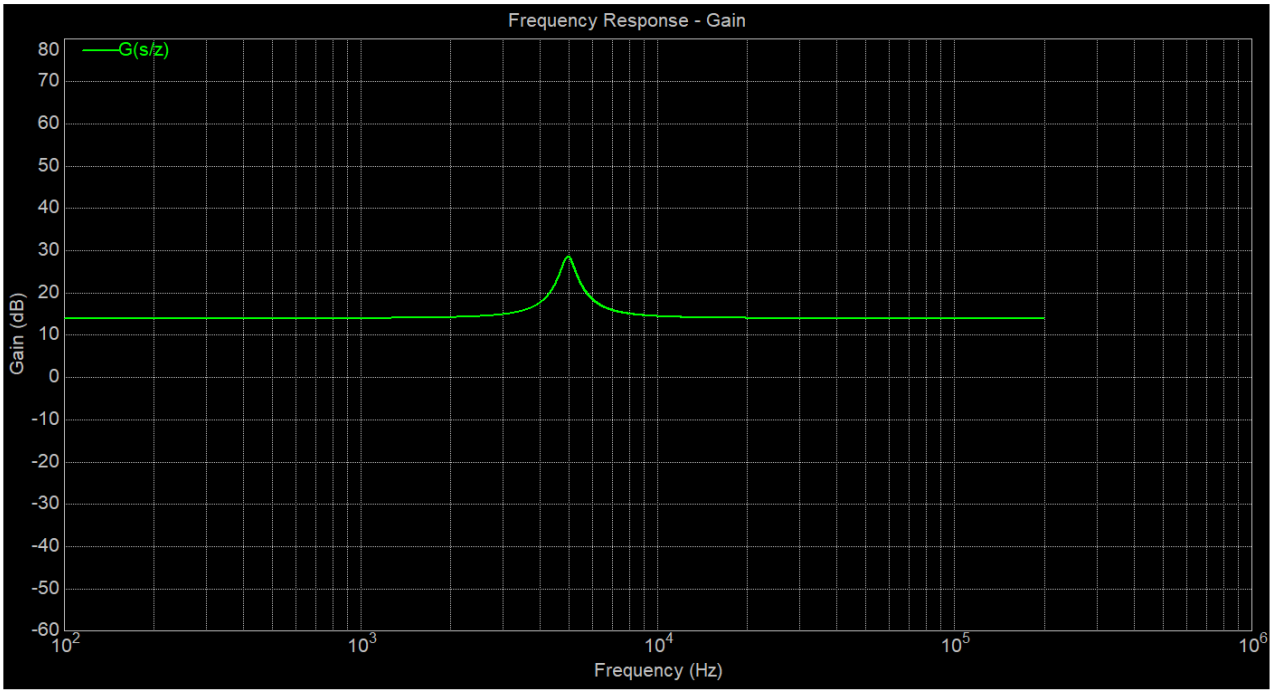
Fixed point scaling radix point:

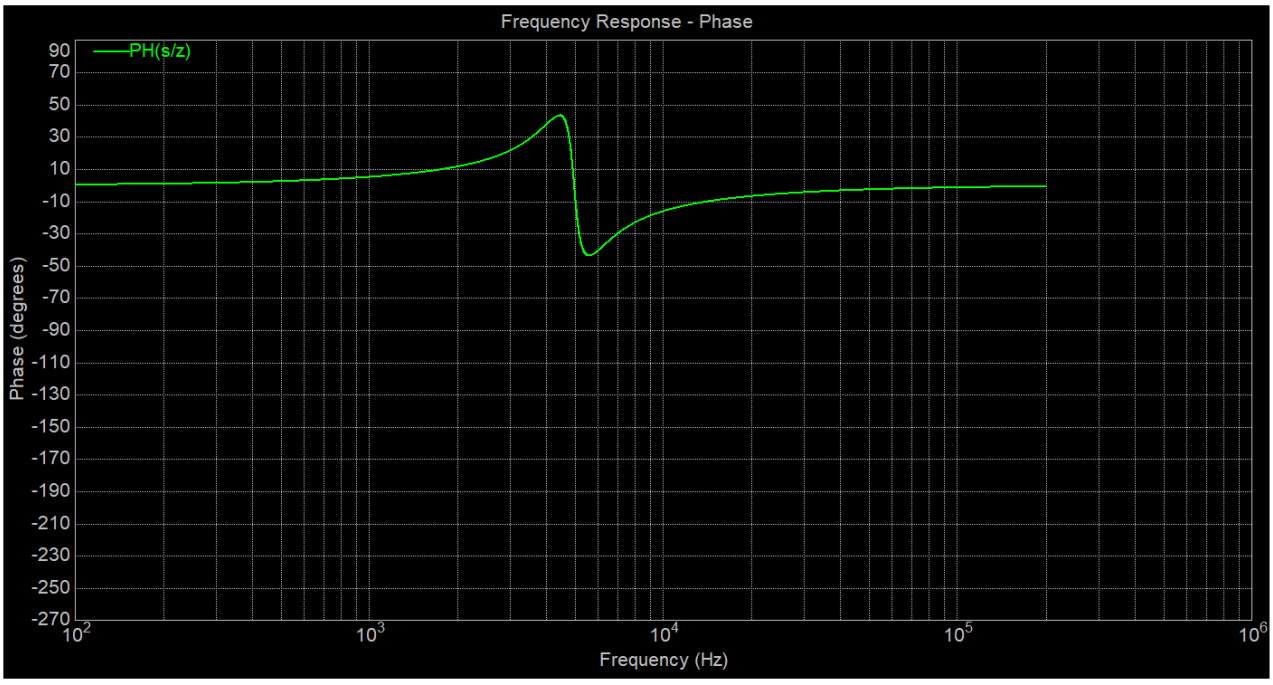
Enter the fixed-point radix scaling in bits. The radix scaling is the number of bits allocated to the whole number plus the sign bit.

e.g. For a fixed point scaling of fx4.16, 4 should selected here and a 16-bit CPU.

The Frequency Response of the compensator can be viewed internally in the 3p3z compensator block:

PR Compensator

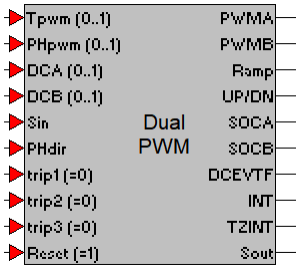




Contents - Simulation

MCU Peripherals

The MCU peripherals are a series of blocks designed to model the hardware peripherals typically embedded within a MCU for digital power applications. These blocks can be used together with the power converters and digital compensators to simulate digital power control routines. The MCU peripherals here are generally based upon the TI C2000 MCUs, though generic models for any MCU are available. Their default colour is grey to distinguish them from external hardware and software emulation blocks.



Dual PWM

This block is a dual, pulse width modulation (PWM) emulator with a common carrier (a triangular wave, ramp or also called the counter for digital PWM). It is based upon the TI C2000 ePWM peripheral and in particular the piccolo ePWM (type 1). However, this block is not 100% equivalent to the ePWM MCU hardware peripheral and the differences here should be taken into account when converting simulation diagrams into downloadable MCU diagrams for the C2000.

Input pins:

Tpwm The period of the dual PWM module carrier (ramp or counter) waveform. This period can vary during a simulation for variable-frequency control routines. Note that the period value at this pin sets the internal PWM counter period directly on a 1:1 basis for up or down count modes (scaled to 1, so that for a 16-bit counter as used internally in the block, a value of 1 at this pin corresponds to a counter value of 65535) and twice the PWM period for up/down count mode. This input pin is only enabled if the “change period dynamically” check box is selected in the dialog display of this block.

PHpwm The phase value of the counter on a sync event. If a sync event occurs (sync input pin or digital compare event; see below), the internal counter will be immediately loaded with this value. The value must be between 0 and 1 which corresponds to counter values of 0 to 65535.

DCA This input pin sets the duty cycle of any PWM waveform which is referenced to the compare A (CMPA) value within the dual PWM block. Note that this input does not set a CMPA value as with the C2000 but rather directly sets the duty cycle similar to the ePWM block (under Embedded menu).

DCB This input pin sets the duty cycle of any PWM waveform which is referenced to the compare B (CMPB) value within the dual PWM block. Note that this input does not set a CMPB value as with the C2000 but rather directly sets the duty cycle similar to the ePWM block (under Embedded menu).

Sin The sync input pin can be connected from an external source (GPIO pin), software (implemented with Embed blocks) or from another Dual PWM block sync out pin.

PHdir The phase direction pin. This pin is only active for up/down count mode as with the C2000 ePWM. It determines the direction of the counter (up or down) after a sync event. This is set as a pin so that it can be changed dynamically (see the relative figure on Dual PWM synchronization below for the use of this pin). When the input

to this pin is ≥ 1, the counter will count UP after a synchronisation event, when the input is < 1, the counter will count down after a synchronisation event.

Trip1 The trip inputs are similar to the trip zone (TZ) inputs on the C2000 ePWM. The trip inputs can cause either PWMA or PWMB to be reset low or set high (the high impedance option is not available), cause a sync event, send out a start of conversion pulse for an ADC or cause a trip-zone interrupt TZINT. The tripping of the PWM outputs can be cycle-by-cycle digital compare (CBC-DC) or cycle-by-cycle trip zone (CBC-TZ) or one-shot digital compare (OS-DC) or one-shot trip zone (OS-TZ). Refer to the relevant TI documentation for a more detailed description on the trip zone module within the C2000 ePWM peripheral. The basic difference between a CBC and a OS event as implemented here is that the CBC event is automatically reset while a OS event must be reset by software (in this case at the reset input pin). The basic difference between a DC CBC event and a TZ CBC event is that the DC trip is reset immediately the event is no longer present (the input pin returns high) while the TZ CBC trip is reset when the counter returns to zero. The trip input pins are active low (< 1).

Trip2 A second trip pin option.

Trip3 A third trip pin option.

Reset The reset pin enables a reset of the one-shot trip event. This is typically performed by software in the C2000 MCU and can be performed in a simulation diagram using standard Embed blocks. When the input to this pin is ≥ 1, a reset of a OS trip event will be performed, when the input is < 1, there will be no OS trip event reset. Note that if a OS event is enabled, it may be necessary to hold the reset active at the start of a simulation for a few simulation cycles to ensure that the Dual PWM block OS event is not set on simulation start.

Output pins: **PWMA** The PWM output A.

PWMB The PWM output B.

Ramp The ramp pin output is analogous to the counter register on the C2000 except that it is scaled from 0 to 1 for the graphical output representation. In this way, although the internal counter operates similarly to the C2000, the amplitude of this output pin does not vary with the counter period value.

UP/DN This output pin gives the current direction of the internal counter (1 = UP, 0 = DOWN).

SOCA The Start Of Conversion A (SOCA) signal out to initiate a conversion of an ADC block (If “Set SOC outputs as external GPIO output pins” is selected in the dialog display below, on a SOC this output will be active low for 32 SYSCLKOUT (CPU period) cycles, otherwise =1 for one time step only).

SOCB The Start Of Conversion B (SOCB) signal out to initiate a conversion of an ADC block similar to SOCA.

DCEVTF This output allows the visualization of the filtered blanking window.

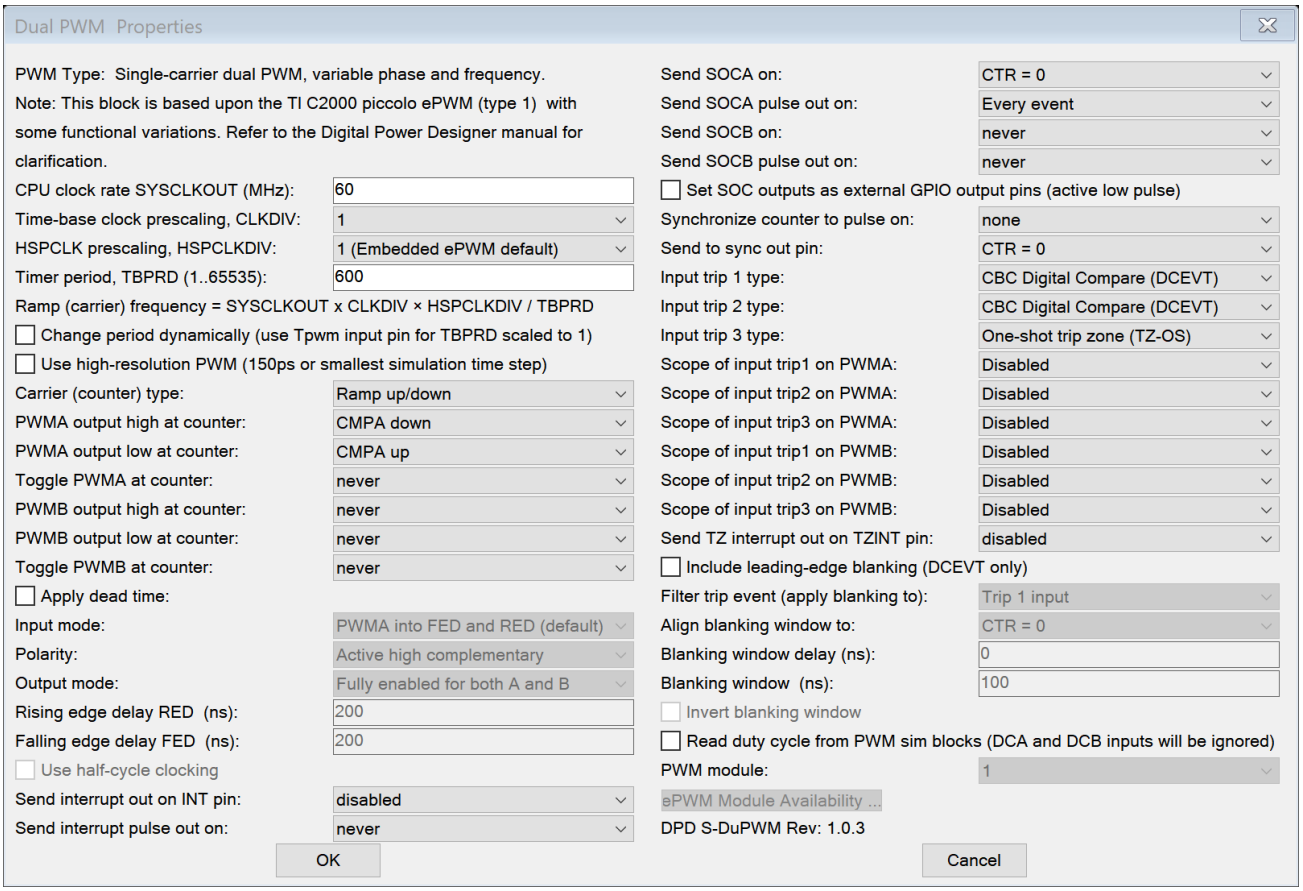
INT This output pin gives a high pulse (duration one simulation time step) according to the selected interrupt output as given in the dialog display.

TZINT This output pin gives a high pulse (duration one simulation time step) according to the selected interrupt trip input to be outputted as a trip-zone interrupt as given in the dialog display.

Sout The sync out pin which can be connected up to other Dual PWM blocks in order to synchronize their counters and eventually the PWM outputs.

Dialog properties:

The dual PWM block properties menu is shown in the following box which appears when right-clicking on the block.



CPU clock rate SYSCLKOUT:

The CPU rate is set with this value in MHz. This value will affect the PWM resolution and the internal timing and delays within the block.

Time base clock prescaling CLKDIV:

The counter pre-scaling and therefore the counter resolution can be set with this value.

HSPCLK prescaling HSPCLKDIV:

Another option for pre-scaling of the PWM counter. This value is set to a default of 1 when code is generated for the ePWM block (under the Embedded menu).

Timer period TBPRD (1..65535):

Set the timer period and therefore the PWM frequency with this pin. The counter frequency = SYSCLKOUT*CLKDIV*HSPCLKDIV/TBPRD for up count or down count modes and the counter frequency = SYSCLKOUT*CLKDIV*HSPCLKDIV/(2*TBPRD) for up/down count mode.

Change period dynamically:

If this box is checked, the above timer period value is ignored and the PWM period is set using the input pin **Tpwm**.

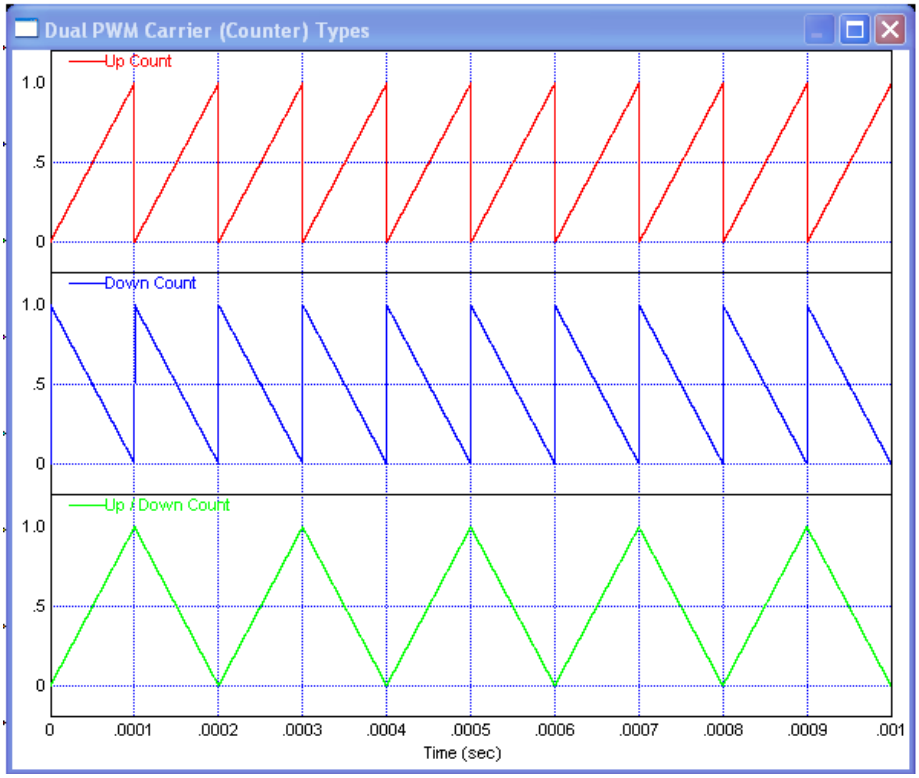
Use high resolution PWM:

Check this box to enable high resolution of the ePWM generation. Since the C2000 ePWM high resolution is set around 150ps, this would require a simulation time step of 75ps (or 13.3 GHz!) to represent it correctly and since such a time step would rarely be used in a simulation, the high resolution PWM rate is limited to the simulation time step for time steps greater than 150ps. The high resolution option is implemented by changing the resolution of the carrier (counter) waveform. This varies from the technique used for the C2000 which uses a proprietary Micro Edge Positioner (MEP). See the relevant TI documentation for details.

Carrier (counter) type:

The choices here are (see the figure below):

1. Up count
2. Down count
3. Up / down count



PWMA output high at counter:

Select the counter value at which the PWMA output is set to high (=1). The choices are:

1. Zero – The counter equals zero.
2. Period – The counter equals the maximum set value (the output pin ramp = 1).
3. CMPA up – The counter reaches the DCA input value on the UP count (not available for down count configuration).

4. CMPA down – The counter reaches the DCA input value on the DOWN count (not available for up count configuration).
5. CMPB up – The counter reaches the DCB input value on the UP count (not available for down count configuration).
6. CMPB down – The counter reaches the DCB input value on the DOWN count (not available for up count configuration).
7. Never – no action is taken.

PWMA output low at counter:

The choices and actions are the same as in PWMA output high above except that the PWM output will be reset to zero on the selected event.

Toggle PWMA output at counter:

The choices and actions are the same as in PWMA output high above except that the PWMA output will be toggled (the output will change its state) on the selected event.

PWMB output high at counter:

The choices and actions are the same as in PWMA output high above except that the PWMB output will be set to high (=1) on the selected event.

PWMB output low at counter:

The choices and actions are the same as in PWMA output high above except that the PWMB output will be reset to zero on the selected event.

Toggle PWMB output at counter:

The choices and actions are the same as in PWMB output high above except that the PWMB output will be toggled (the output will change its state) on the selected event.

Note that with this block configuration, only one event can be chosen for each type of action on a particular PWM output. In the C2000 ePWM (as in the ePWM block (under the Embedded menu)), any number of the available events can be assigned to a particular PWM action.

Apply dead time:

Check this box to apply a dead time between the two PWM outputs. This dead time can be configured in many different ways by setting the following options. This section emulates directly the dead-band generator sub-module in the C2000 ePWM (type 1) peripheral. For further information, refer to the relative TI documentation.

Input mode:

Select the scope of the dead time on the two PWM outputs. The choices are:

1. PWMA into FED and RED (default)
2. PWMB into RED, PWMA into FED
3. PWMB into FED, PWMA into RED
4. PWMB into FED and RED.

Polarity:

Select the polarity of the dead-time from the following:

1. Active high
2. Active low complementary
3. Active high complementary
4. Active low

These configurations are shown in the figure below.

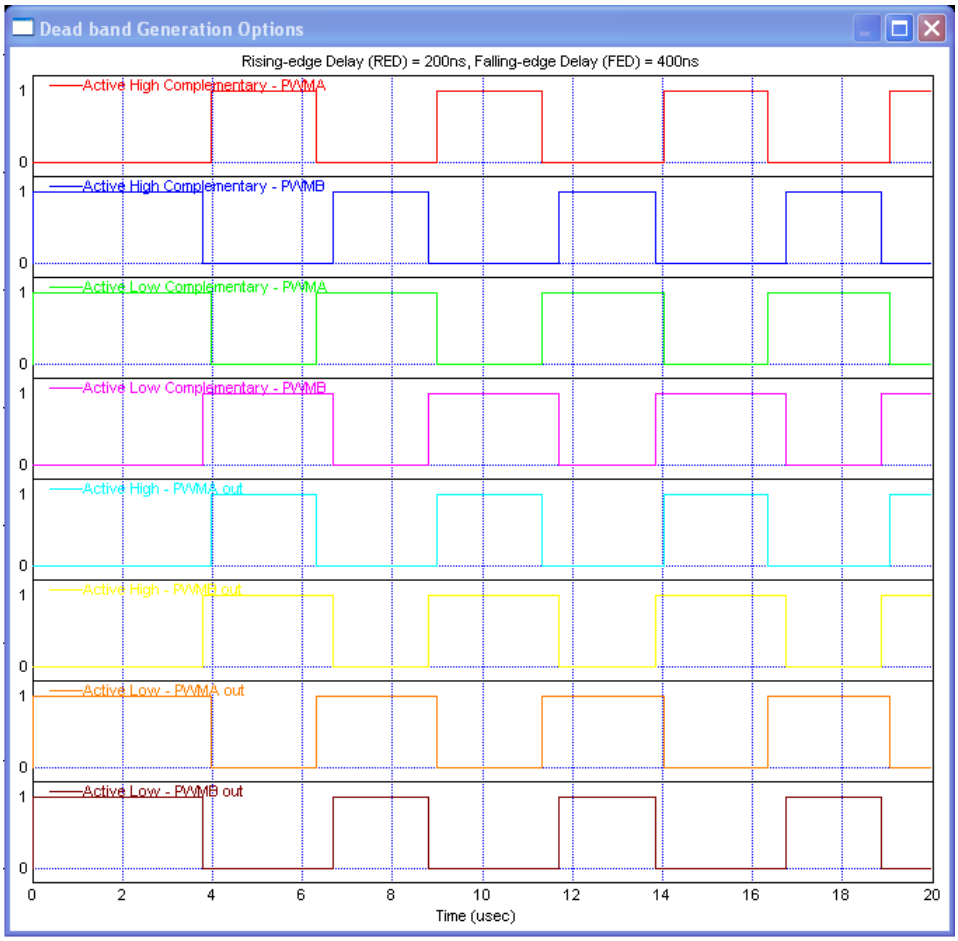
Rising edge delay:

Enter the desired value of the rising edge delay in nanoseconds

Falling edge delay:

Enter the desired value of the falling edge delay in nanoseconds.

Note that although the delays are entered in nanoseconds, the delays are discretized at 10 bit resolution emulating the C2000 type 1 ePWM dead-time module.



Use Half-cycle clocking:

By checking this box, no significant functional difference may be observed, however this feature will effectively double the resolution of the RED and FED delay times again emulating the C2000.

Send interrupt out on INT pin:

Select the source or event which will send a pulse out to the INT output pin. This pulse is used to generate an interrupt at a certain precise moment within the PWM cycle. The choices here are:

1. Disabled
2. CTR = 0 – Generate an interrupt when the counter reaches zero.
3. CTR = Period – Generate an interrupt when the counter reaches the period value.
4. CTR = 0 or Period - Generate an interrupt when the counter reaches zero value or the period value.

5. CMPA up – Generate an interrupt when the counter equals the DCA input on the up count.
6. CMPA down – Generate an interrupt when the counter equals the DCA input on the down count.
7. CMPB up – Generate an interrupt when the counter equals the DCB input on the up count.
8. CMPB down – Generate an interrupt when the counter equals the DCB input on the down count.

Send interrupt pulse out on:

Here the choices are:

1. Never
2. Every event
3. Every 2nd event
4. Every 3rd event

The output pin will normally be low (zero) and go high (=1) for one simulation time step on the selected interrupt event.

Send SOCA on:

Select the source or event which will send a pulse out to the SOCA output pin. This pulse is used to send a Start Of Conversion to an analog-to-digital converter (ADC). The choices here are:

1. Never
2. CTR = 0 – Send a SOC when the counter reaches zero.
3. CTR = Period – Send a SOC when the counter reaches the period value.
4. CTR = 0 or Period – Send a SOC when the counter reaches the period value.
5. CMPA up – Send a SOC when the counter equals the DCA input on the up count.
6. CMPA down – Send a SOC when the counter equals the DCA input on the down count.
7. CMPB up – Send a SOC when the counter equals the DCB input on the up count.
8. CMPB down – Send a SOC when the counter equals the DCB input on the down count.
9. Trip 1 – Send a SOC when a trip 1 event occurs (only applicable when configured as a digital compare).
10. Trip 2 1 – Send a SOC when a trip 2 event occurs (only applicable when configured as a digital compare).
11. Trip 3 1 – Send a SOC when a trip 3 event occurs (only applicable when configured as a digital compare).

Send SOCA pulse out on:

Here the choices are:

1. Never
2. Every event
3. Every 2nd event
4. Every 3rd event

Send SOCB on:

Select the source or event at which a pulse is sent at the SOCB output pin. The selection and actions are the same as for SOCA.

Send SOCB pulse out on:

The selection here is the same as for SOCA.

Set SOC outputs as external GPIO output pins.:

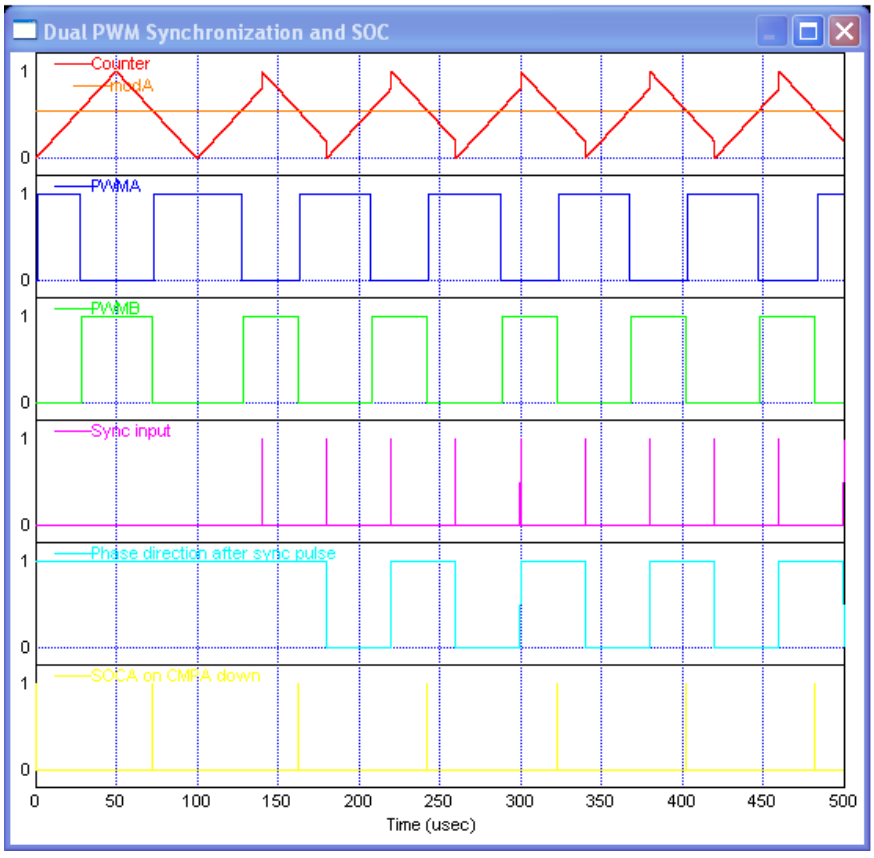
If the check box is selected then the SOC output will be active low. i.e. they will normally be high (=1) and go low (=0) on the selected SOC event for 32 SYSCLKOUT cycles. Otherwise, if unchecked, the SOC output pins will normally be low and go high for one simulation time step on the selected SOC event.

Synchronize counter to pulse on:

Set the event on which to synchronise the counter. The choices are:

1. None
2. Trip 1
3. Trip 2
4. Trip 3

Note that the trip signals must be set as digital compare (DC) events. The selected event is ORed with the Sin input pin similar to the C2000 piccolo ePWM.



Send to sync out pin:

Select the event at which to send an output pulse on the output sync pin Sout. The choices are:

1. Disabled

2. CTR = 0 – the counter has returned to zero.
3. CTR = CMPB – the counter equals the internal counter compare B input (calculated from the duty cycle DCB input).
4. ePWMxSYNC signal – the output pulse is the internally set sync signal (input sync pin or the selected trip event).

Input trip 1 type:

Configure the type of PWM trip event for the input trip 1. The choices here are:

1. CBC Digital Compare (reset after the event is cleared).
2. One-Shot Digital Compare.
3. CBC trip zone (reset when the counter returns to zero).
4. One-shot trip zone.

Input trip 2 type:

Second input trip configuration. See the description above on the Trip 1 input pin for a description on the trip types.

Input trip 3 type:

Third input trip configuration. See the description above on the Trip 1 input pin for a description on the trip types.

Scope of input trip 1 on PWMA:

Configure the action taken on the PWMA output on a trip 1 event. The choices here are:

1. Disabled
2. Force low
3. Force high

Note that a high impedance output option is not available.

Scope of input trip 2 on PWMA:

Configure the action taken on the PWMA output on a trip 2 event.

Scope of input trip 3 on PWMA:

Configure the action taken on the PWMA output on a trip 3 event.

Scope of input trip 1 on PWMB:

Configure the action taken on the PWMB output on a trip 1 event.

Scope of input trip 2 on PWMB:

Configure the action taken on the PWMB output on a trip 2 event.

Scope of input trip 3 on PWMB:

Configure the action taken on the PWMB output on a trip 3 event.

Send TZ interrupt out on TZINT pin:

This selection will allow a trip interrupt pulse to be sent out on the TZINT pin. The choices are:

1. Disabled
2. Trip 1 – only generated on a digital compare event.
3. Trip 2 – only generated on a digital compare event.
4. Trip 3 – only generated on a digital compare event.
5. CBC trip event – generated on any cycle-by-cycle event.
6. OS trip event – generated on any one-shot event.

Include leading edge blanking:

Check this box to include a blanking window (filter) on the selected trip event.

Filter (apply blanking) to trip event:

Leading-edge blanking (LEB) is normally applied to a trip signal in order to filter that signal or more precisely “ignore” it for a given window of time. This is useful to filter out any noise impulses during the switching instant of power semiconductor devices.

Select the source for the filtered signal for blanking. The choices are:

1. Trip 1 input
2. Trip 2 input
3. Trip 3 input
4. PWMA trip
5. PWMB trip

Note that this selection varies from the blanking configuration of the TI C2000 ePWM leading-edge blanking (LEB) configuration. Please refer to the appropriate TI documentation. In this block, either one of the trip inputs or the actual trip on the PWM output can be blanked.

Align blanking window to:

The blanking window can be aligned to:

1. CTR = 0
2. CTR = period.

Blanking window delay:

Enter the delay time at which the blanking window commences (aligned as above), in nanoseconds.

Blanking window:

Enter the width of the blanking window in nanoseconds.

Note that although the blanking time delay and window are given in nanoseconds, the times are discretized to emulate the C2000 blanking time sub-module.

Invert blanking window:

Select this box to invert (phase shift) the blanking window.

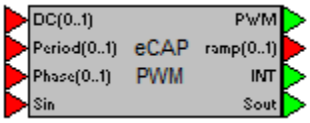
Read duty cycle from PWM sim blocks:

Select this if the duty cycle is to be read from the PWM sim blocks. In this case the values at the input pins DCA and DCB will be ignored.

PWM module:

Select the PWM module used within the code-gen diagram of which the duty cycle is read at its input.

Contents - Simulation



eCAP-PWM

This block is based upon the TI C2000 eCAP peripheral sub-module for Asynchronous PWM.

Input Pins:

DC The duty cycle input from 0 to 1. Note that this is not a compare value input.

Period The value at this pin will set the period value of the PWM carrier (Up counter). The input value is the value of the 32-bit counter scaled from 0 to 1.

Phase The value at this pin will set the phase value of the PWM carrier. The input value is the value of the 32-bit counter scaled from 0 to 1. The counter will be set to this value at the instant that the input Sin pin goes high.

Sin Input pin to synchronize the counter with other eCAP modules or PWM modules.

Output pins:

PWM The PWM output.

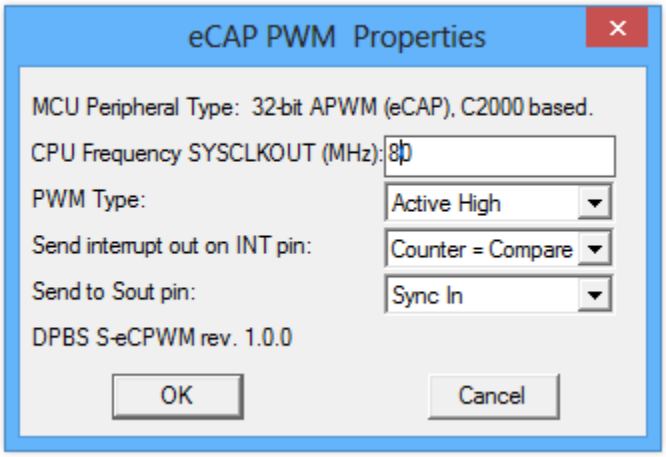
ramp The internal counter value scaled from 0 to 1 for all periods.

INT Interrupt output pin (active high for one simulation time step).

Sout Synch output pin (active high for one simulation time step).

Dialog properties:

The eCAP-PWM block properties menu is shown in the following box which appears when right-clicking on the block.



CPU Frequency SYSCLKOUT:

Enter the CPU frequency in MHz.

PWM type:

Select either active high (the ON-time is set) or active low (the OFF-time is set).

Send out to INT pin an interrupt on:

Send an one-sample-time active-high output pulse to the INT pin. The choices here are:

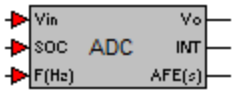
1. Disabled
2. Counter = Compare
3. Counter = period
4. Counter overflow

Send to Sout pin:

Send an one-sample-time active-high output pulse to the Sout pin. The choices here are:

1. Disabled
2. Counter = period
3. Sync In

Contents - Simulation



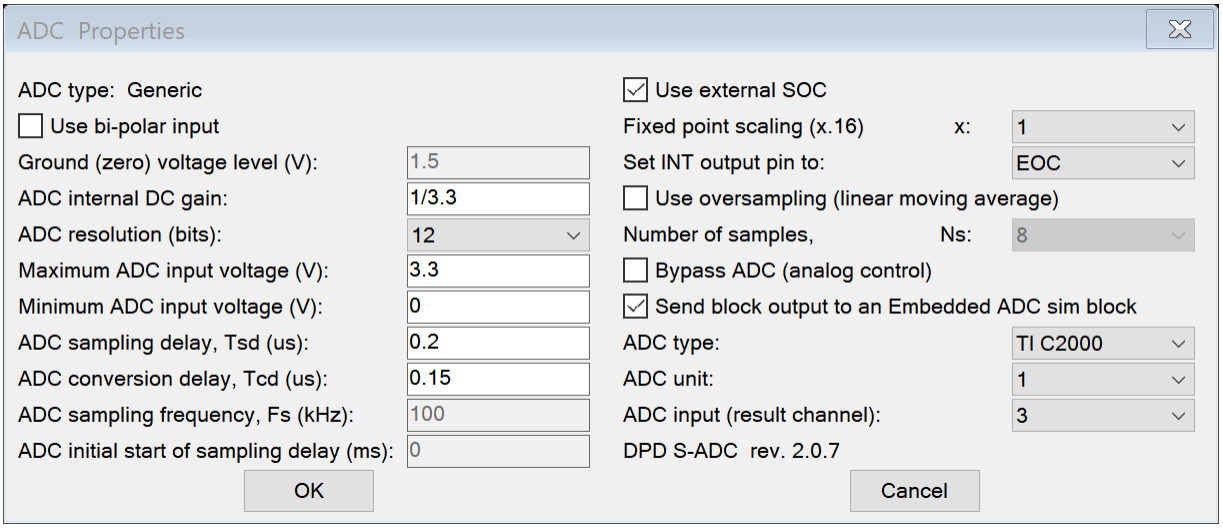
Analog to Digital converter (ADC)

This block is a generic ADC block which can be set up similar to the TI C2000 peripheral by appropriately setting the necessary fields in the dialog properties.

Input Pins:	**Vin**	Input analog voltage (V).
	SOC	Start Of Conversion input.
	F(Hz)	Frequency input for frequency response analysis.
Output pins:	**Vo**	Output digital voltage in Volts.
	INT	Output pulse on an interrupt event.
	AFE(s)	Frequency response output.

Dialog properties:

The ADC block properties menu is shown in the following box which appears when right-clicking on the block.



Use bi-polar input:

Check this box if a bi-polar input is applied at the Vin input pin.

Ground (zero) voltage level:

Set the ground reference voltage.

ADC internal DC gain:

Enter the internal ADC DC gain.

ADC resolution:

Select the ADC resolution form 6 to 16 bits. The TI C2000 ADC has a resolution of 12 bits.

Maximum ADC input voltage:

The maximum convertible input voltage or ADC high-level saturation voltage.

Minimum ADC input voltage:

The minimum convertible input voltage or low-level saturation voltage.

ADC sampling delay Tsd:

Enter the sampling delay time (time for a full sample at the ADC output) in microseconds.

ADC sampling frequency:

If no external SOC is used, enter the required ADC sampling frequency in kilohertz. An error will occur if the sampling period is shorter than the sampling delay time.

Use external SOC:

Check this box if the sampling frequency is to be ignored and the external input pin is used to start the ADC conversion.

Fixed point scaling (x.16):

Within the Embed environment, the ADC output is set to fx1.16 for the piccolo and fx4.16 for the F280x, which provides full 12-bit resolution from 0 to 1.

Set INT output to:

Choose from SOC or EOC for the interrupt output pin.

Use oversampling:

Check this box if oversampling is to be applied.

Number of samples, Ns:

Enter the number of samples to be decimated into one sample. For example, if the ADC sampling rate is 100kHz and the number of samples is set to 4 here, the effective ADC sampling frequency will be reduced to 25kHz, however the output resolution of the sampled input signal will be improved (theoretically) by 1 bit.

Bypass ADC:

Check this box if the entire ADC block is to be bypassed. This is useful if, when debugging a diagram, one can easily change from an analog control to a digital control without removing or disconnecting blocks.

Send block output to an embedded ADC sim block:

Check this box if the ADC output is to be sent to an embedded ADC sim block for simulation within a code-generable diagram.

ADC Type:

The choices are:

1. TI C2000
2. STM32
3. Cortex M3
4. Arduino
5. Generic MCU

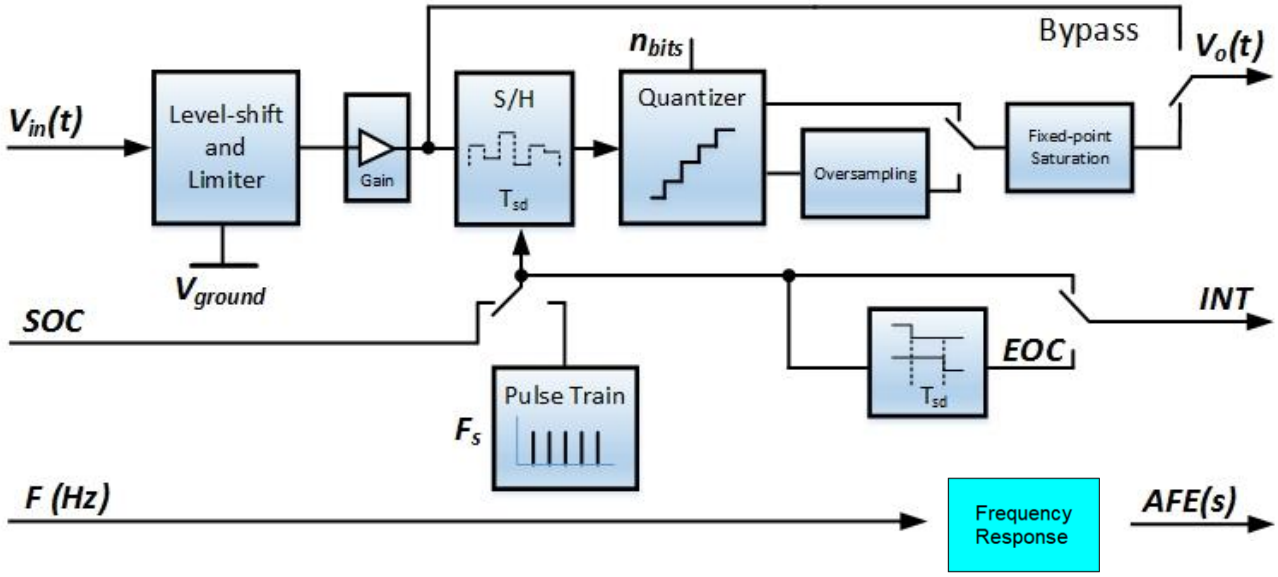
ADC unit:

Select the ADC unit from 1 to 4.

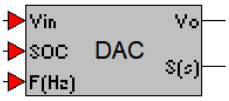
ADC input (result channel):

Select the ADC result channel form 0 to 15.

The ADC block is internally structured as follows:



Contents - Simulation



Digital to Analog converter (DAC)

This block is a generic DAC block which can be set up similar to the TI C2000 peripheral by appropriately setting the necessary fields in the dialog properties.

Input Pins: **Vin** Input voltage in Volts. This input can be represented in bits if the DAC internal DC gain is set accordingly.

SOC Start Of Conversion input.

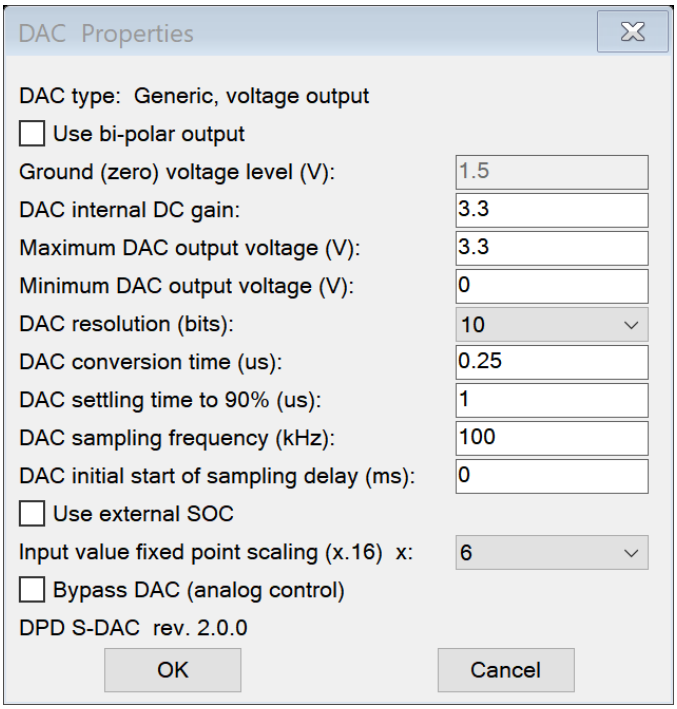
F(Hz) Frequency input for frequency response analysis.

Output pins: **Vo** Output analog voltage.

S(s) Frequency response output.

Dialog properties:

The DAC block properties menu is shown in the following box which appears when right-clicking on the block



Use bi-polar output:

Check this box if a bi-polar output is required

Ground (zero) voltage level:

Set the ground reference voltage.

DAC internal DC gain:

Enter the internal DAC DC gain.

DAC resolution:

Select the DAC resolution form 6 to 16 bits. The TI C2000 piccolo DAC has a resolution of 10 bits.

Maximum DAC output voltage:

The output high-level limit or saturation voltage.

Minimum DAC output voltage:

The output low-level limit.

DAC settling time to 90%:

This is the typical settling time of the output voltage to within 90% of its expected value.

DAC sampling frequency:

Enter the required DAC sampling frequency in kilohertz.

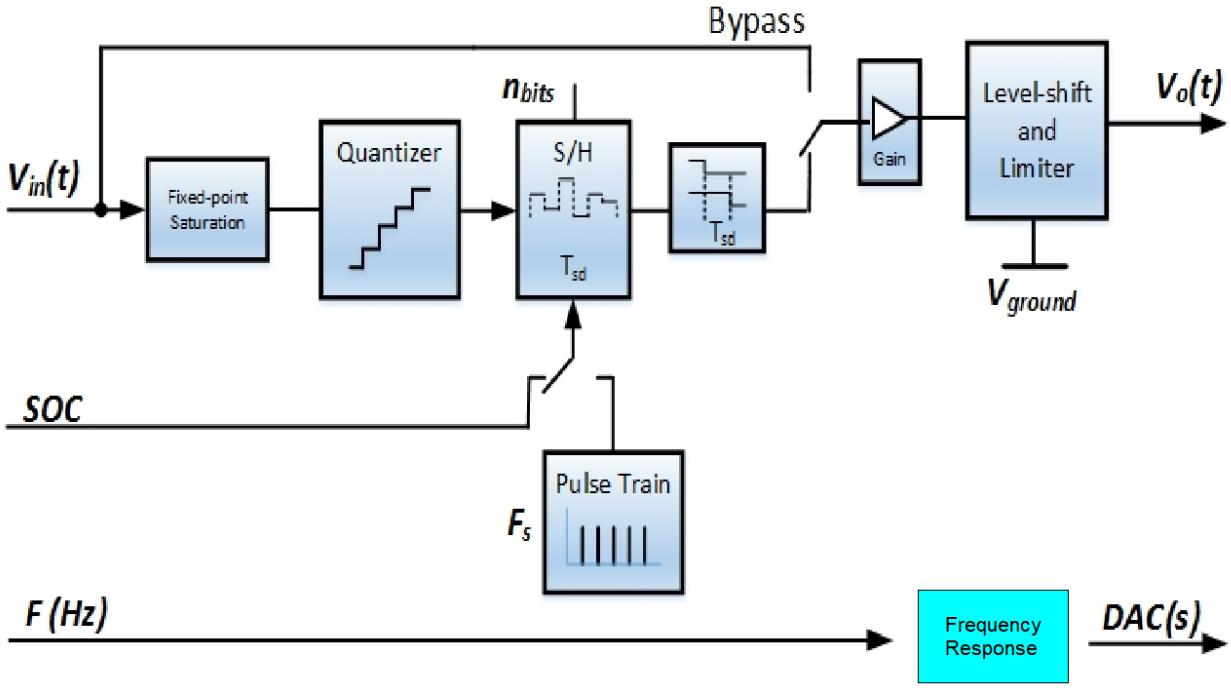
Use external SOC:

Check this box if the sampling frequency is to be ignored and the external input pin is used to start the DAC conversions.

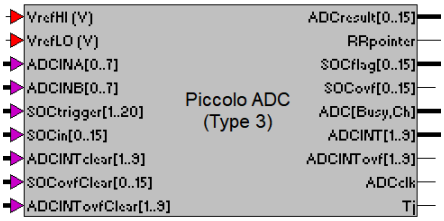
Input value fixed point scaling (x.16):

Within the Embed environment, the DAC input is set to fx6.16 which provides full 10-bit resolution from 0 to 1.

The DAC block is internally structured as follows:



Contents - Simulation



Piccolo ADC (C2000 Type 3)

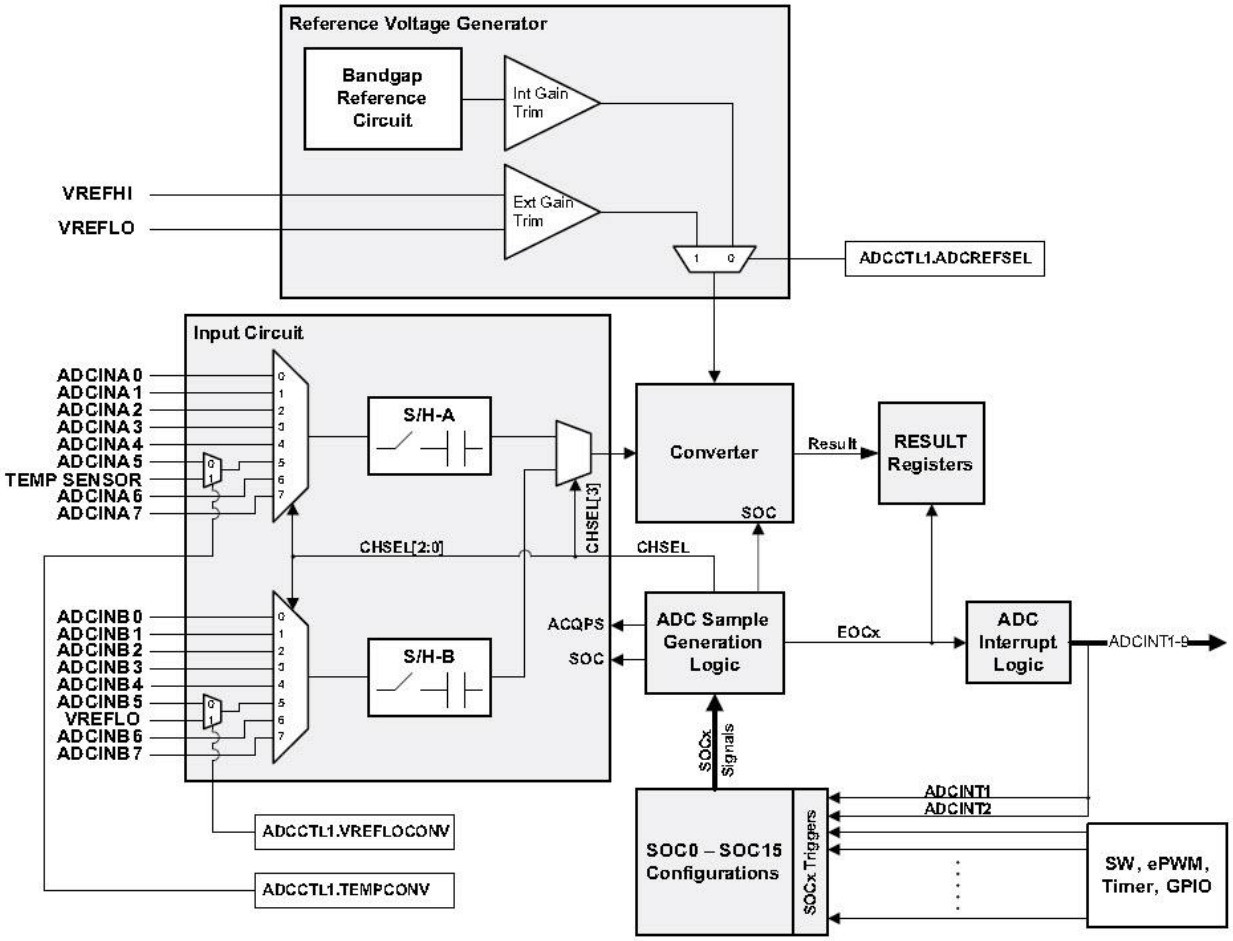
This block is a specific ADC model of the TI C2000 type 3 ADC peripheral. It contains a dual-sampler and one ADC. The block models as closely as possible the piccolo ADC peripheral in order to enable high fidelity simulations and to check ADC timing in control routines.

The configuration can be exported to a file and that file can be used to configure the ADC peripheral in piccolo MCUs identically to the simulation configuration.

This block is currently in a preview status and will be finalised for complete ADC emulation in a later revision of the Digital Power Designer.

Input Pins:	**VrefHI (V)**	If the external reference voltage is enabled, this is the upper level of the reference voltage in volts.
	VrefLO (V)	If the external reference voltage is enabled, this is the lower level of the reference voltage in volts.
	ADCINA[0..7]	Analog inputs: 8 element input vector for the first or A sampler.
	ADCINB[0..7]	Analog inputs: 8 element input vector for the second or B sampler.
	SOCtrigger[0..20]	SOC trigger inputs: 20 element input vector.
	SOCin[0..15]	Start of Conversion (SOC) inputs: 16 element input vector.
	ADCINTclear[0..9]	Inputs to clear the ADCINT flags: 10 element input vector.
	SOCovfClear[0..15]	Inputs to clear the SOC overflow flags: 16 element input vector.
	ADCINTovfClear[0..9]	Inputs to clear the ADCINT overflow flags: 10 element input vector.
Output pins:	**ADCresult[0..15]**	The result values of the ADC conversion in the specified result and the specified format.
	RRpointer	Round robin pointer value.
	SOCflag[0..15]	Start of Conversion flags: 16 element output vector.
	SOCovf[0..15]	Start of Conversion overflow flags: 16 element output vector.
	ADC[Busy,Ch]	ADC busy and the current channel being converted.
	ADCINT[0..9]	ADC interrupt flags: 10 element output vector.
	ADCINTovf[0..9]	ADC interrupt overflow flags: 10 element output vector.
	ADCclk	The ADC clock is output at this pin.
	Tj	Junction temperature of the chip in the specified units. The temperature sensor must be enabled and the power dissipation is then input at the ADCINA[5] input.

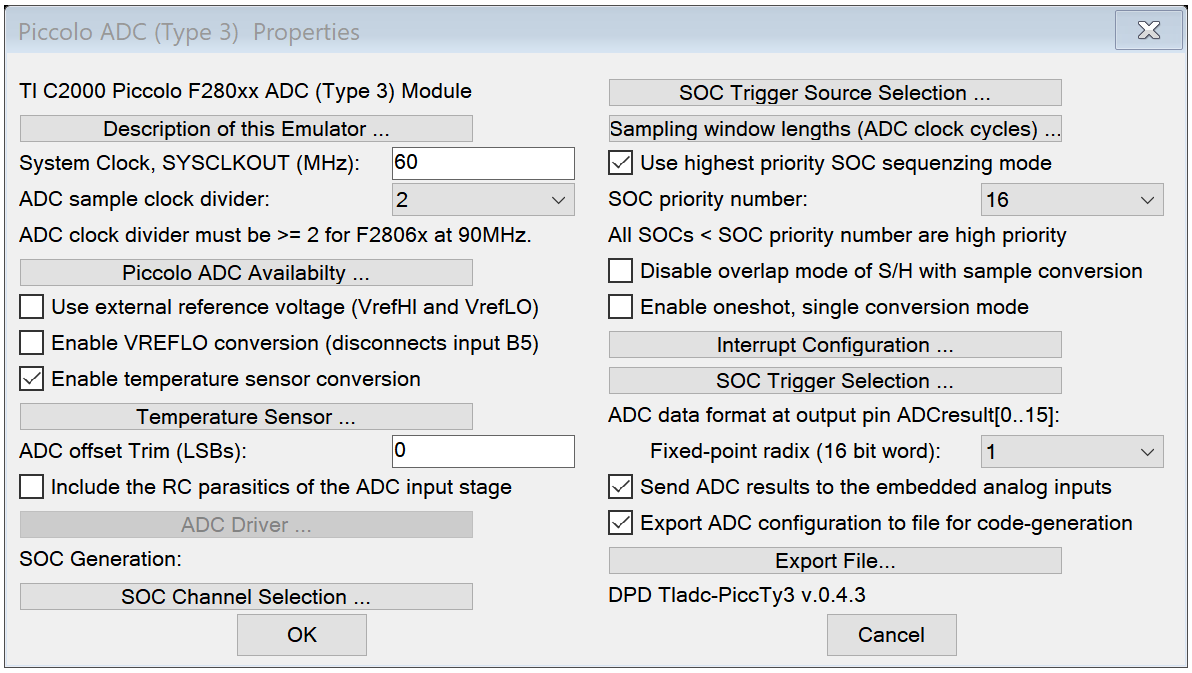
The ADC Type 3 peripheral found in the Texas Instruments C2000 Piccolo microcontroller series F2802x, F2803x, F2805x and F2806x:



Extract form the Texas Instruments TMS320F2803x Technical Reference Manual, spui10.pdf http://www.ti.com/lit/ug/sprui10/sprui10.pdf
Also refer to the relevant TI C2000 datasheets for the specific device.

Dialog properties:

The Piccolo ADC (Type 3) block properties menu is shown in the following box which appears when right-clicking on the block



System clock, SYSCLKOUT (MHz):

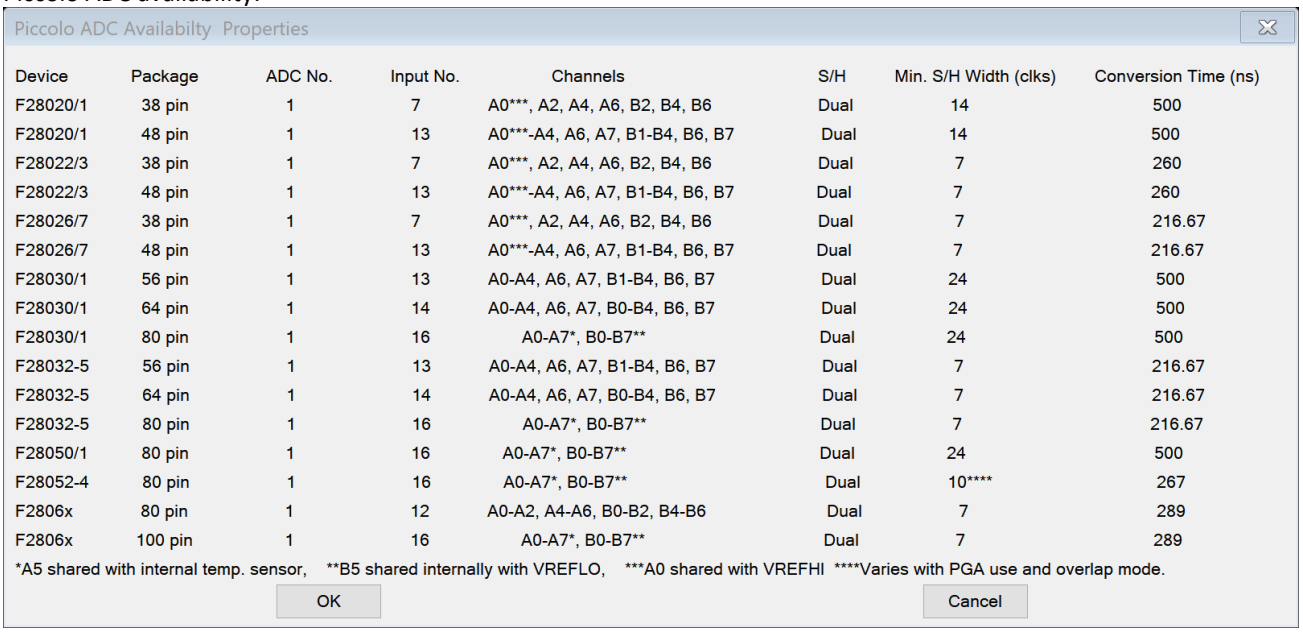
Enter the value of the system CPU clock in MHz.

Note that all of the following configuration settings will be set in the export file (if enabled) which can be used in a diagram to completely configure the ADC peripheral., overriding the embed diagram ADC configuration.

ADC sample clock divider:

Select the clock divider applied to the CPU clock above for the ADC clock and operation. The selections available are 1, 2 or 4. Note that a divisor of 4 is available only on the F2806x since it normally operates at 90MHz. The maximum ADC operation is at a 40MHz clock (refer to TI data sheets).

Piccolo ADC availability:



Use external reference voltage (VREFHI and VREFLO):

Select this if the external reference voltage is to be used. The voltage value at the inputs pins VREFHI and VREFLO will be used instead of the internal 3.3V reference such that:

$$Vref = (VREFHI - VREFLO)$$

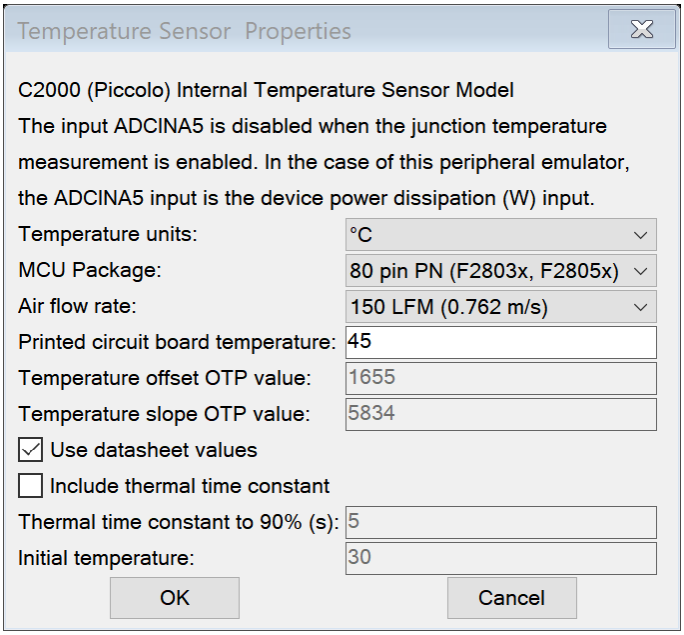
and all ADC results will be offset by VREFLO. Any input voltage below VREFLO will convert to a value of 0h.

Enable VREFLO conversion:

Select this if it is desired to sample and convert VREFLO. The input at ADCINB5 will be disconnected and the voltage VREFLO will be connected internally on this channel.

Enable temperature sensor conversion:

Select this if it is desired to monitor the chip junction temperature. The input at ADCINA5 will be disconnected in the microcontroller. In the case of this emulator however, the input at ADCINA5 becomes the power dissipation input (W) of the device. On the selection of this option, the following dialog will become available:



Temperature units:

The choices here are:

1. °C
2. °F
3. K

The emulator will calculate all temperature values in the defined unit.

MCU package:

Select the MCU package of the device used.

Air flow rate:

Select the airflow rate around the MCU chip.

Printed circuit board temperature:

Insert the printed circuit board temperature in the units as selected above.

Temperature offset OTP value:

This represents the value stored in the piccolo One-Time-Programmable (OTP) memory to calibrate the temperature sensor offset and would normally be read at the start of a routine running on a MCU. Refer to the TI documentation for further details.

Temperature slope OTP value:

This represents the value stored in the piccolo One-Time-Programmable (OTP) memory to calibrate the temperature sensor slope or gain and would normally be read at the start of a routine running on a MCU. Refer to the TI documentation for further details.

Use datasheet values:

Select this box if the OTP values above are to be ignored and the typical datasheet values for the piccolo internal temperature sensor are to determine its characteristic.

Include thermal time constant:

Select this box if the temperature sensor is to be modelled with a thermal time constant.

Thermal time constant to 90% (s):

This is the time to reach 90% of the expected output value.

Initial temperature (°C):

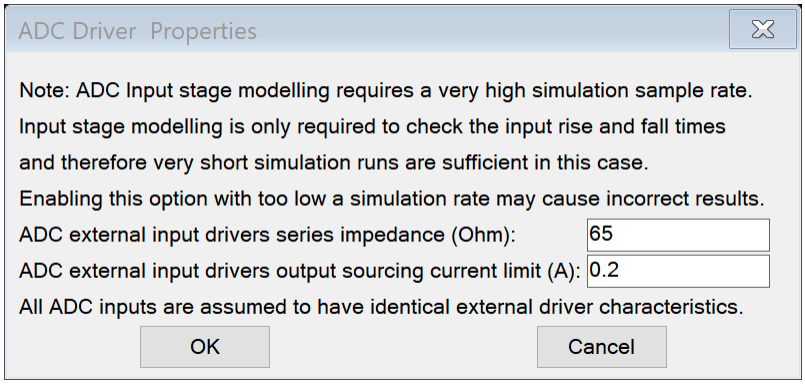
Enter the initial temperature in degrees Celsius.

ADC Offset Trim (LSBs):

Enter the value of any offset trim for the ADC in LSBs of the expected output value. Note that the value of this register is normally preset by TI and should only be varied in practise if recommended by TI. The effects of the offset can be simulated however in this emulator.

Include the RC parasitics of the ADC input stage:

Select this option if the RC parasitics of the ADC input sampler and ADC driver are to be included. Note that due to the very low value of the parasitic components, the simulation rate will need to be significantly higher in order to correctly simulate the input stage. For normal simulations this option is not necessary. It can however be used in very short simulations in order to simulate the ADC higher frequency input characteristics.



ADC external input drivers series impedance (Ohms):

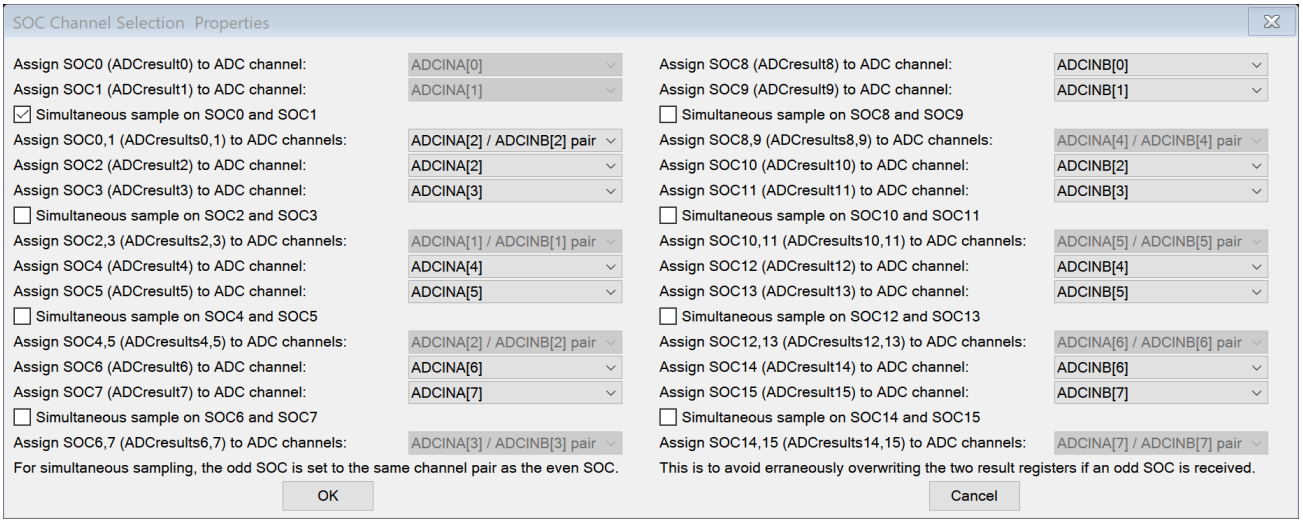
Enter the output impedance of the ADC input driver and / or any series impedance in the path of the ADC input.

ADC external input drivers series impedance (Ohms):

Enter the ADC input driver output source current limitation in amperes.

Note that all ADC channels are assumed to have identical driver characteristics, both internally and externally to the ADC.

SOC Configuration:



Assign SOCx (ADCRESULTx) to ADC channel:

Select the ADC input channel which is to be assigned to this even numbered SOC and to be loaded in the corresponding ADCRESULT register.

Assign SOCy (ADCRESULTy) to ADC channel:

Select the ADC input channel which is to be assigned to this odd numbered SOC and to be loaded in the corresponding ADCRESULT register.

Simultaneous sample on SOCx and SOCy:

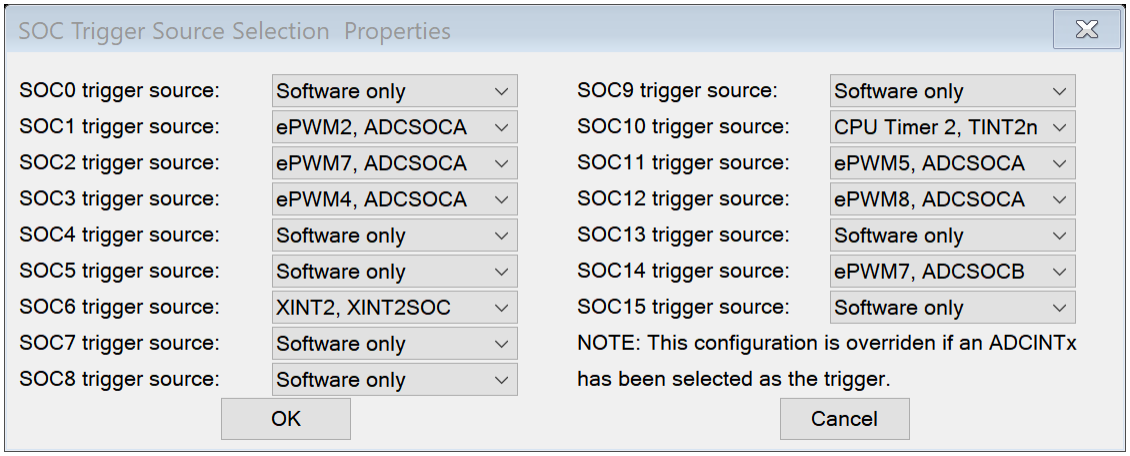
Select this option if the x (even) and y (consecutive, odd) pair are to be sampled together by the dual samplers A and B.

Assign SOCx,y (ADCRESULTx,y) to ADC channels:

Select the ADC input pair which are to be loaded in the x and y ADCRESULT registers. The selection will always be any ADCINA channel along with the corresponding ADCINB channel.

1. ADCINA[0] / ADCINB[0] pair
2. ADCINA[1] / ADCINB[1] pair
3. ADCINA[2] / ADCINB[2] pair
4. ADCINA[3] / ADCINB[3] pair
5. ADCINA[4] / ADCINB[4] pair
6. ADCINA[5] / ADCINB[5] pair
7. ADCINA[6] / ADCINB[6] pair
8. ADCINA[7] / ADCINB[7] pair

Note that for simultaneous sampling, the odd SOC is normally not used but will however be set to the same as the corresponding even SOC in order to avoid erroneously overwriting the result registers if triggered.

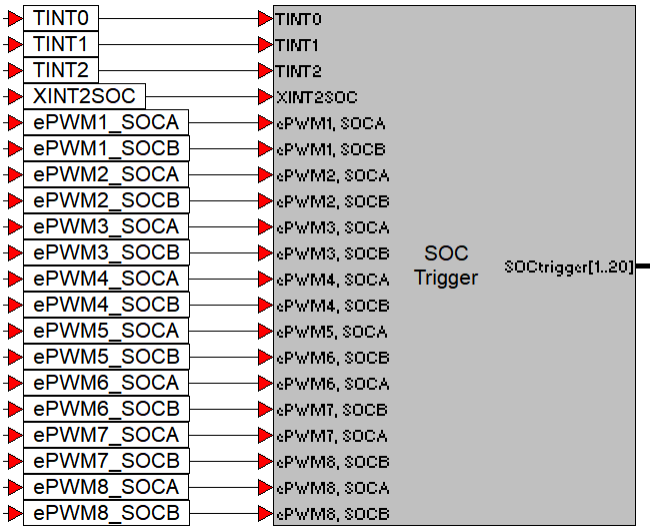


SOCx trigger source:

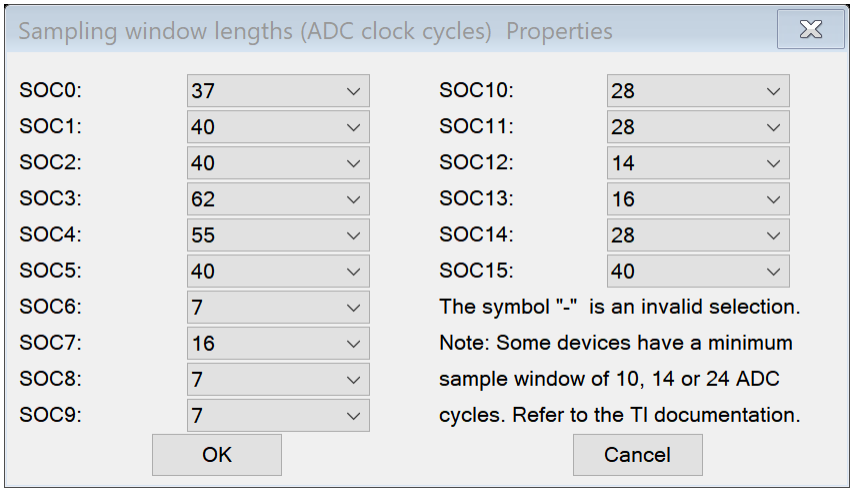
Select the source of the SOC trigger from the following:

0. Software only
1. CPU Timer 0, TINT0
2. CPU Timer 1, TINT1
3. CPU Timer 2, TINT2
4. XINT2, XINT2SOC
5. ePWM1, ADCSOCA
6. ePWM1, ADCSOCB
7. ePWM2, ADCSOCA
8. ePWM2, ADCSOCB
9. ePWM3, ADCSOCA
10. ePWM3, ADCSOCB
11. ePWM4, ADCSOCA
12. ePWM4, ADCSOCB
13. ePWM5, ADCSOCA
14. ePWM5, ADCSOCB
15. ePWM6, ADCSOCA
16. ePWM6, ADCSOCB
17. ePWM7, ADCSOCA
18. ePWM7,ADCSOCB
19. ePWM8, ADCSOCA
20. ePWM8, ADCSOCB

Note that this configuration will be ignored for any SOC if an ADCINTx has been selected as the trigger in the SOC trigger selection below.
For the purposes of this peripheral emulator, the triggers will be initiated if the SOCtrigger[1..20] input goes high (≥ 1). Each trigger is at the corresponding vector element as numbered above. The software trigger is not included at the input since it can only be performed by the microcontroller software.
The SOC input trigger block which can be connected to the SOCtrigger[1..20] input is as given below:



SOC sampling window lengths:



SOCx sampling window length:

Select the length of the ADC sampling window for each SOC in ADC clock cycles. The sampling length can range from 7 to 64 ADC clock cycles, though many of the selections in between are invalid as can be seen in the drop-down list in the emulator block.

Use highest priority sequencing mode:

Select this mode to set which SOC will have the highest priority

SOC priority number:

Select the SOC priority number. All SOCs less than the selected SOC will become high priority SOCs and will not be part of the round robin scheme.

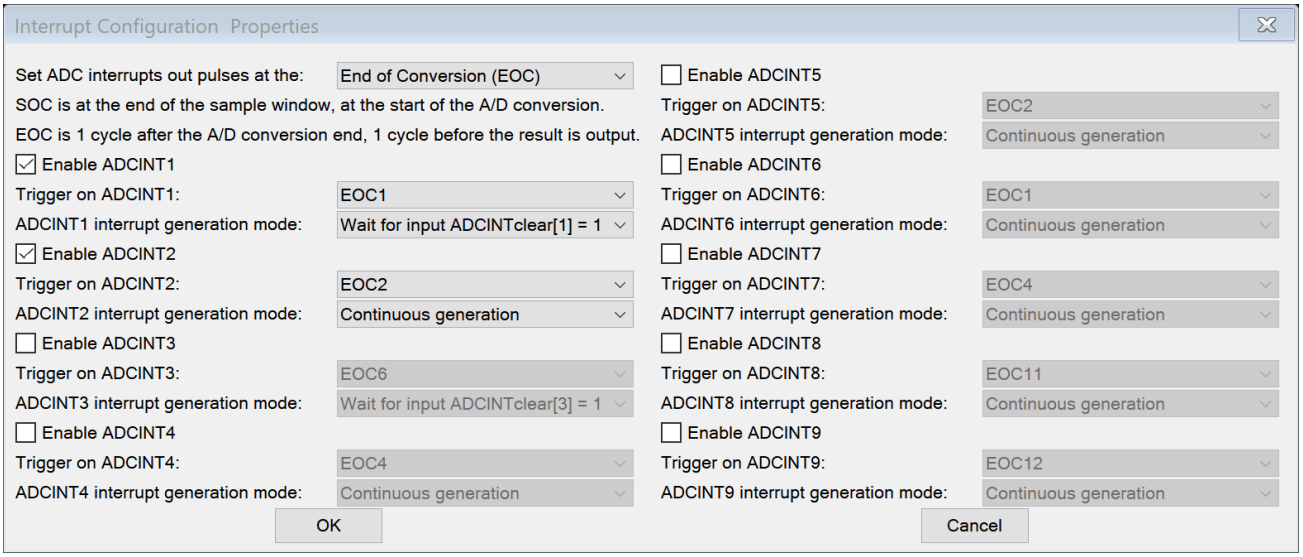
Disable overlap mode of S/H with sample conversion:

If this option is selected, the ADC sampling will not be performed while a conversion is in process. The operations will be performed sequentially.

Enable one-shot single conversion mode:

Select this option if one shot single conversion is to be performed on an SOC trigger.

Interrupt Configuration:



Set the ADC interrupts out pulses at the:

Select the point during the conversion of the ADC input at which the interrupts are to occur. SOC is the point at the end of the sample window and at the start of the conversion. EOC is the point one ADC clock cycle after the conversion end and one ADC clock cycle before the result is stored ion the ADCRESULT register.

Enable ADCINTx:

Select this to enable the ADC interrupt. Up to 10 ADC interrupts can be enabled.

Trigger on ADCINTx:

Select the SOC / EOC which will trigger the selected ADC interrupt from 0 to 15.

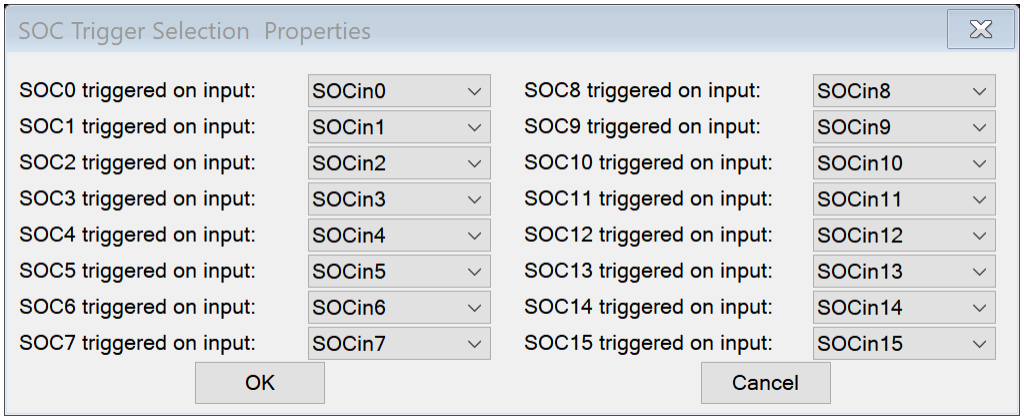
ADCINTx interrupt generation mode:

There are two choices here:

1. Wait for ADCINT clear = 1
2. Continuous conversion

In selection 1, the ADC interrupt will remain active and cannot be reactivated until it is cleared by the ADCINT clear input. In selection 2, the ADC interrupt will automatically be cleared and further interrupts can be generated.

SOC Trigger Selection:



SOCx triggered on input:

Select the trigger source for each SOC. If the SOCin is selected here, the trigger source is taken from the SOCx trigger source above. If an ADCINT is selected for any SOC here, this configuration will be dominant over the previous SOC trigger source selection above. The choices for each SOC are:

1. SOCinX
2. ADCINT1
3. ADCINT2

ADC format at output pin ADCresult[0..15]:

Select the output format of the ADC result.

Fixed-point radix (16-bit word):

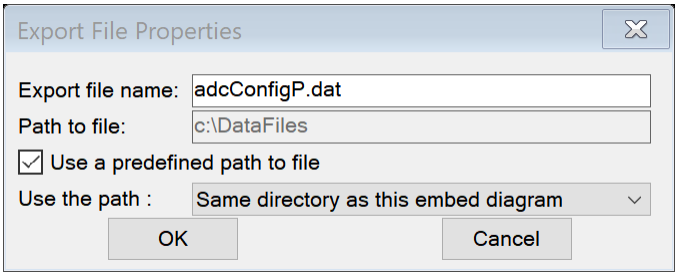
Select the fixed-point radix of the ADCresult output.

Send ADC results to the embedded analog inputs:

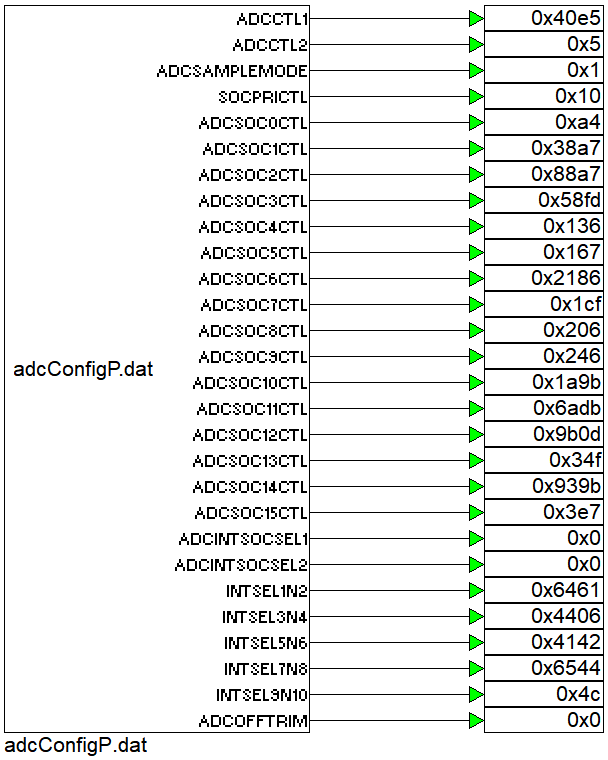
The ADC result outputs can be sent to the ADC sim blocks if this option is enabled.

Export the ADC configuration to file for code-generation:

Select this option to export the ADC configuration to a file. The file name and path needs to be specified as below and the file available at that path.

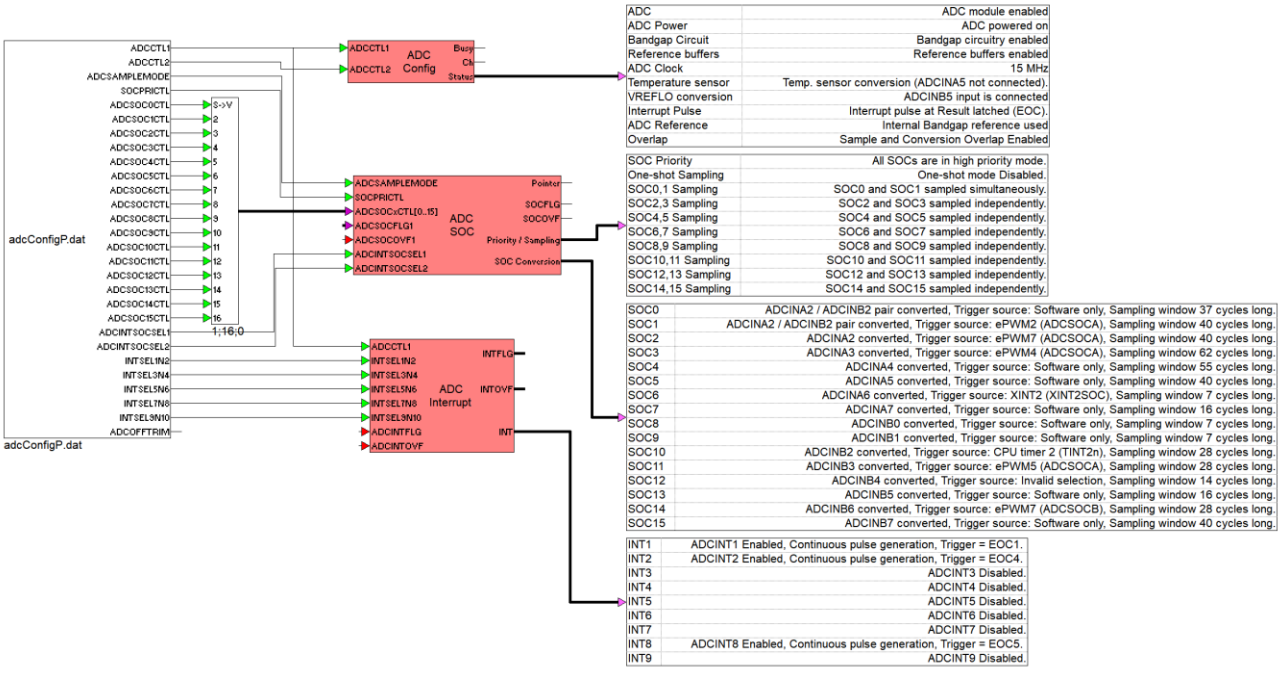


The file can be used in an ADC config block (code-gen section) to configure the ADC of the microcontroller identically to this MCU peripheral emulator block.
The configuration settings used in this emulator will be set in the export file (if enabled) which can be used in a diagram to completely configure the ADC peripheral.
The configuration settings can be viewed by placing a file import block in the diagram as follows:

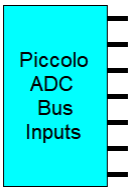


The outputs of the file import block are the register values of the ADC peripheral to be configured in the microcontroller.

The ADC Target diagram decoders in the debug section of DPD can be used to check the configuration before code-generation **and** after compiling while running on the microcontroller as below:

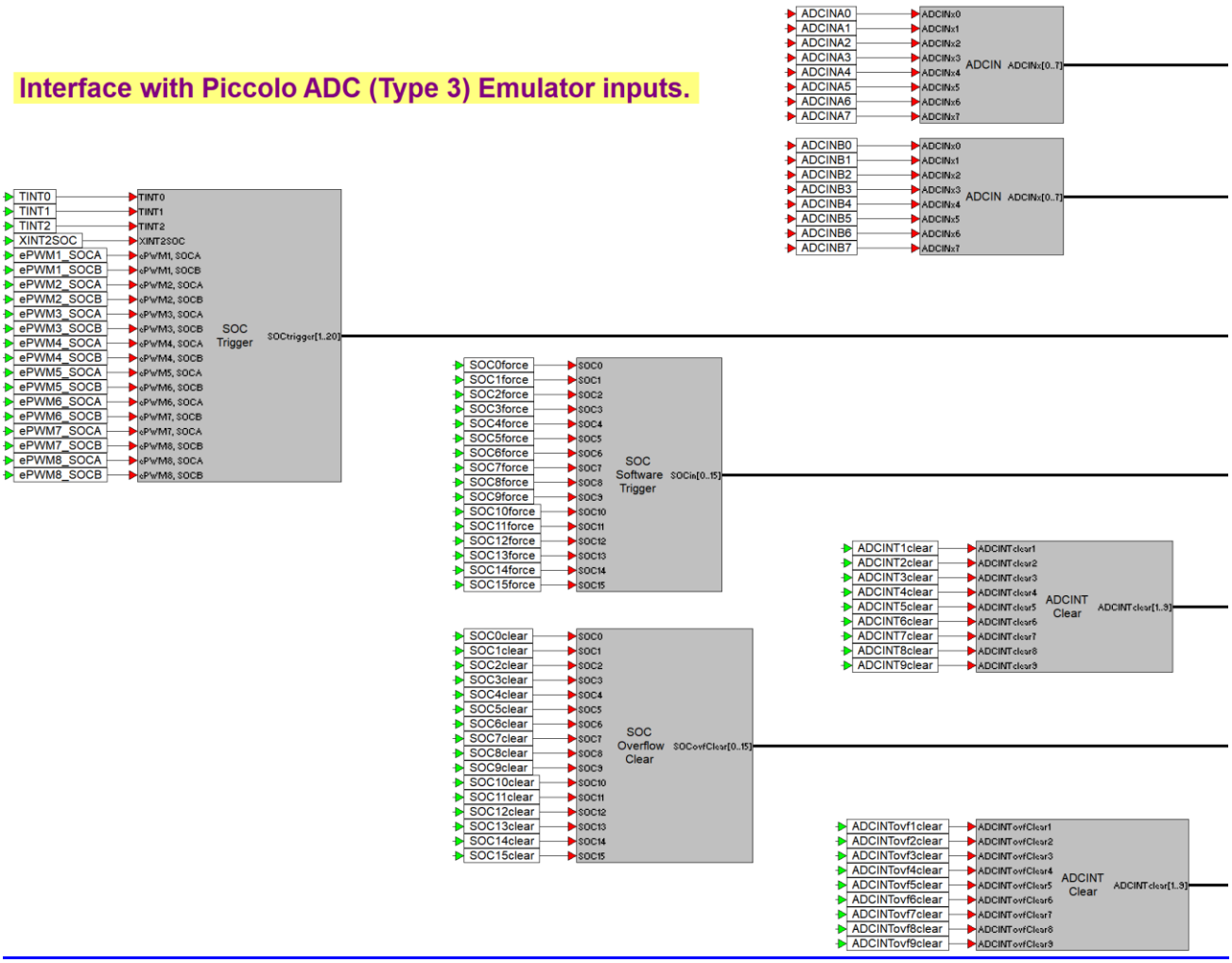


Contents - Simulation



ADC Bus Inputs (Piccolo)

This block is included to easily interface with the Piccolo ADC (type 3) emulator block. The required inputs to the emulator can be set internally in the block as shown below:





GPIO – General Purpose Input / Output

This block is based upon the TI C2000 GPIO / AIO.

Input Pins: **In** Input pin / output signal from a software routine.

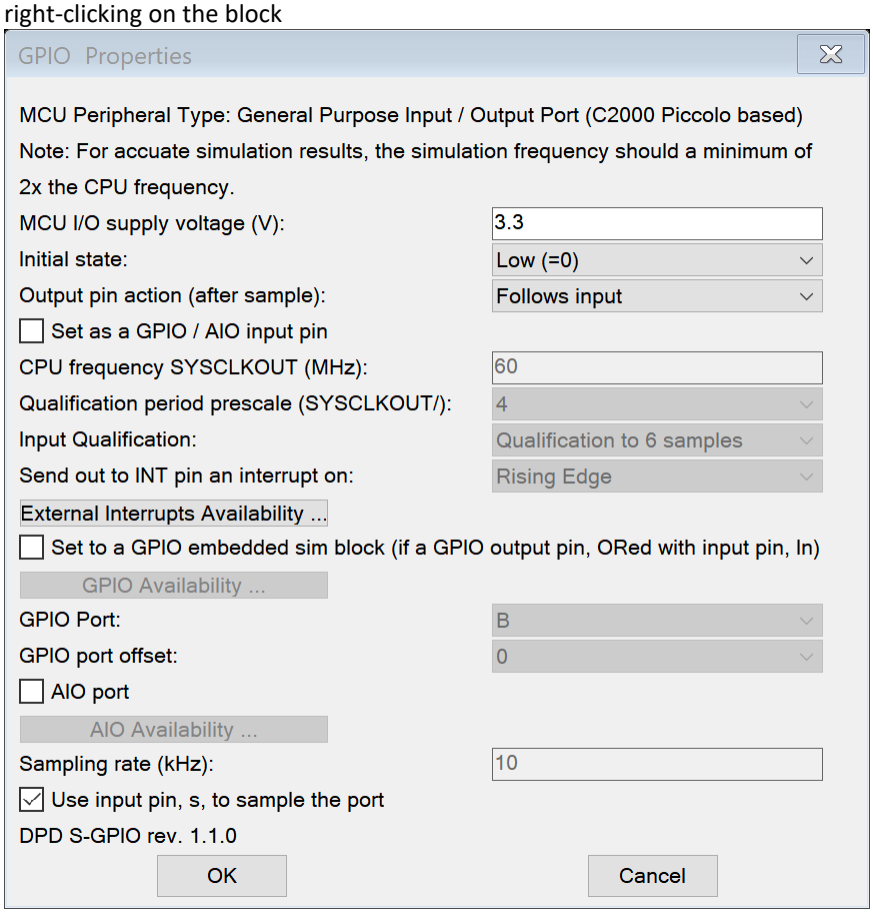
s Sample pin. This pin is only active if “Use input pin, s, to sample the port” is selected in the dialog.

Output Pins: **Out** Output pin / input signal to a software routine.

INT Interrupt signal out depending upon the action selected in the dialog. On an interrupt, this output will go high for one simulation time step.

Dialog properties:

The GPIO block properties menu is shown in the following box which appears when right-clicking on the block



Output pin action (after sample):

Enter the I/O supply voltage of the MCU (default is 3.3V).

Initial State:

The choices are either a low voltage or high voltage at the given supply voltage emulating the MCU GPIO pull-up on start-up.

Output pin action (after sample):

When set as an output pin, the input signal to the block can either be directly sent out or a high value on the input can cause the output to toggle its value.

Set as input pin:

When selected, the input qualification is activated (if not an AIO or JTAG port).

CPU frequency, SYSCLKOUT:

Enter the CPU frequency in MHz (for input qualification).

Qualification period pre-scale:

Select a value to pre-scale the counter for the input GPIO qualification.

Input qualification:

The amount of qualification (filter) can be configured here. The choices are:

1. Sync to SYSCLKOUT
2. Qualification to 3 samples
3. Qualification to 6 samples

Asynchronous is not applicable for a GPIO input and for peripherals inputs, this block is not required in that case; a direct Embed connection is sufficient.

Send out to INT pin an interrupt on:

The choices here, to enable a one time-step pulse simulating an interrupt trigger at the output pin INT, are:

1. Disabled
2. Falling edge
3. Rising edge
4. Falling and rising edge

Interrupt Availability:

External Interrupts Availability Properties

Device	Package	Interrupts	Can be mapped on GPIOs
F2802x	38 pin	3	0 -7, 12, 16 -19, 28, 29 (Port A)
F2802x	48 pin	3	0 -7, 12, 16 -19, 28, 29 (Port A)
F2803x	56 pin	3	0 - 7, 12, 16 - 23, 28 - 31 (Port A)
F2803x	64 pin	3	0 - 12, 16 - 24, 28 - 31 (Port A)
F2803x	80 pin	3	GPIO0 - GPIO31 (Port A)
F2805x	80 pin	3	GPIO0 - GPIO31 (Port A)
F2806x	80 pin	3	GPIO0 - GPIO31 (Port A)
F2806x	100 pin	3	GPIO0 - GPIO31 (Port A)
F280x	100 pin	3	GPIO0 - GPIO31 (Port A)
F2833x	ALL	8	GPIO0 - GPIO63 (Ports A and B)
C2834x	ALL	8	GPIO0 - GPIO63 (Ports A and B)
F2807x	100 pin	5	ALL: 2 - 4,10 - 21, 41 - 43, 58 - 66, 69 - 73, 78, 85 - 87, 89 - 92, 99
F2807x	176 pin	5	ALL: 0 - 94, 99, 133
F2837x	100 pin	5	ALL: 2 - 4,10 - 21, 41 - 43, 58 - 66, 69 - 73, 78, 85 - 87, 89 - 92, 99
F2837x	176 pin	5	ALL: 0 - 94, 99, 133
F2837x	337 pin	5	ALL: 0 - 168
F28004x	56 pin	5	ALL: 0 - 9, 11, 12, 13, 16, 17, 18, 22, 23, 24, 28, 29, 32, 33, 35, 37
F28004x	64 pin (PM)	5	ALL: 0 - 13, 16, 17, 18, 22, 23, 24, 28, 29, 32, 33, 35, 37
F28004x	64 pin (PMQ)	5	ALL: 0 - 11, 16, 17, 18, 22, 23, 24, 28, 29, 32, 33, 35, 37
F28004x	100 pin	5	ALL: 0 - 18, 22 - 35, 37, 39, 40, 56 - 59
F28M35 (28x)	ALL	3	GPIO0 - GPIO38, GPIO40 - GPIO63 (Ports A and B)
F28M36 (28x)	ALL	3	GPIO0 - GPIO63 (Ports A and B)

OK Cancel

Set to an embedded GPIO sim block:

Select this if the emulator will be connected to an embedded GPIO sim block output (if set as an output) or sim block input if set as an input.

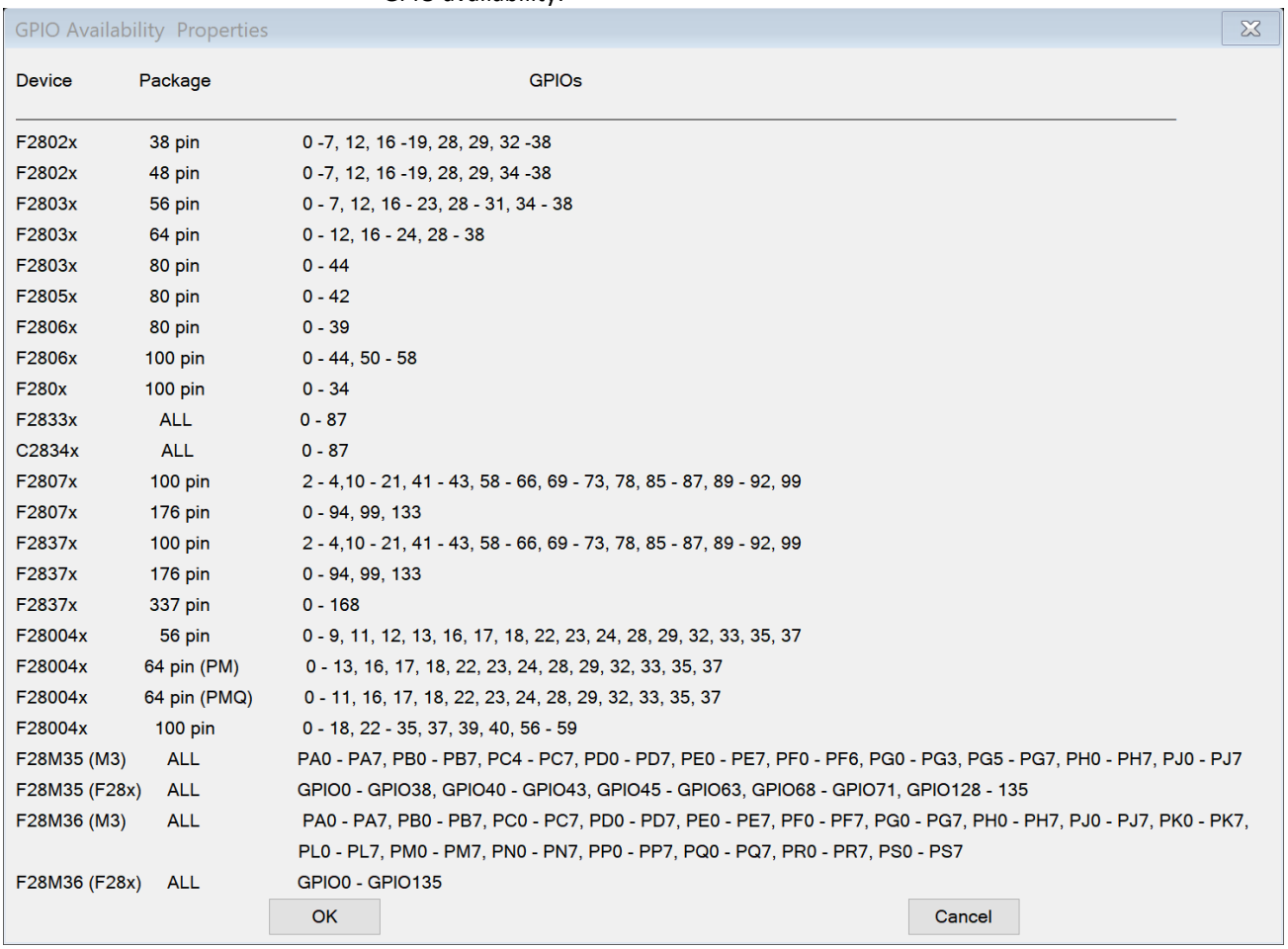
GPIO port:

Choose the GPIO port, A or B.

GPIO port offset:

Choose the GPIO channel from 0 to 31.

GPIO availability:



AIO port:

Select this option is the port is an AIO port. The input will be synchronized with SYSCLKOUT without qualification.

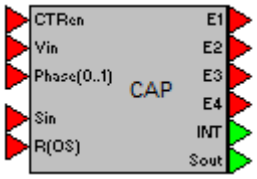
Sampling rate (kHz):

The GPIO port (either input or output) will be sampled at this rate. Enter the value of the sampling rate where the port will be placed in a code-generable diagram.

Use input pin, s, to sample the port:

Select this option if the port is to be sampled by an external signal. In this case, the precise moment of the port sampling instant can be modelled.

[Contents - Simulation]



Event Capture (CAP)

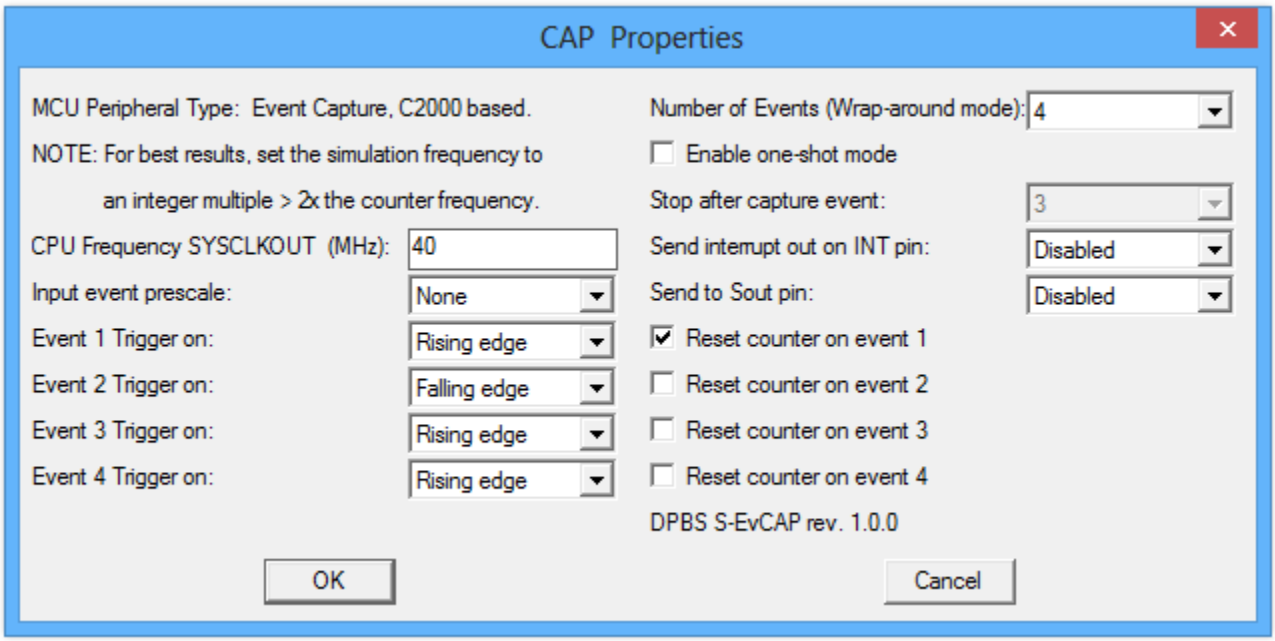
This block is based upon the TI C2000 eCAP peripheral.

Input Pins:

	CTRen	Counter enable pin; if this pin goes low, the counter will be frozen at the current value.
	Vin	Input signal to be captured.
	Phase(0..1)	Phase value of the 32-bit counter scaled from 0 to 1. This value will be set if a sync signal is present at the Sin pin.
	Sin	Sync input signal. This pin can be used to synchronize several CAP block timers to synchronise the CAP timer with a PWM block.
	R	Input reset applicable for one-shot mode.
Output Pins:	**E1**	Counter value on Event 1
	E2	Counter value on Event 2
	E3	Counter value on Event 3
	E4	Counter value on Event 4
	INT	Interrupt signal out depending upon the event selection in the dialog. On an interrupt, this output will go high for one simulation time step.
	Sout	Sync signal output pin to be connected to other CAP blocks.

Dialog properties:

The CAP block properties menu is shown in the following box which appears when right-clicking on the block



CPU frequency SYSCLKOUT:

Enter the value of the 32-bit counter frequency. The higher the frequency, the more accurate the result however the smaller the simulation time step required. The value is typically the MCU rate, however lower values can be applied in order to speed up the simulation.

Input event pre-scale:

The input signal can be pre-scaled or rather, the frequency of the input signal is frequency divided.

Event x Trigger on:

Each event can be set up to trigger either on the rising or the falling edge.

Number of events:

This is applicable for wrap-around mode. Select the maximum number of events required. After the specified number of events, the captures will “wrap-around” to the first event and repeat.

Enable one-shot mode:

Check this checkbox if one-shot mode is required. In this mode the captures will stop after the specified event. It can be reset using the R(OS) input pin.

Stop after capture event:

Select the event on which the captures should stop (values frozen).

Send out to INT pin an interrupt on:

Send a one simulation-time-step, active-high output pulse to the INT pin. The choices here are:

1. Disabled
2. Event 1
3. Event 2
4. Event 3
5. Event 4
6. Counter overflow

Send to Sout pin:

Send an one simulation-time-step, active-high output pulse to the Sout pin. The choices here are:

1. Disabled
2. Sync In

Reset counter on event x:

When selected, the counter will be reset on this event. Multiple events can be selected for reset.

Contents - Simulation



Analog comparator (MCU)

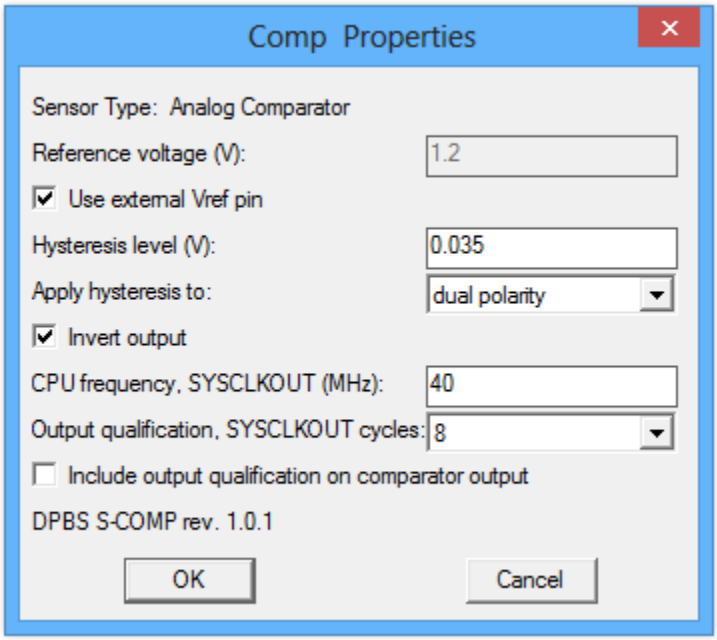
The analog comparator can be used in a simulation as a typical analog comparator or as an embedded comparator found in a MCU such as that of the TI piccolo MCU.

Input Pins: **Vin(+)** Input voltage (V) – positive input pin.

	Vref(-)	Reference voltage (V) – negative input pin (only active if the external reference is selected).
Output pins:	**Vo**	Output = 1 if Vin > Vref and hysteresis = none. = 0 if Vin < Vref and hysteresis = none. If hysteresis is defined then the output will also depend upon this value and its polarity.
	RR	Reset Ramp. This pin is always subject to the selected qualification and is normally used to reset the ramp generator back to its maximum value after a comparator output change.

Dialog properties:

The Comparator block properties menu is shown in the following box which appears when right-clicking on the block



Reference voltage:

Enter the value of the voltage, in Volts, at the reference pin.

Use external reference pin:

If checked, the reference voltage above will be ignored and the input pin Vref(+) will be taken as the reference voltage.

Hysteresis level:

Enter the value of the hysteresis in Volts. For the C2000 piccolo comparators this is typically 35mV.

Apply hysteresis to:

An hysteresis voltage can be applied according to the following selection:

1. None
2. output H -> L transition only.
3. output L -> H transition only.
4. Dual polarity.

Note that this selection varies from the C2000 peripheral where in that case the hysteresis is fixed in hardware.

Invert output:

The output will be inverted when this box is checked.

CPU frequency, SYSCLKOUT:

Enter the frequency of the CPU clocking.

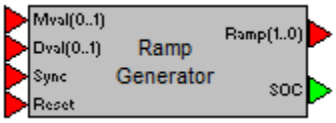
Output qualification, SYSCLKOUT cycles:

Enter the number of CPU clock cycles that will determine the duration of the filtering of the comparator trip output. Note that this filter will always be active on the comparator reset ramp (RR) output.

Include qualification on comparator output:

The output qualification will be included on the comparator output when this box is checked.

Contents - Simulation



Ramp Generator

The ramp generator block emulates the ramp generator in the comparator-DAC block of the TI C2000.

Input Pins: **Mval(0..1)** This pin sets the maximum value or reset value of the ramp in 10 bit resolution, scaled from 0 to 1.

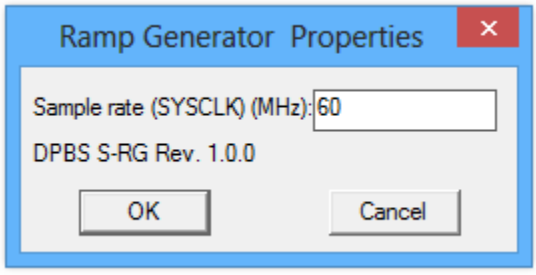
Dval(0..1) This pin sets the decrement value of the ramp in 10 bit resolution, scaled from 0 to 1.

Sync Input sync pin to synchronise the ramp with a PWM output – connect from a Dual PWM sync output pin.

Reset A reset input to reset the ramp back to its maximum value (Mval).

Output pins: **Ramp(1..0)** The output ramp.

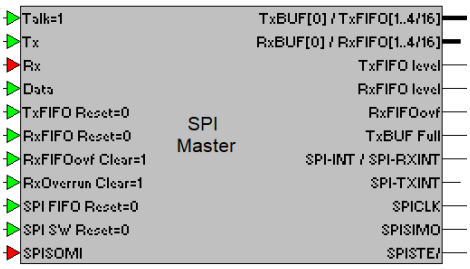
SOC A start of conversion pulse which can be connected to the SOC input of a DAC block.



Sample rate (SYSCLKOUT):

Set the sample rate of the ramp generator at the CPU frequency. The ramp is decremented according to the most significant 10 bits of a 16 bit counter and is therefore decremented at a rate of SYSCLKOUT/64.

Contents - Simulation



SPI Master

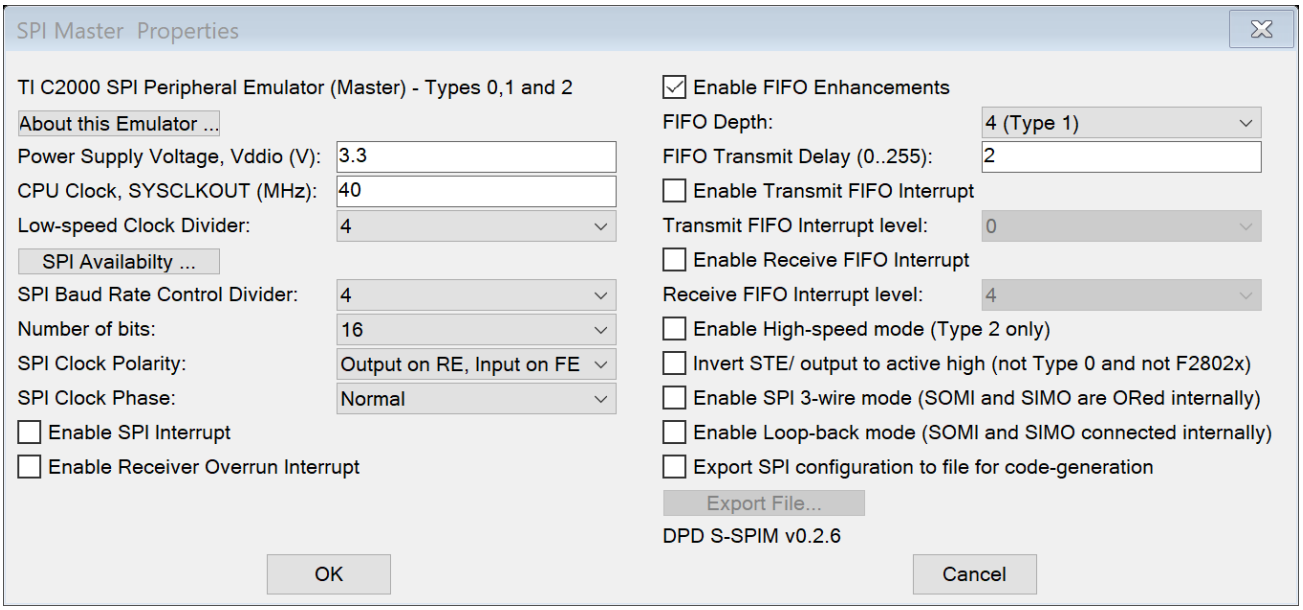
This block is based upon the TI C2000 SPI module and emulates the SPI peripheral in the master mode.

This emulator is currently in a preview status and will be improved upon in later updates of DPD.

Input Pins:	**Talk=1**	The talk input acts as an enable input to the peripheral.
	Tx	The transmit input. This is an input to be connected to software running in a diagram together with this emulator.
	Rx	The receive input. This is an input to be connected to software running in a diagram together with this emulator.
	Data	Data input pin. This is an input to be connected to software running in a diagram together with this emulator.
	TxFIFO Reset=0	Input pin to reset the transmit FIFO pointer to zero.
	RxFIFO Reset=0	Input pin to reset the receive FIFO pointer to zero.
	RxFIFOovf Clear=1	Input pin to clear the receive FIFO overflow flag.
	RxOverrun Clear=1	Input pin to clear the receive FIFO overrun flag.
	SPI FIFO Reset=0	Input pin to reset the SPI FIFO.
	SPI SW Reset=0	Input pin for a software reset on the SPI module.
	SPISOMI	Input pin emulating the hardware master input data.
Output pins:	**TxBUF[0]/TxFIFO[1..4/16]**	The transmit FIFO buffer output. This is either a single-element buffer output when the FIFO is not enabled or the buffer + transmit FIFO when the FIFO is enabled of either a depth of 4 or 16, depending upon the type of SPI peripheral being emulated.
	RxBUF[0]/RxFIFO[1..4/16]	The receive FIFO buffer output. This is either a single-element buffer output when the FIFO is not enabled or the buffer + transmit FIFO when the FIFO is enabled of either a depth of 4 or 16, depending upon the type of SPI peripheral being emulated.
	TxFIFO Level	Output giving the current pointer value of the transmit FIFO.
	RxFIFO Level	Output giving the current pointer value of the receive FIFO.
	RxFIFO ovf	Output = 1 when the receive buffer is in overflow (another word has arrived before the buffer could be read out).
	TxBUF Full	Output = 1 when the transmit buffer is full (a word is ready to be transmitted).
	SPI-INT/SPI-RxINT	Output SPI interrupt or the receive FIFO interrupt pin.
	SPI-TxINT	Output transmit FIFO interrupt pin.
	SPICLK	Output hardware pin for the SPI clock.
	SPISIMO	Output hardware pin for the master data output.
	SPISTE/	Output hardware pin for the Slave Transmit Enable.

Dialog properties:

The SPI Master emulator block properties menu is shown in the following box which appears when right-clicking on the block:



Power supply voltage, Vddio (V):

Enter the value of the power supply voltage, in Volts of the I/O of the microcontroller.

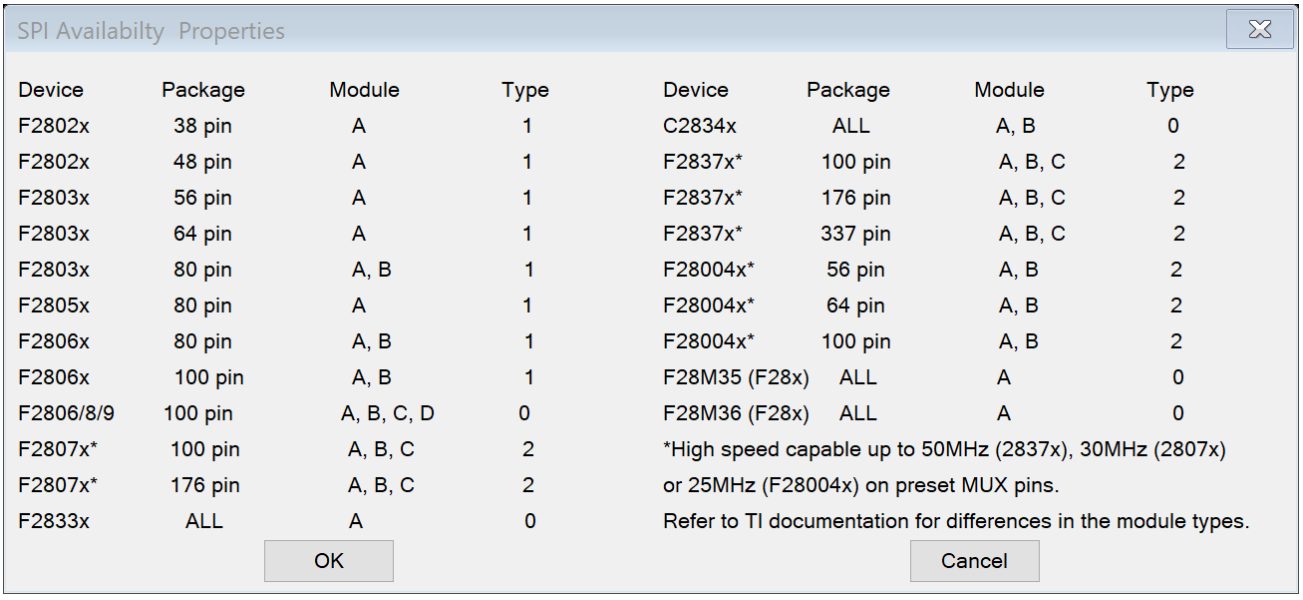
CPU clock, SYSCLKOUT (MHz):

Enter the CPU clock frequency in MHz.

Low speed clock divider:

Select the divider on the CPU clock above to generate the low speed clock (LSP) on which the SPI peripheral operates.

SPI availability:



SPI Baud rate control divider:

Select the LSP clock divider in order to generate the SPI baud rate clock. The divider can be from 4 to 128.

Number of bits:

Select the number of bits for the SPI word from 1 to 16.

SPI Clock Polarity:

Select the SPI clock polarity. The choices are:

1. Output on rising edge, data latched on falling edge (clock is normally low)
2. Output on falling edge, data latched on rising edge (clock is normally high)

SPI Phase:

Select the phase of the SPI clock. The choices are:

1. Normal
2. Half-cycle delayed.

Enable SPI Interrupt:

Select this option to enable the SPI interrupt.

Enable receiver overrun interrupt:

Select this option to enable the SPI Overrun interrupt.

Enable FIFO Enhancements:

Select to enable the transmit and receive FIFOs.

FIFO depth:

Select the depth of the FIFO. The choices are:

1. 4 for the type 1 SPI module (F2802x, F2803x, F2805x, F2806x)
2. 16 for the types 0 and 2 SPI modules (F280x, F28x7x, F28004x, Concerto)

FIFO Transmit delay (0..255):

Select the delay between the transmission of words from the FIFO. The delay is in SPI baud rate clock cycles.

Enable Transmit FIFO Interrupt:

Select to enable the transmit FIFO interrupt.

Transmit FIFO Interrupt level:

Select the FIFO level at which the interrupt will be generated.

Enable Receive FIFO Interrupt:

Select to enable the receive FIFO interrupt.

Receive FIFO Interrupt level:

Select the FIFO level at which the interrupt will be generated.

Enable High-speed mode:

This option is available for F28x7x devices which can operate up to 50MHz and require a specific MUX configuration.

Invert STE/ output to active high:

Select this option to invert the slave transmit enable output so that it will be active high. This option is not available on SPI modules of type 0 and also F2802x devices.

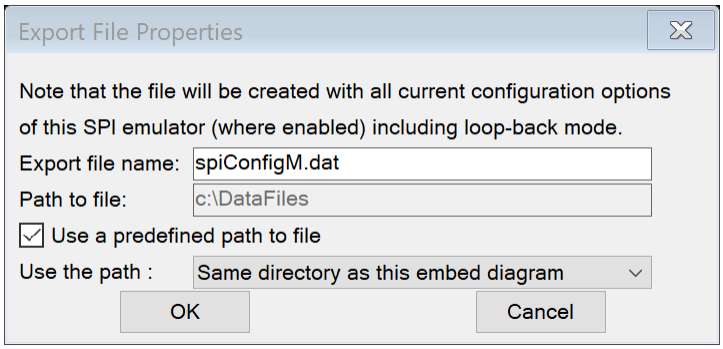
Enable SPI 3-wire mode:

Select this option to enable 3-wire SPI mode. The SOMI and SIMO pins will be ORed internally in the emulator.

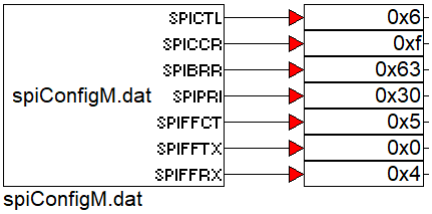
Enable loop-back mode:

Select this option to enable SPI loop-back mode. The SOMI and SIMO pins will be connected internally in the emulator.

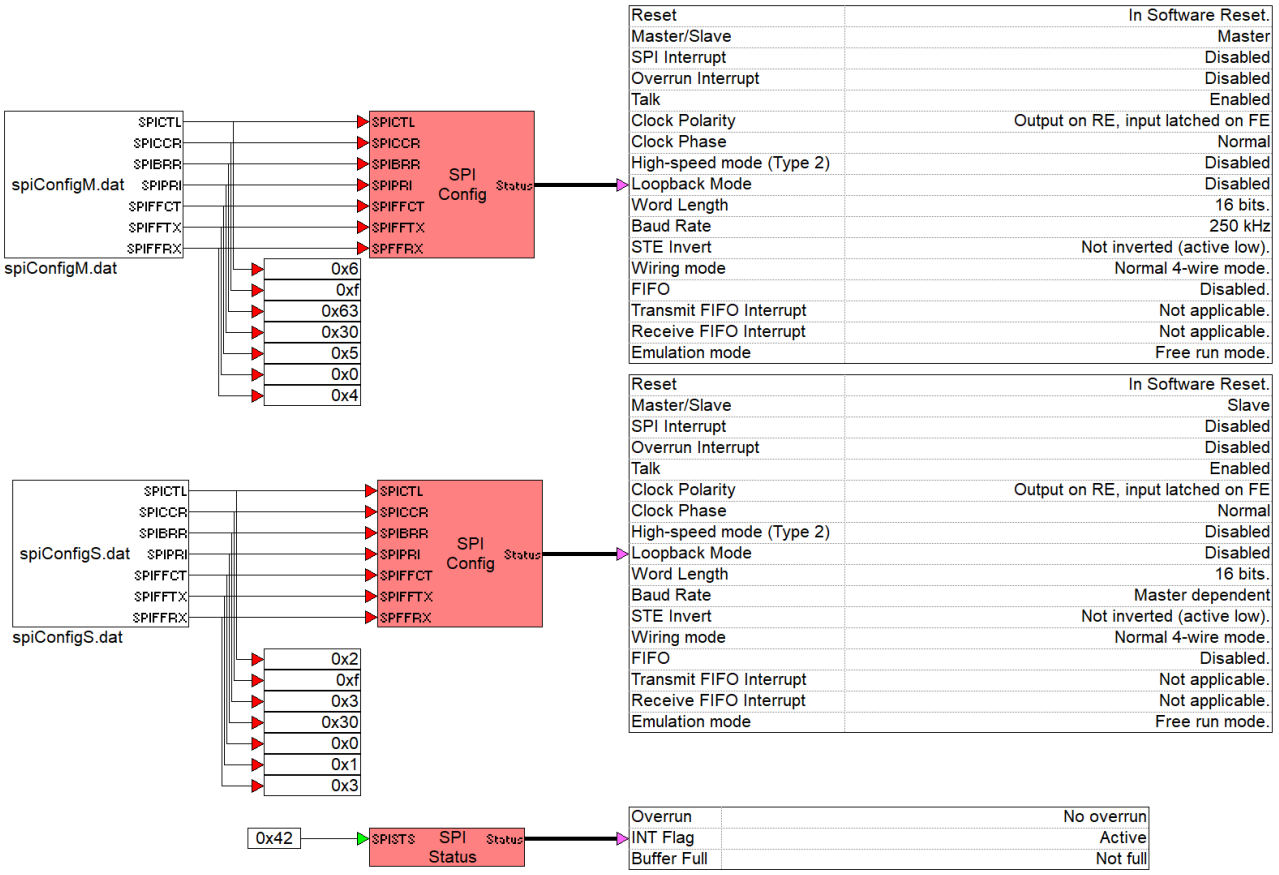
Export SPI configuration to file for code-generation:



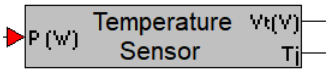
The file can be used in SPI config block (code-gen section) to configure the SPI of the microcontroller identically to this MCU peripheral emulator block.
The configuration settings used in this emulator will be set in the export file (if enabled) which can be used in a diagram to completely configure the SPI peripheral. Note that the low speed clock will not be set in the configuration file as it is not a part of the SPI peripheral. For the correct SPI baud rate, the LSP clock must be set to in the code-gen diagram to the same divider as in this emulator.
The configuration settings can be viewed by placing a file import block in the diagram as follows:



The outputs of the file import block are the register values of the SPI peripheral to be configured in the microcontroller.
The SPI Target diagram decoders in the debug section of DPD can be used to check the configuration before code-generation **and** after compiling while running on the microcontroller as below:



Contents - Simulation



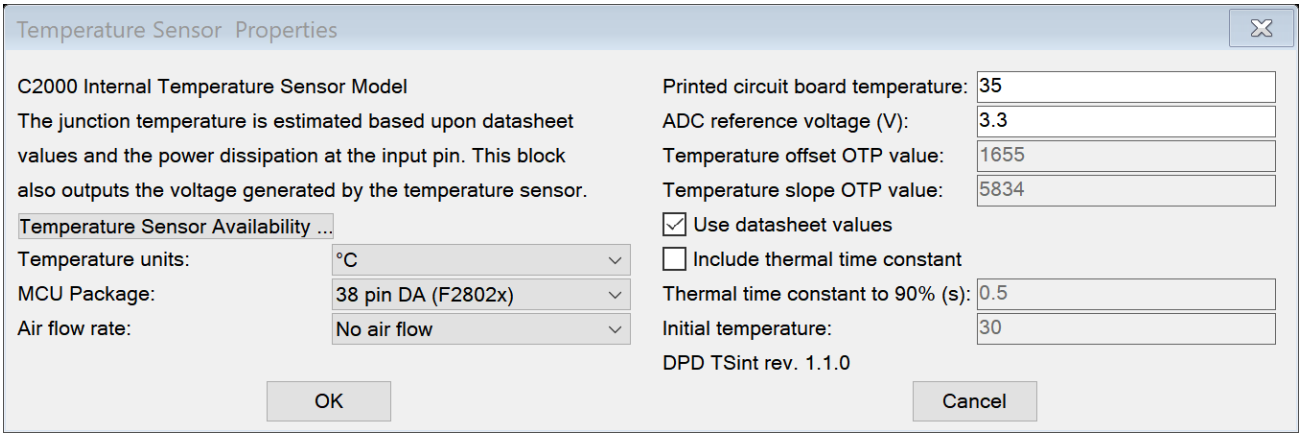
Temperature Sensor

The temperature sensor block emulates the internal temperature sensor of the TI C2000 piccolo series of MCUs.

Input Pins: **P (W)** The power dissipation input in Watts..

Output pins: **Vt (V)** The temperature sensor output in volts.

Tj The junction temperature of the chip in the selected temperature units.



Temperature units:

The choices here are:

4. °C
5. °F
6. K

The emulator will calculate all temperature values in the defined unit.

MCU package:

Select the MCU package of the device used.

Air flow rate:

Select the airflow rate around the MCU chip.

Printed circuit board temperature:

Insert the printed circuit board temperature in the units as selected above.

ADC reference voltage:

The ADC reference voltage should be entered here (default is 3.3V). This may vary if an external reference is used.

Temperature offset OTP value:

This represents the value stored in the piccolo One-Time-Programmable (OTP) memory to calibrate the temperature sensor offset and would normally be read at the start of a routine running on a MCU. Refer to the TI documentation for further details.

Temperature slope OTP value:

This represents the value stored in the piccolo One-Time-Programmable (OTP) memory to calibrate the temperature sensor slope or gain and would normally be read at the start of a routine running on a MCU. Refer to the TI documentation for further details.

Use datasheet values:

Select this box if the OTP values above are to be ignored and the typical datasheet values for the piccolo internal temperature sensor are to determine its characteristic.

Include thermal time constant:

Select this box if the temperature sensor is to be modelled with a thermal time constant.

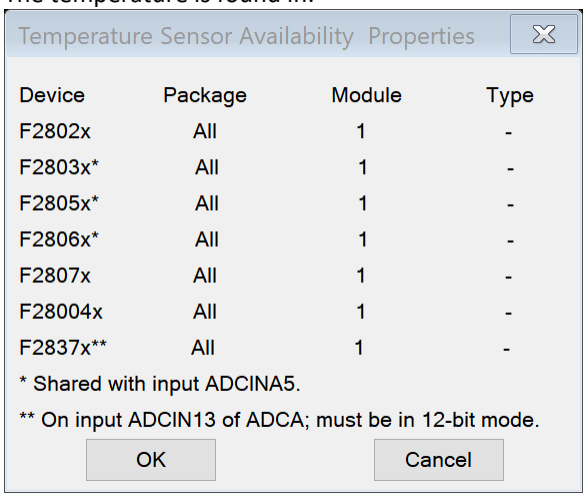
Thermal time constant to 90% (s):

This is the time to reach 90% of the expected output value.

Initial temperature (°C):

Enter the initial temperature in degrees Centigrade.

The temperature is found in:



Contents - Simulation

Loads

The blocks in the loads section of the digital power block set are generally designed to be connected to the load% input pin of the power converter blocks.



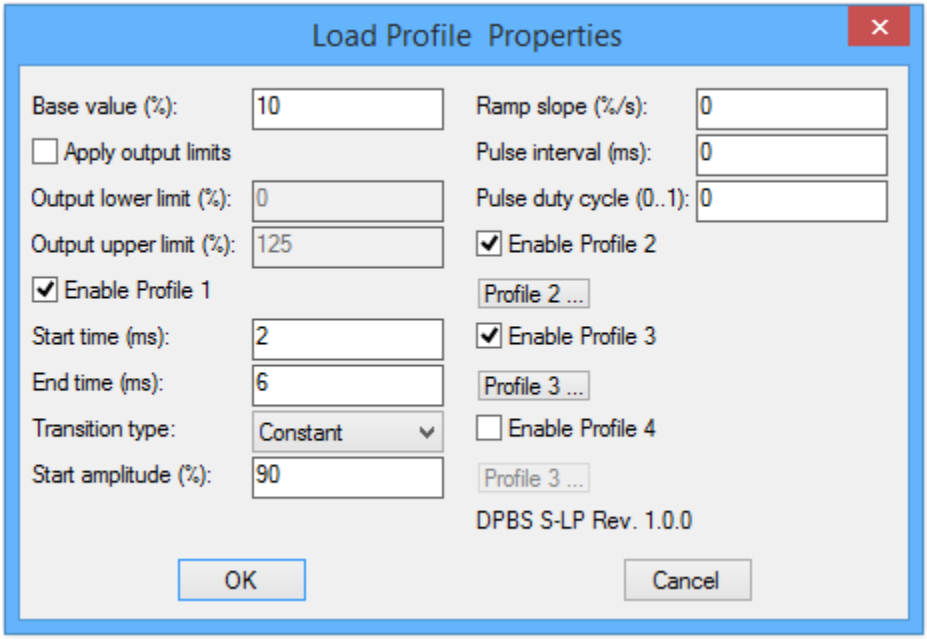
Load profile

Output Pins: **%**

A percentage output according to the internally set profile.

Dialog properties:

The load profile block properties menu is shown in the following box which appears when right-clicking on the block.



Base value:

Enter a value (%) which will remain constant during the simulation.

Apply output limits:

Check this box to apply limits on the output value.

Output lower and upper limit:

Enter the required limiting values in %.

Enable Profile 1:

Check each profile to enable a different time slot and / or transition.

Start time:

Enter the start time of each profile in milliseconds.

End time:

Enter the stop time of each profile in milliseconds.

Transition type:

There are four choices here:

1. Constant
2. Ramp up
3. Ramp down
4. Pulses

Start amplitude:

The amplitude in % at the start of the profile.

Ramp slope:

When a ramp is selected as a transition, enter the slope of the ramp in %/s.

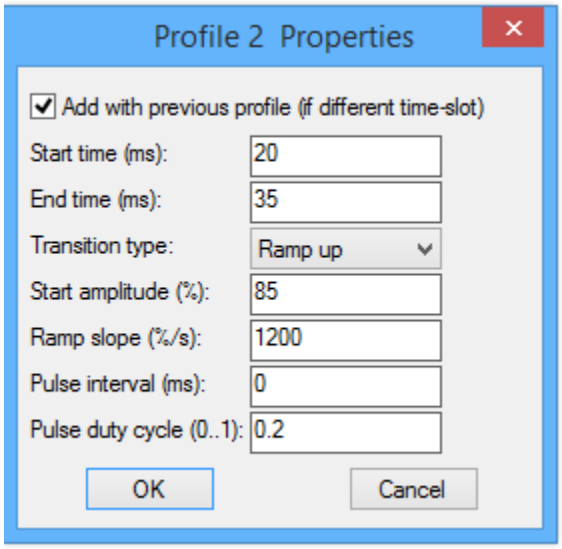
Pulse interval:

When pulses are selected, enter the pulse interval (period) in milliseconds.

Pulse duty cycle:

Enter the duty cycle of the pulses (when selected).

Enable Profiles 2 to 4:



Add with previous profile:

If the profile has an overlapping time slot, it will automatically be added to the other profile(s) with that time slot. If the time slots are not overlapping, the corresponding profile can be summed with the previous profile by checking this box.

Contents - Simulation



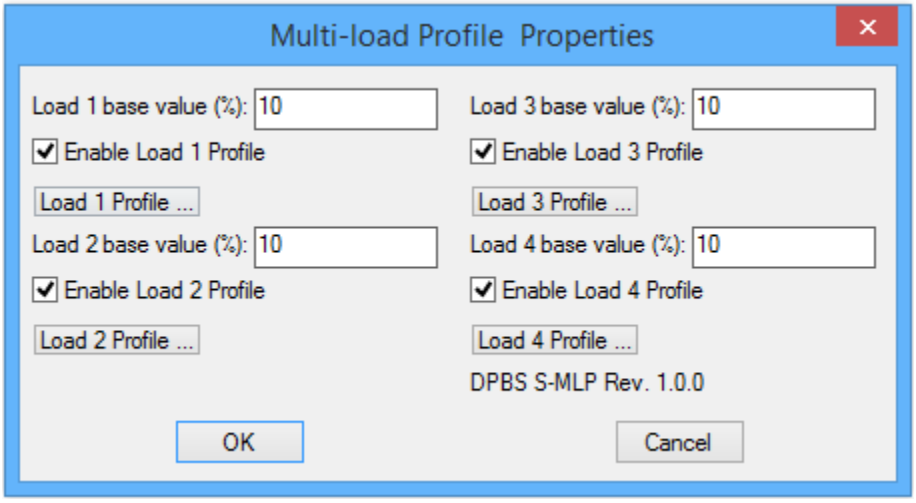
Multi-load Profile

This block can be connected to the Load% input pin of the power converters for load profiles of converters with up to 4 different outputs.

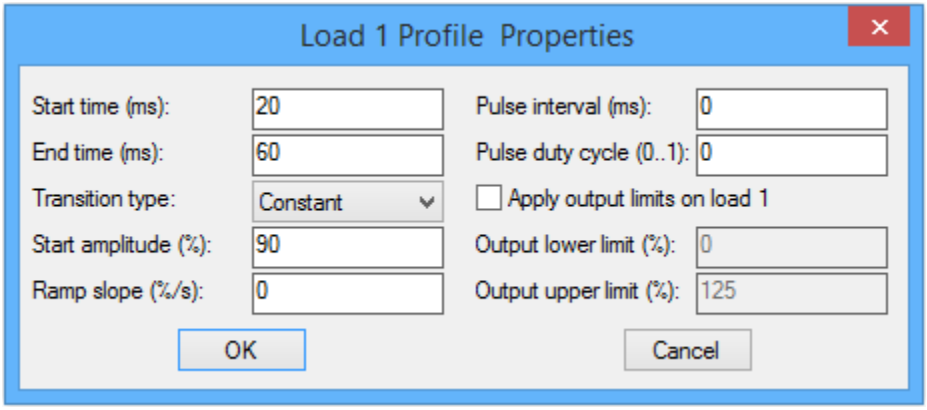
Output Pin: **%[1..4]** A percentage output according to the internally set profiles, vector (rows = 1, columns = 4).

Dialog properties:

The multi-load profile block properties menu is shown in the following box which appears when right-clicking on the block.



The fields are the same as for the load profile block accept that only one profile can be applied per converter output.



Contents - Simulation



Constant current load

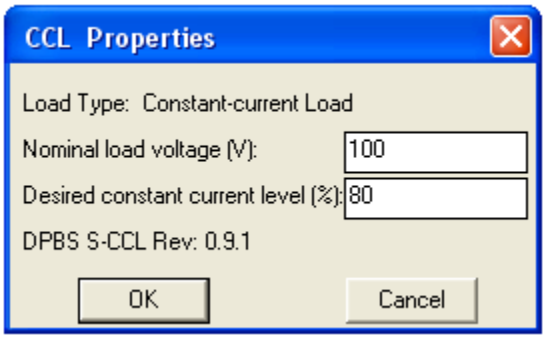
This block can be connected to the Load% input pin of the power converters for regulation of constant output current (up to the limits of the power converter).

Input Pins: **Vo** Connect to the voltage (V) seen by the load.

Output Pins: **%** A percentage output according to the set current level and the block input voltage. Connect to the Load% input pin of the power converters for constant current loading.

Dialog properties:

The constant current load block properties menu is shown in the following box which appears when right-clicking on the block.



Nominal load voltage:

Enter the nominal load voltage in Volts. This will be confronted with the Vrms input voltage.

Desired constant current level:

Enter the desired constant current level in %.



Constant power load

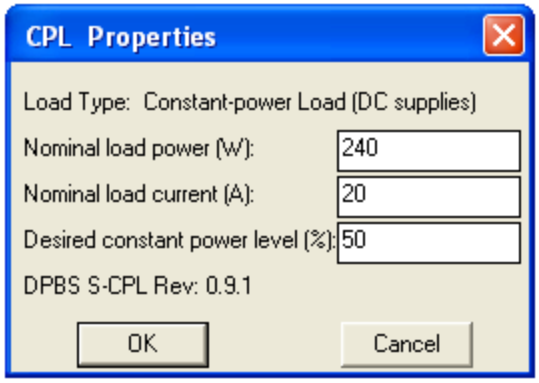
This block can be connected to the Load% input pin of the power converters for regulation of constant power (up to the limits of the power converter).

Input Pin: **Vo** Connect to the voltage (V) seen by the load.

Output Pin: **%** A percentage output according to the block input voltage and the constants entered in the dialog. Connect to the Load% input pin of the power converters for constant power loading.

Dialog properties:

The constant power load block properties menu is shown in the following box which appears when right-clicking on the block.



Nominal load power:

Enter the nominal power of the load in Watts.

Nominal load current:

Enter the nominal load current in Amperes.

Desired constant power level:

Enter the desired load power level in %.

Contents - Simulation



RL load

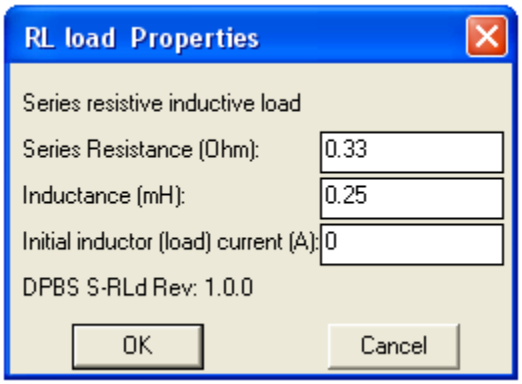
This block can be connected to the %Load/Io input pin of the power converters to simulate a power converter with a series resistive-inductive load.

Input Pins: **Vo** Connect from the converter output voltage (V) seen by the load.

Output Pins: **Io** The load current according to the block input voltage, the resistance and inductance values entered. Connect to the %Load/Io input pin of the power converters.

Dialog properties:

The RL load block properties menu is shown in the following box which appears when right-clicking on the block.



Series resistance:

Enter the series load resistance in Ohms.

Series inductance:

Enter the series inductance in milli-Henries.

Initial inductor (load) current:

Enter the initial load current flowing through the inductive load at the start of a simulation in amperes.

Contents - Simulation



Resistive load with line impedance to load

This block can be connected to the %Load/Io input pin of the power converters to simulate a power converter with a remote load where the load is located some distance from the converter and the load line is modelled as a series inductance and resistance .

Input Pins: **Vo** Connect the voltage (V) into the load at this pin.

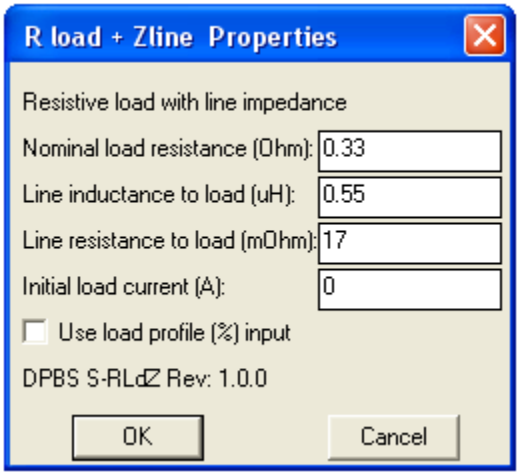
%Load This is the time-varying load input usually connected from a load profile block.

Output Pins: **Vload** The load voltage across the load resistance in volts.

Io The load current output in amperes according to the block input voltage, the internal load and the load control input pin. Connect to the %Load/Io input pin of the power converters.

Dialog properties:

The Resistive load with load line impedance block properties menu is shown in the following box which appears when right-clicking on the block.



Nominal load resistance:

Enter the desired nominal resistance of the load in Ohms.

Line inductance to load:

Enter the series inductance of the load line connection in micro-Henrys.

Line resistance to load:

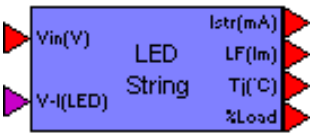
Enter the series resistance of the load line in milli-Ohms.

Initial load current:

Enter the initial value of the load current in amperes.

Use load profile (%) input:

Enable this check box to vary the load according to the % value at the %Load input pin.



LED String

The Light-emitting Diode (LED) string block models up to 30 LEDs connected in series.

Input Pins:

Vin(V) Input voltage pin in volts. This pin should be connected coming from the output voltage pin of a power converter block.

V-I(LED) Input pin for the input voltage-current forward characteristic of each LED within a string. This pin is activated if "Apply piecewise linear interpolation for V-I characteristic" is selected in the block dialog and "Import LED V-I characteristic from file" is not selected. The format of the input is a matrix of 2 rows x 20 columns of x-y (I-V) data. For less data points, fill in the remaining columns with zeros and select the number of valid data points in the dialog.

Output Pins:

Istr(mA) The string current in milli-amperes.

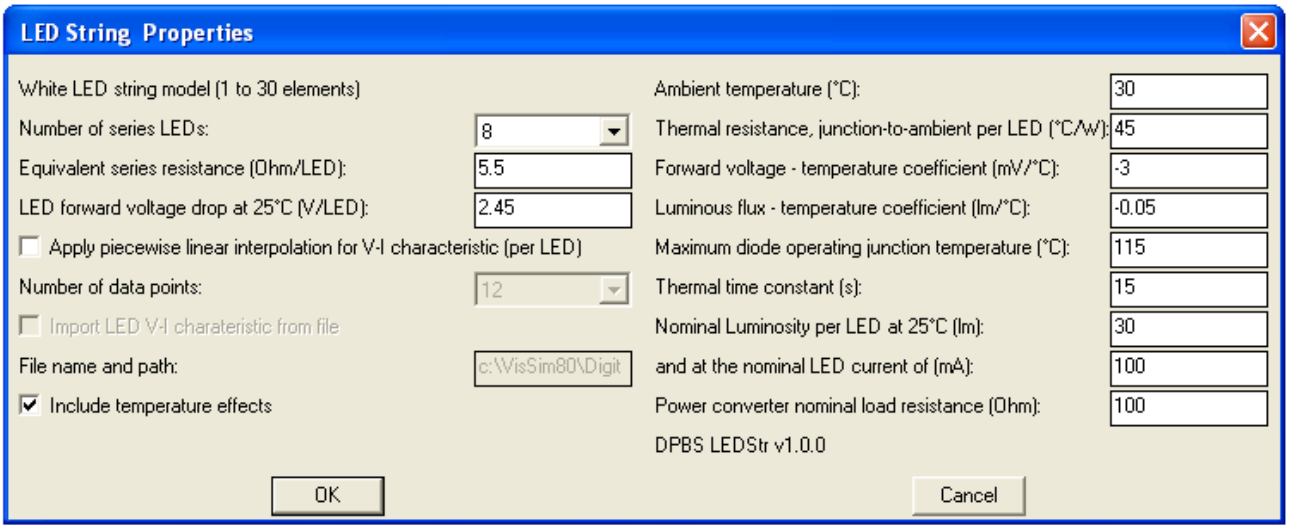
LF(lm) The total luminosity output of the LED string in lumens based upon the given nominal LED luminosity, the calculated temperature and the actual string current.

Tj(°C) The calculated junction temperature of each LED.

%Load A percentage output to be connected to the power converter which is loaded with the LED string. Connect this output pin to the Load% input pin of the power converter of which the output voltage is connected to the Vin input pin of this block.

Dialog properties:

The LED String block properties menu is shown in the following box which appears when right-clicking on the block.



Number of series LEDs:

Select from 1 to 30 LEDs connected in series.

Equivalent series resistance:

For the simple LED model, enter the value of the equivalent series resistance of each LED in Ohms.

LED forward voltage drop at 25°C (V/LED):

Again for the simple LED model, enter the value of the LED forward voltage drop in Volts.

Apply piecewise linear interpolation for V-I characteristic:

A piece-wise linear approximation can be applied to the LED curve in order to achieve a more accurate representation of the LED V-I characteristic.

Number of data points:

Enter the number of data points to be used within the model from 2 to 20.

Import LED V-I characteristic from file:

If the piecewise linear model is selected and this box is checked, the LED string block will use the specified data file. Otherwise the input V-I pin will be used for the V-I characteristic. The file and the matrix at the input pin should be 2 rows x 20 columns. If less data points are required, the file or matrix should be filled with zeros and the number of points in the model can be selected as above.

File path and name:

Enter the file name and path of the LED V-I characteristic data file.

Include temperature effects:

Select this if the LED temperature is to be considered within the model (applies to both the simple linear and the piece-wise linear models).

Ambient temperature (°C):

Enter the expected ambient temperature around the LED string in degrees centigrade.

Thermal resistance, junction-to-ambient per LED (°C/W):

Enter the value of the junction to ambient thermal resistance of each LED. This would be the sum of the junction to pad (case) thermal resistance, the pad to copper/FR4 printed circuit thermal resistance and the printed circuit to ambient thermal resistance.

Forward voltage temperature coefficient (mV/°C):

Enter the value of the rate at which the LED forward voltage (per LED) decreases with increasing temperature. This value would normally be negative as the forward voltage tends to decrease with temperature. This characteristic is assumed to be linear.

Luminous flux temperature coefficient (lm/°C):

Enter the value of the rate at which the luminous flux output of each LED varies with temperature. This value would normally be negative as the luminous flux tends to decrease with temperature. This characteristic is assumed to be linear.

Maximum diode operating junction temperature (°C):

Enter the value of the maximum LED junction operating temperature in degrees Celsius. If the LED model exceeds this temperature, the block will turn red and the simulation will be stopped.

Thermal time constant:

This value is related to the thermal inertia of the LED body and its mounting. It is assumed that for a change in LED power input, ΔP, the temperature will increase exponentially asymptotically towards its final value with a time constant equal to

this given value in seconds. Instantaneous changes will be modelled for a time constant equal to zero.

Nominal luminosity at 25°C (lm):

Enter the value of the nominal luminosity (per LED) at the nominal LED current in lumens.

and at the nominal LED current of:

Enter the value of the nominal LED current at which the nominal luminosity is specified.

Power converter nominal load resistance:

Enter the value of the nominal load resistance set in the dialog of the power converter to which the %Load output pin of this block is connected to the Load% input pin of that converter. For correct load performance, the value entered here must be the same as the value of the nominal load resistance entered in the power converter dialog.

Contents - Simulation



Controlled LED String

The controlled-Light-emitting Diode (LED) string block models up to 30 LEDs connected in series similar to the LED string block except that this model can be used to control the LEDs using a PWM control input.

Input Pins:

Vin(V) Input voltage pin in volts. This pin should be connected coming from the output voltage pin of a power converter block.

SW Control input for the PWM switch (SW < 1 = OFF, SW ≥ 1 = ON).

V-I(LED) Input pin for the input voltage-current forward characteristic of each LED within a string. This pin is activated if "Apply piecewise linear interpolation for V-I characteristic" is selected in the block dialog and "Import LED V-I characteristic from file" is not selected. The format of the input is a matrix of 2 rows x 20 columns of x-y (I-V) data. For less data points, fill in the remaining columns with zeros and select the number of valid data points in the dialog.

Output Pins:

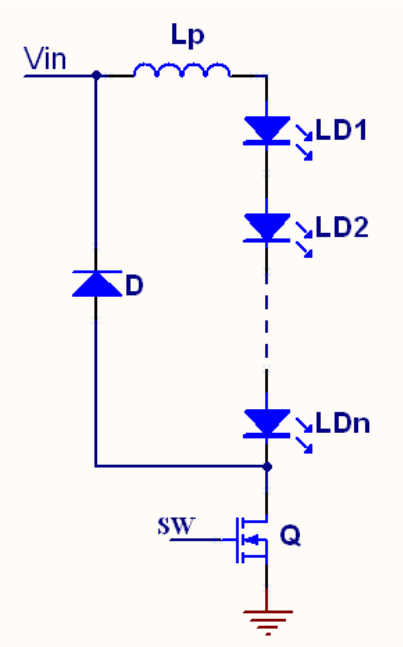
Istr(mA) The string current in milli-amperes.

LF(lm) The total luminosity output of the LED string in lumens based upon the given nominal LED luminosity, the calculated temperature and the actual string current. Note that for the controlled LED string, the luminosity output is filtered with a low-pass filter at 100Hz, which is above the normal conceivable flicker.

Tj(°C) The calculated junction temperature of each LED.

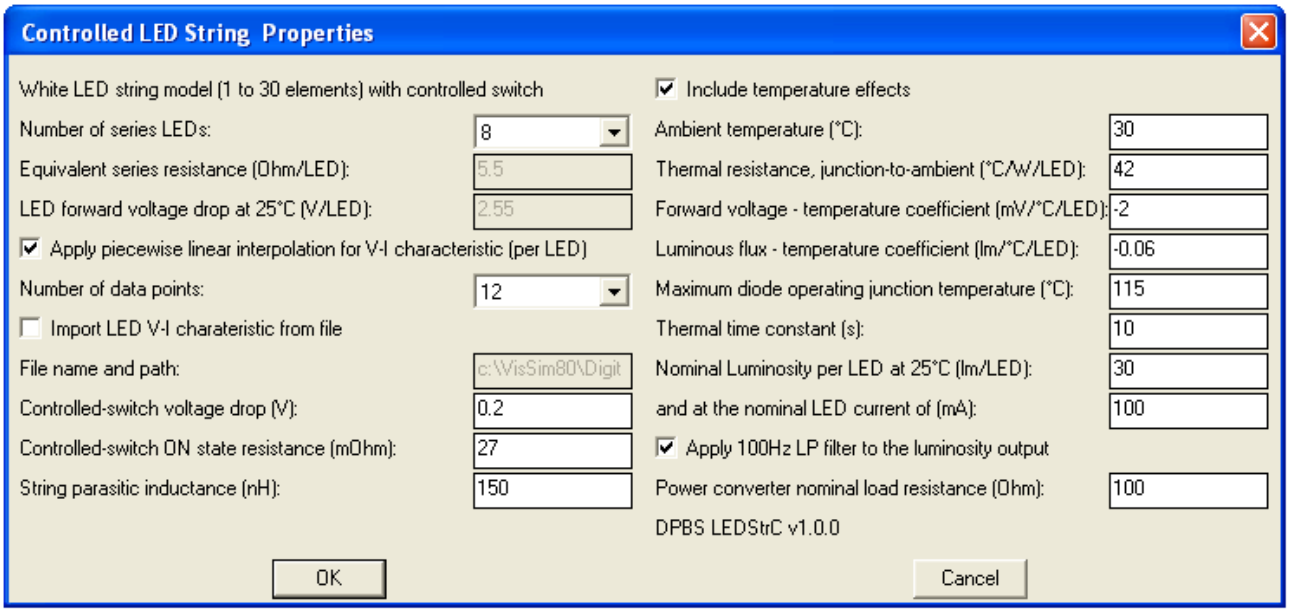
%Load A percentage output to be connected to the power converter which is loaded with the LED string. Connect this output pin to the Load% input pin of the power converter of which the output voltage is connected to the Vin input pin of this block.

Circuit schematic:



Dialog properties:

The controlled LED String block properties menu is shown in the following box which appears when right-clicking on the block.



Number of series LEDs:

Select from 1 to 30 LEDs connected in series.

Equivalent series resistance:

For the simple LED model, enter the value of the equivalent series resistance of each LED in Ohms.

LED forward voltage drop at 25°C (V/LED):

Again for the simple LED model, enter the value of the LED forward voltage drop in Volts.

Apply piecewise linear interpolation for V-I characteristic:

A piece-wise linear approximation can be applied to the LED curve in order to achieve a more accurate representation of the LED V-I characteristic.

Number of data points:

Enter the number of data points to be used within the model from 2 to 20.

Import LED V-I characteristic from file:

If the piecewise linear model is selected and this box is checked, the LED string block will use the specified data file. Otherwise the input V-I pin will be used for the V-I characteristic. The file and the matrix at the input pin should be 2 rows x 20 columns. If less data points are required, the file or matrix should be filled with zeros and the number of points in the model can be selected as above.

File path and name:

Enter the file name and path of the LED V-I characteristic data file.

Controlled-switch voltage drop:

The forward voltage drop, in Volts, across the PWM control switch of the LED string. This value will provide a fixed forward ON-state voltage regardless of the current flowing through the switch.

Controlled-switch ON-state resistance:

The ON-state resistance, in milli-Ohms, of the PWM control switch can be entered. This value will model a variable voltage drop dependent upon the current flowing through the switch such as with a MOSFET.

String parasitic inductance:

The LED string will have some parasitic inductance and the value can be entered here. In order to ensure correct operation of the LED string, without excessive voltage overshoot when switching off the PWM switch, the LED string is modelled with an ideal anti-parallel diode with a fixed forward voltage drop of 0.7V.

Include temperature effects:

Select this if the LED temperature is to be considered within the model (applies to both the simple linear and the piece-wise linear models).

Ambient temperature (°C):

Enter the expected ambient temperature around the LED string in degrees centigrade.

Thermal resistance, junction-to-ambient per LED (°C/W):

Enter the value of the junction to ambient thermal resistance of each LED. This would be the sum of the junction to pad (case) thermal resistance, the pad to copper/FR4 printed circuit thermal resistance and the printed circuit to ambient thermal resistance.

Forward voltage temperature coefficient (mV/°C):

Enter the value of the rate at which the LED forward voltage (per LED) decreases with increasing temperature. This value would normally be negative as the forward voltage tends to decrease with temperature. This characteristic is assumed to be linear.

Luminous flux temperature coefficient (lm/°C):

Enter the value of the rate at which the luminous flux output of each LED varies with temperature. This value would normally be negative as the luminous flux tends to decrease with temperature. This characteristic is assumed to be linear.

Maximum diode operating junction temperature (°C):

Enter the value of the maximum LED junction operating temperature in degrees Celsius. If the LED model exceeds this temperature, the block will turn red and the simulation will be stopped.

Thermal time constant:

This value is related to the thermal inertia of the LED body and its mounting. It is assumed that for a change in LED power input, ΔP, the temperature will increase exponentially asymptotically towards its final value with a time constant equal to this given value in seconds. Instantaneous changes will be modelled for a time constant equal to zero.

Nominal luminosity at 25°C (lm):

Enter the value of the nominal luminosity (per LED) at the nominal LED current in lumens.

and at the nominal LED current of :

Enter the value of the nominal LED current at which the nominal luminosity is specified.

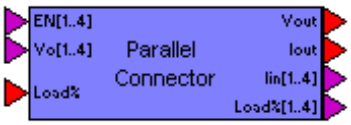
Apply 100Hz LP filter to the luminosity output:

If this box is checked, the luminosity output will be filtered by a 100Hz low-pass filter. Since the human eye cannot detect above this frequency it can be desirable to select this option to determine the effective visible luminosity (note that, depending upon the frequency and duty cycle the LED string may appear to be brighter than the calculated average luminosity).

Power converter nominal load resistance:

Enter the value of the nominal load resistance set in the dialog of the power converter to which the %Load output pin of this block is connected to the Load% input pin of that converter. For correct load performance, the value entered here must be the same as the value of the nominal load resistance entered in the power converter dialog.

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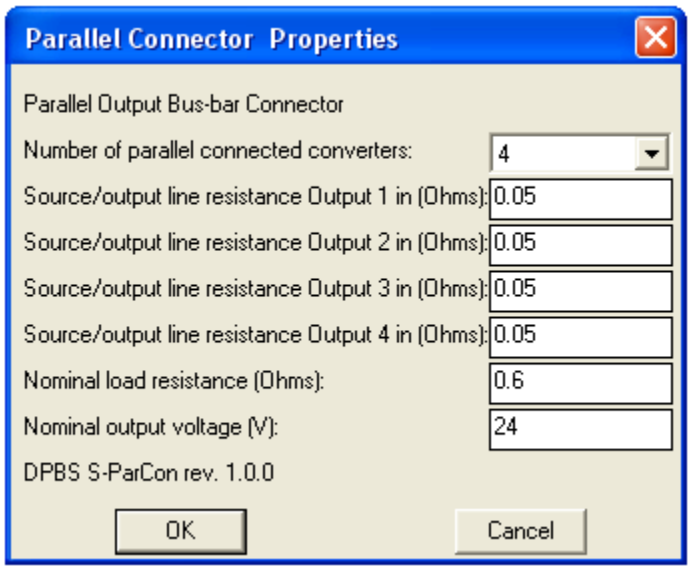
Parallel connector

Up to four power converters can be connected together at their output in a parallel configuration using this block.

Input Pins:	**EN[1..4]**	Enable input pin for each output – vector with columns = 4, rows = 1.
	Vo[1..4]	Output voltage input from each parallel-connected converter – vector with columns = 4, rows = 1.
	%Load	Total load on the system of converters expressed as a percentage – vector; columns = 4, rows = 1.
Output Pins:	**Vout**	The total output voltage in Volts.
	Iout	The total output current in Amperes determined by the output voltage and the Load% input pin.
	Iin[1..4]	Output currents of each of the parallel-connected converters into the parallel connector block – vector with columns = 4, rows = 1.
	Load%[1..4]	A percentage output for each converter according to the proportion of output impedances set in the dialog and the respective converter output voltage – vector with columns = 4, rows = 1. Connect this output to the Load%/Io input pin of each power converter connected here at the output. Alternatively, the Input currents above can be connected to each parallel-connected power converter.

Dialog properties:

The parallel connector block properties menu is shown in the following box which appears when right-clicking on the block.



Number of parallel connected converters:

Select from 1 to 4 converters.

Source / output line resistance output x:

Enter the value of the output line / connection resistance in Ohms for each connected converter. Different resistance values can be entered for each converter connection in order to verify load sharing control algorithms.

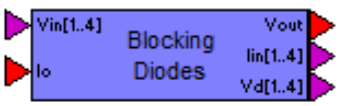
Nominal load resistance:

Enter the value of the nominal (full-load) load resistance in Ohms.

Nominal output voltage:

Enter the value of the nominal output voltage in Volts.

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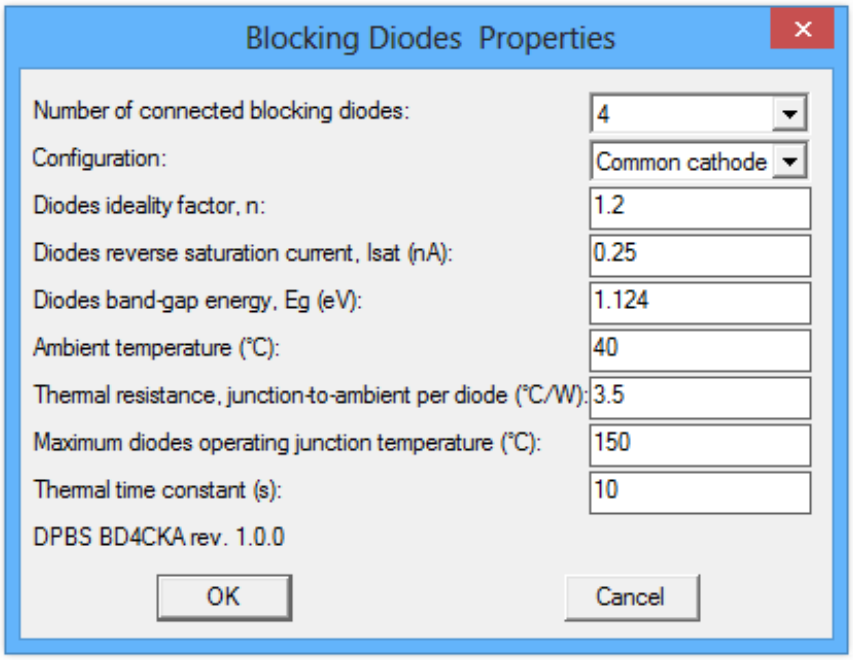
Blocking Diodes

This model uses the Schockly diode equation to emulate the diode characteristics. The limitations of this model are that the physical parameters need to be known.

Input Pins:	**Vin[1..4]**	Enable input pin for each output – vector with columns = 4, rows = 1.
	Io	The output current input (after the diode common connection) in amps.
Output Pins:	**Vout**	The total output voltage in Volts.
	Iin[1..4]	Output currents of each of the parallel-connected converters into the parallel connector block – vector with columns = 4, rows = 1.
	Vd1..4]	The forward voltage drop of the connected blocking diodes – vector with columns = 4, rows = 1.

Dialog properties:

The blocking diodes block properties menu is shown in the following box which appears when right-clicking on the block.



Number of connected blocking diodes:

Select from 1 to 4 diodes.

Configuration:

Select from:

1. Common cathode
2. Common anode

Diodes ideality factor, n:

Enter the ideality factor parameter for the diodes

Diodes reverse saturation current, Isat:

Enter the reverse saturation current in nano-amperes.

Diodes band-gap energy, Eg:

Enter the band-gap energy parameter of the diodes in Electron-Volts.

Ambient temperature:

Enter the ambient temperature in degrees Celsius.

Thermal resistance, junction-to-ambient per diode:

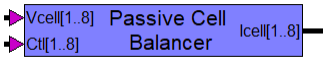
Enter the value of the thermal resistance in °C/W for each diode including mounting (to the ambient).

Maximum diodes operating junction temperature:

Enter the value of the nominal (full-load) load resistance in Ohms.

Thermal time constant:

Enter the value of the nominal output voltage in Volts.



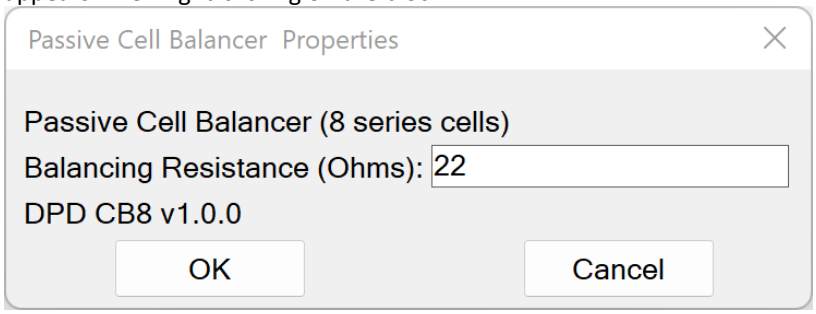
Passive Cell Balancer

This block models a passive (resistive) battery cell balancer. It can be controlled using the Cell Balance Controller in the Codegen section.

Input Pins:	**Vcell[1..8]**	The cell voltage inputs – vector with columns = 8, rows = 1.
	Ctrl[1..8]	The control inputs switching on (=1) or off (=0) each cell balancer.
Output Pins:	**Icell1..8]**	The balancing current output for each of up to 8 cells.

Dialog properties:

The cell balancer block properties menu is shown in the following box which appears when right-clicking on the block.



Balancing resistance (ohms):

Enter the passive resistance value for each cell connection in Ohms.

More than eight cells can be balanced by placing multiple blocks in a diagram.

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Block Reference – Real-time

The real-time section of Altair Embed / Digital Power Designer consists of a series of blocks which can be used in simulations and / or code-generation.

The blocks in this section are designed to be used in fast simulations, to be able to be used together with Altair Embed Analyze for frequency domain analysis and to be code-generated in order to run optimized models in real-time applications on real-time hardware.

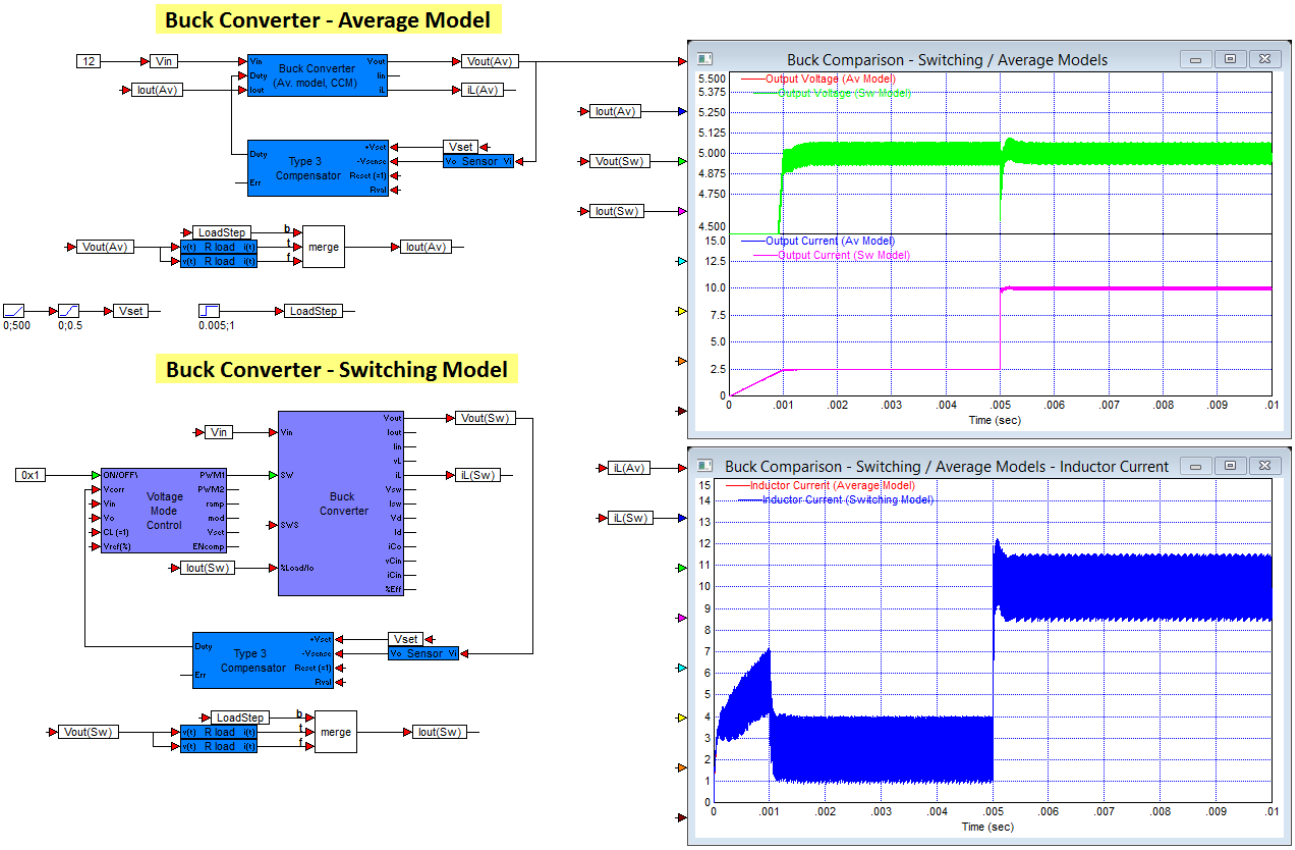
The blocks in this section of DPD are in general considerably simplified when compared to the simulation section of DPD and have fewer configuration options.

Block Convention

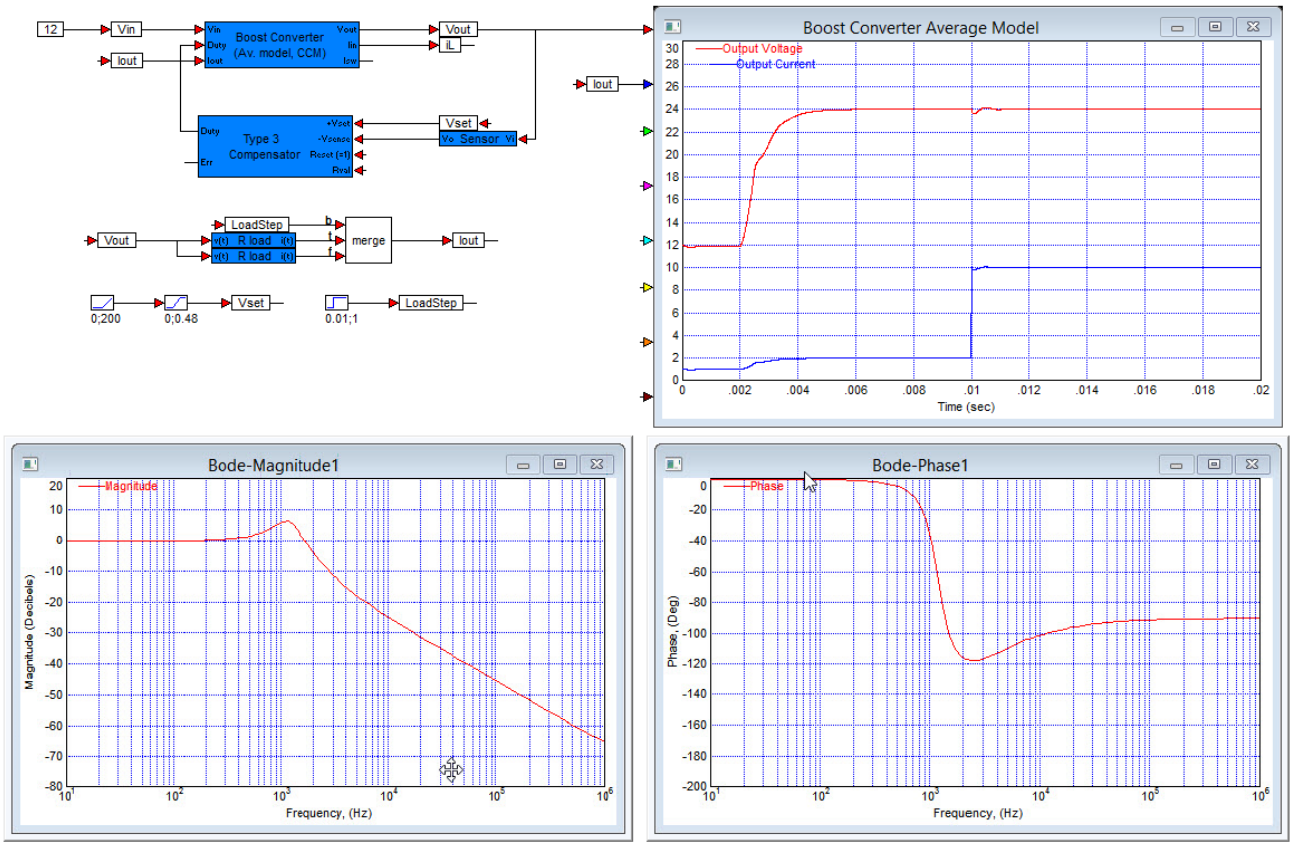
The blocks within the real-time environment are colour-coded in blue in order to distinguish them from the other blocks within DPD which have differencing functions. The blocks and their colours can be customized if so desired by CTL + right clicking on the block to bring up the compound block properties dialog.

Some examples of the use of the real-time blocks within the digital power designer block set.

Examples of Applications of Real-time Blocks



Average model comparison with the switching models of the simulation section of DPD. The average models do not model the switching characteristics of the converter.



Using analyze to plot the frequency response of the converter or control loop.

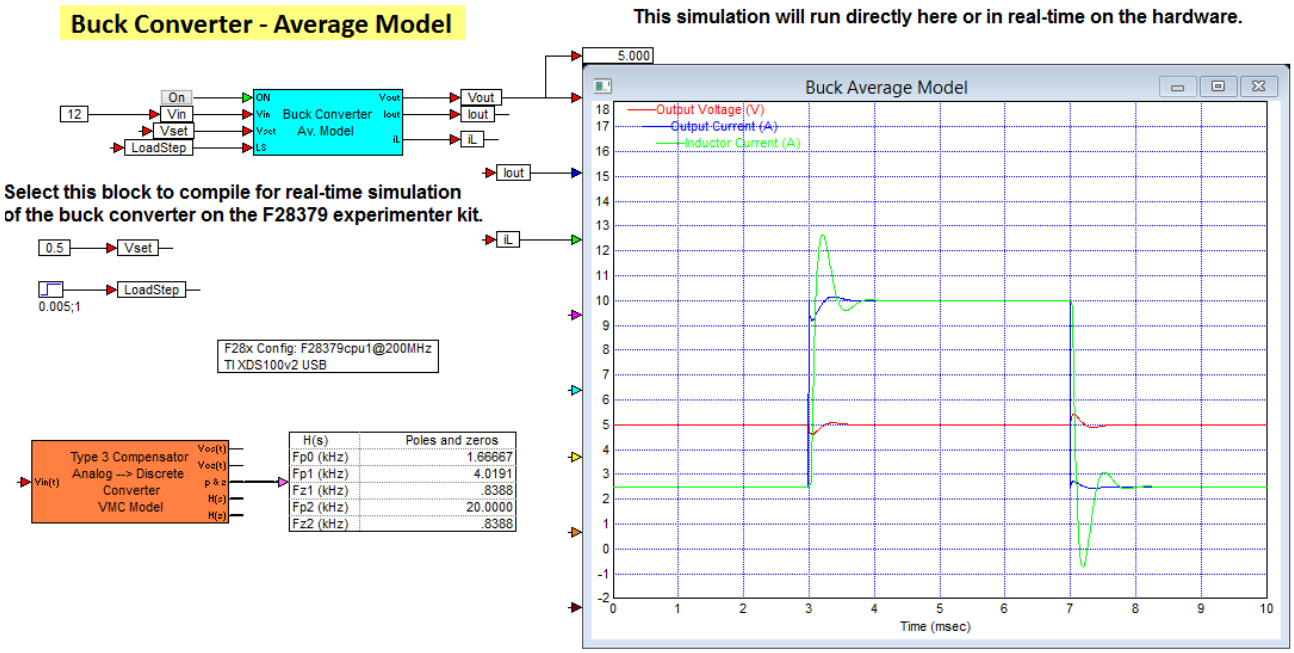
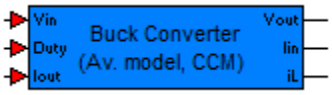


Diagram for code-generation of models for real-time simulation.

Average Models - Converters



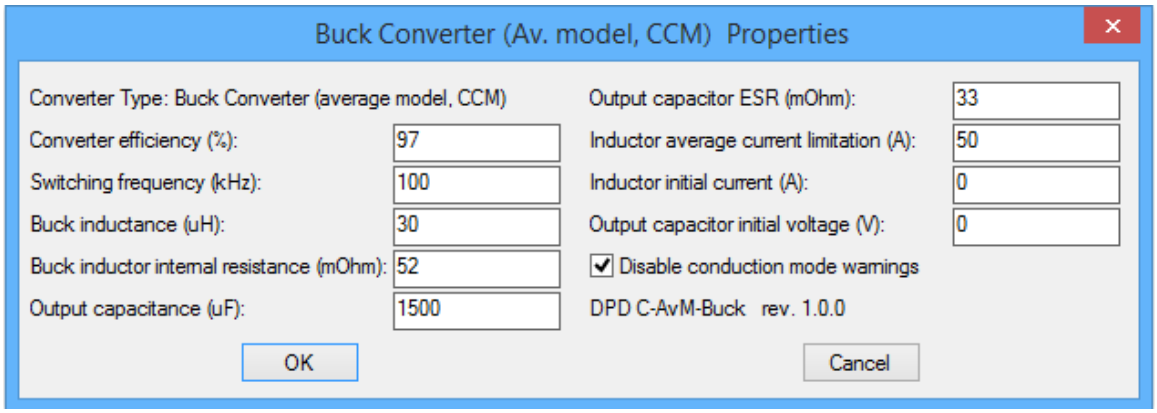
Buck Converter (CCM)

Average model of a buck converter in continuous conduction mode (CCM).

Input pins:	**Vin**	Input Voltage (V).
	Duty	The duty cycle control input (0..1).
	Iout	The converter output current (A).
Output pins:	**Vout**	The output voltage of the converter (V).
	Iin	The input current to the converter (A).
	iL	The buck inductor current (A).

Dialog properties:

The buck converter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Converter efficiency:

Enter the value of the expected efficiency of the converter. The input parameters will be compensated for this efficiency value.

Switching frequency:

Enter the value of the expected switching frequency. This value is only required for the conduction mode warnings.

Buck inductance:

Enter the value of the buck inductance in micro-Henrys.

Buck inductor internal resistance:

Enter the value of the internal resistance of the inductor in milli-ohms.

Output capacitance:

Enter the value of the converter output capacitance in micro-Farads.

Output capacitor ESR:

Enter the value of the output capacitor internal resistance (ESR) in milli-ohms.

Inductor average current limitation:

Enter the value to limit the internal inductor current of the converter in amperes.

Initial inductor current:

Enter the value of the initial inductor current in amperes.

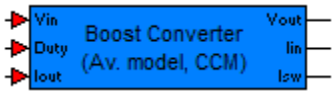
Initial capacitor voltage:

Enter the value of the initial capacitor voltage in volts.

Disable conduction mode warnings:

Since this average model is valid for continuous conduction mode (CCM), check this to disable the conduction mode warnings if the converter momentarily enters discontinuous conduction mode (DCM).

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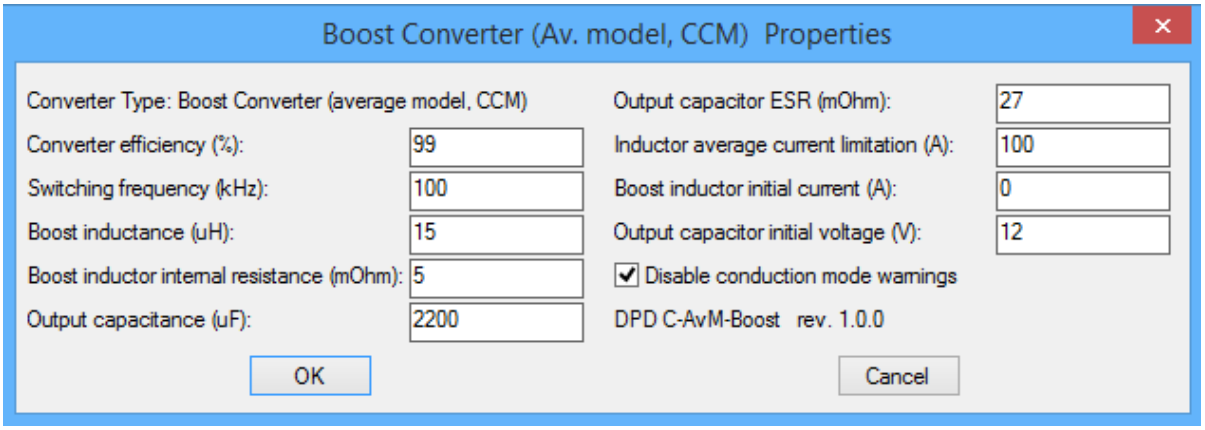
Boost Converter (CCM)

Average model of a boost converter in continuous conduction mode (CCM).

Input pins:	**Vin**	Input Voltage (V).
	Duty	The duty cycle control input (0..1).
	Iout	The converter output current (A).
Output pins:	**Vout**	The output voltage of the converter (V).
	Iin	The input current to the converter (A).
	Isw	The boost switch current (A).

Dialog properties:

The boost converter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Converter efficiency:

Enter the value of the expected efficiency of the converter. The input parameters will be compensated for this efficiency value.

Switching frequency:

Enter the value of the expected switching frequency. This value is only required for the conduction mode warnings.

Boost inductance:

Enter the value of the buck inductance in micro-Henrys.

Boost inductor internal resistance:

Enter the value of the internal resistance of the inductor in milli-ohms.

Output capacitance:

Enter the value of the converter output capacitance in micro-Farads.

Output capacitor ESR:

Enter the value of the output capacitor internal resistance (ESR) in milli-ohms.

Inductor average current limitation:

Enter the value to limit the internal inductor current of the converter in amperes.

Initial inductor current:

Enter the value of the initial inductor current in amperes.

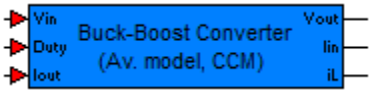
Initial capacitor voltage:

Enter the value of the initial capacitor voltage in volts.

Disable conduction mode warnings:

Since this average model is valid for continuous conduction mode (CCM), check this to disable the conduction mode warnings if the converter momentarily enters discontinuous conduction mode (DCM).

[Contents – Real-time]



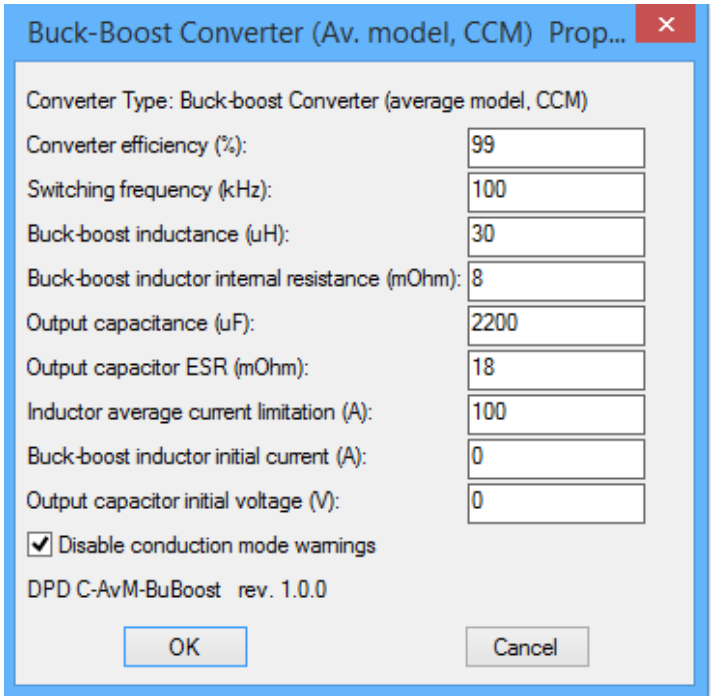
Buck-boost Converter (CCM)

Average model of a buck-boost converter in continuous conduction mode (CCM).

Input pins:	**Vin**	Input Voltage (V).
	Duty	The duty cycle control input (0..1).
	Iout	The converter output current (A).
Output pins:	**Vout**	The output voltage of the converter (V).
	Iin	The input current to the converter (A).
	iL	The buck-boost inductor current (A).

Dialog properties:

The buck-boost converter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Converter efficiency:

Enter the value of the expected efficiency of the converter. The input parameters will be compensated for this efficiency value.

Switching frequency:

Enter the value of the expected switching frequency. This value is only required for the conduction mode warnings.

Buck-boost inductance:

Enter the value of the buck inductance in micro-Henrys.

Buck-boost inductor internal resistance:

Enter the value of the internal resistance of the inductor in milli-ohms.

Output capacitance:

Enter the value of the converter output capacitance in micro-Farads.

Output capacitor ESR:

Enter the value of the output capacitor internal resistance (ESR) in milli-ohms.

Inductor average current limitation:

Enter the value to limit the internal inductor current of the converter in amperes.

Initial inductor current:

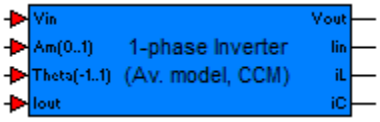
Enter the value of the initial inductor current in amperes.

Initial capacitor voltage:

Enter the value of the initial capacitor voltage in volts.

Disable conduction mode warnings:

Since this average model is valid for continuous conduction mode (CCM), check this to disable the conduction mode warnings if the converter momentarily enters discontinuous conduction mode (DCM).



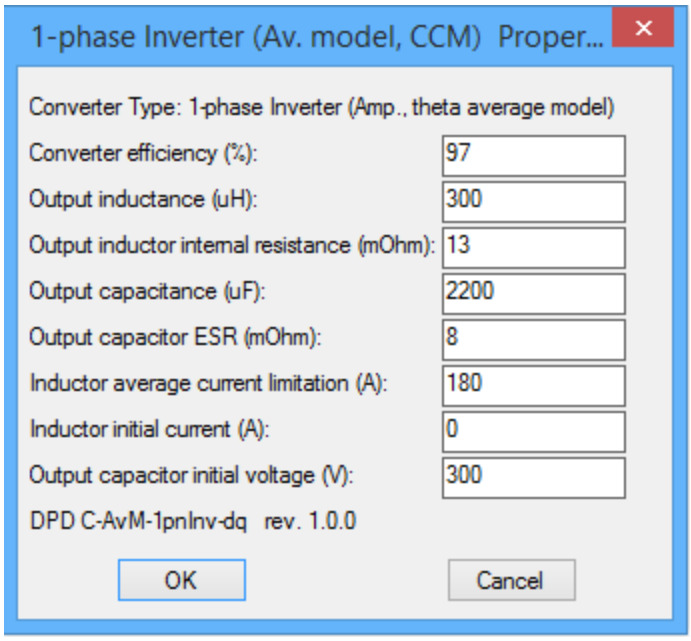
Single-phase Inverter (CCM, Amp.-Theta Control)

Average model of a single-phase inverter in continuous conduction mode (CCM) with amplitude and phase angle control inputs.

Input pins:	**Vin**	Input DC Voltage (V).
	AM	The amplitude control input from 0 to 1.
	Theta	The phase angle control input from -1 to 1, scaled to π or 180 degrees.
	Iout	The inverter output current (A).
Output pins:	**Vout**	The output voltage of the inverter (V).
	Iin	The input current to the inverter (A).
	iL	The inverter output filter inductor current (A).
	iC	The inverter output filter capacitor current (A)

Dialog properties:

The single-phase inverter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Inverter efficiency:

Enter the value of the expected efficiency of the inverter. The input parameters will be compensated for this efficiency value.

Output inductance:

Enter the value of the inverter output filter inductance in micro-Henrys.

Output inductor internal resistance:

Enter the value of the internal resistance of the output inductor in milli-ohms.

Output capacitance:

Enter the value of the inverter output filter capacitance in micro-Farads.

Output capacitor ESR:

Enter the value of the output capacitor internal resistance (ESR) in milli-ohms.

Inductor average current limitation:

Enter the value to limit the internal inductor current of the converter in amperes.

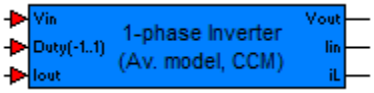
Initial inductor current:

Enter the value of the initial inductor current in amperes.

Output capacitor initial voltage:

Enter the value of the output capacitor initial voltage in volts.

Contents – Real-time



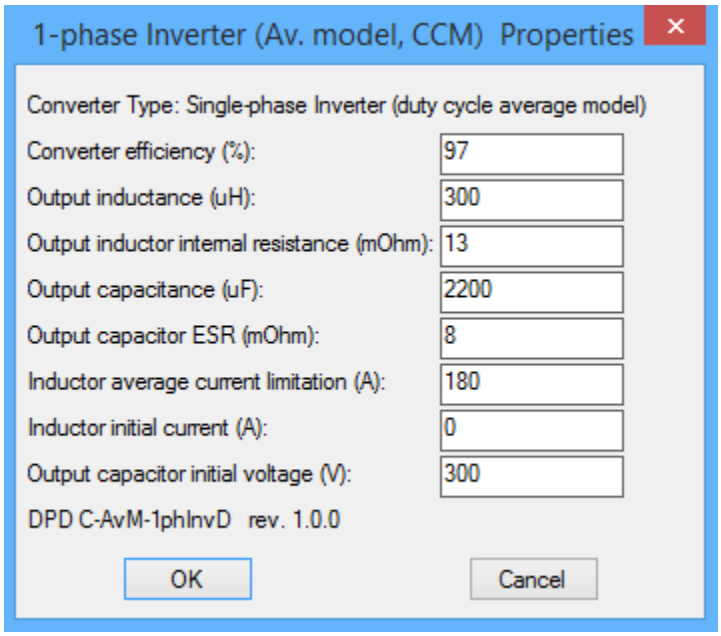
Single-phase Inverter (CCM, Duty-cycle Control)

Average model of a single-phase inverter in continuous conduction mode (CCM) using a duty-cycle input to control the converter output.

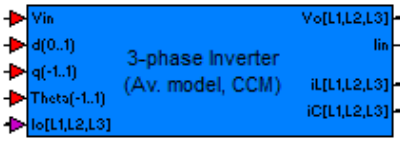
Input pins:	**Vin**	Input DC Voltage (V).
	Duty	The duty cycle control input (0..1).
	Iout	The inverter output current (A).
Output pins:	**Vout**	The output voltage of the inverter (V).
	Iin	The input current to the inverter (A).
	iL	The inverter output filter inductor current (A).

Dialog properties:

The single-phase inverter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



The dialog parameters are similar to the single-phase inverter with amplitude and phase angle control.



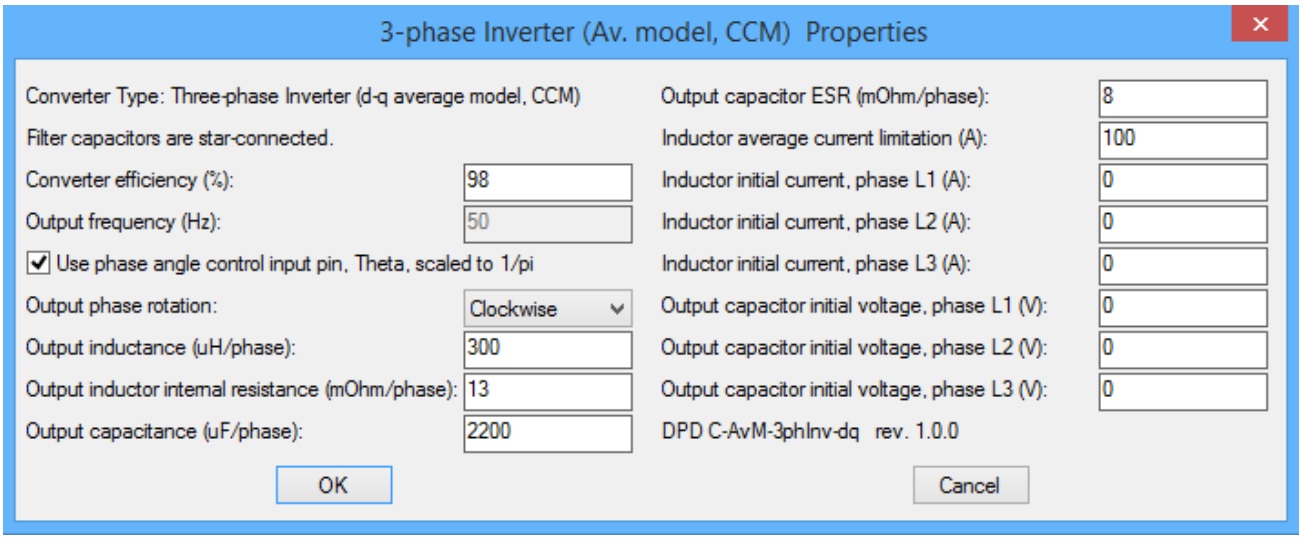
Three-phase Inverter (CCM, d-q Control)

Average model of a three-phase inverter in continuous conduction mode (CCM) with direct and quadrature axis control inputs.

Input pins:	**Vin**	Input DC Voltage (V).
	AM	The amplitude control input from 0 to 1.
	Theta	The phase angle control input from -1 to 1, scaled to π or 180 degrees.
	Iout	The inverter output current (A).
Output pins:	**Vout**	The output voltage of the inverter (V).
	Iin	The input current to the inverter (A).
	iL	The inverter output filter inductor current (A).
	iC	The inverter output filter capacitor current (A)

Dialog properties:

The three-phase inverter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Inverter efficiency:

Enter the value of the expected efficiency of the inverter. The input parameters will be compensated for this efficiency value.

Output frequency:

Enter the nominal frequency output of the inverter in Hertz (if phase angle pin is not used).

Use phase angle control pin, Theta:

Select this if the inverter phase angle and frequency is to be controlled from the Theta input pin (scaled to 1/π radians).

Output phase rotation:

Select between clockwise and anti-clockwise rotation of the output phases.

Output inductance:

Enter the value of the inverter output filter inductance in micro-Henrys / phase.

Output inductor internal resistance:

Enter the value of the internal resistance of the output inductor in milli-ohms / phase.

Output capacitance:

Enter the value of the inverter output filter capacitance in micro-Farads / phase.

Output capacitor ESR:

Enter the value of the output capacitor internal resistance (ESR) in milli-ohms / phase.

Inductor average current limitation:

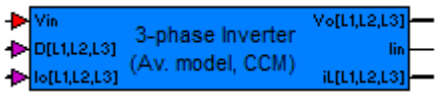
Enter the value to limit the internal inductor current of the converter in amperes.

Initial inductor current L1, L2, L3:

Enter the value of the initial inductor current in amperes for each phase.

Output capacitor initial voltage, L1, L2, L3:

Enter the value of the output capacitor initial voltage in volts for each phase.



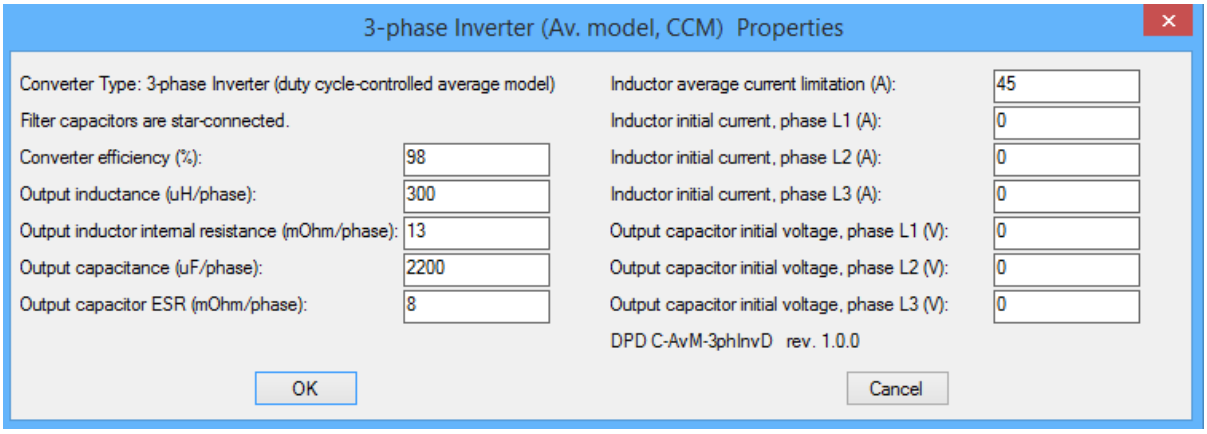
Three-phase Inverter (CCM, duty-cycle Control)

Average model of a three-phase inverter in continuous conduction mode (CCM) with duty-cycle control input.

Input pins:	**Vin**	Input DC Voltage (V).
	AM	The amplitude control input from 0 to 1.
	Theta	The phase angle control input from -1 to 1, scaled to π or 180 degrees.
	Iout	The inverter output current (A).
Output pins:	**Vout**	The output voltage of the inverter (V).
	Iin	The input current to the inverter (A).
	iL	The inverter output filter inductor current (A).
	iC	The inverter output filter capacitor current (A)

Dialog properties:

The three-phase inverter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Inverter efficiency:

Enter the value of the expected efficiency of the inverter. The input parameters will be compensated for this efficiency value.

Output inductance:

Enter the value of the inverter output filter inductance in micro-Henrys / phase.

Output inductor internal resistance:

Enter the value of the internal resistance of the output inductor in milli-ohms / phase.

Output capacitance:

Enter the value of the inverter output filter capacitance in micro-Farads / phase.

Output capacitor ESR:

Enter the value of the output capacitor internal resistance (ESR) in milli-ohms / phase.

Inductor average current limitation:

Enter the value to limit the internal inductor current of the converter in amperes.

Initial inductor current L1, L2, L3:

Enter the value of the initial inductor current in amperes for each phase.

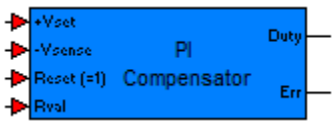
Output capacitor initial voltage, L1, L2, L3:

Enter the value of the output capacitor initial voltage in volts for each phase.

Contents – Real-time

Average Models – Control

The control blocks provide compensators and controllers for real-time simulation.

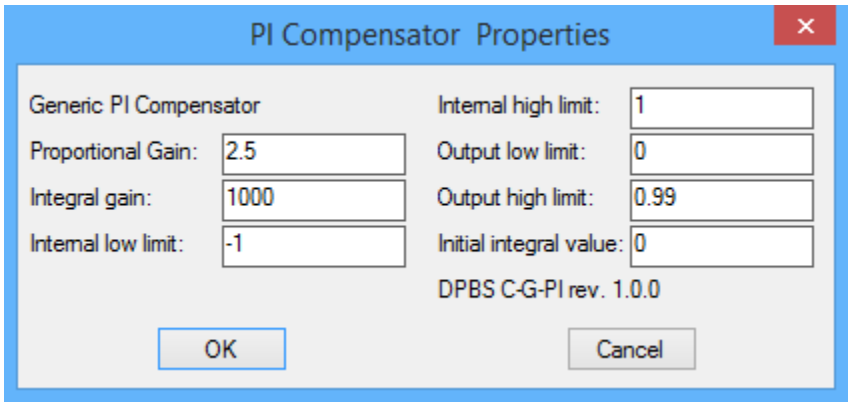


PI Compensator

Input pins:	**+Vset**	Set point value of the compensator (+).
	-Vsense	Sense input to the compensator (-).
	Reset	Reset input to reset the compensator.
	Rval	The reset value which will be set when the reset input pin = 1.
Output pins:	**Duty**	The compensator control output which can be connected to a duty cycle input of a converter.
	Err	Error output which is the difference between the sense and set inputs.

Dialog properties:

The PI compensator average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Proportional gain:

Enter the value of the proportional gain of the PI compensator.

Integral gain:

Enter the value of the integral gain of the PI compensator.

Internal low limit:

Enter the value of the internal low limit of the integral stage.

Internal high limit:

Enter the value of the internal high limit of the integral stage.

Output low limit:

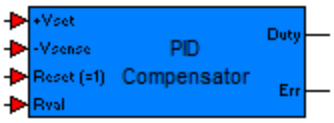
Enter the value of the output low limit of the compensator.

Output high limit:

Enter the value of the output high limit of the compensator.

Initial integral value:

Enter the value of the initial value of the internal integrator (before reset).

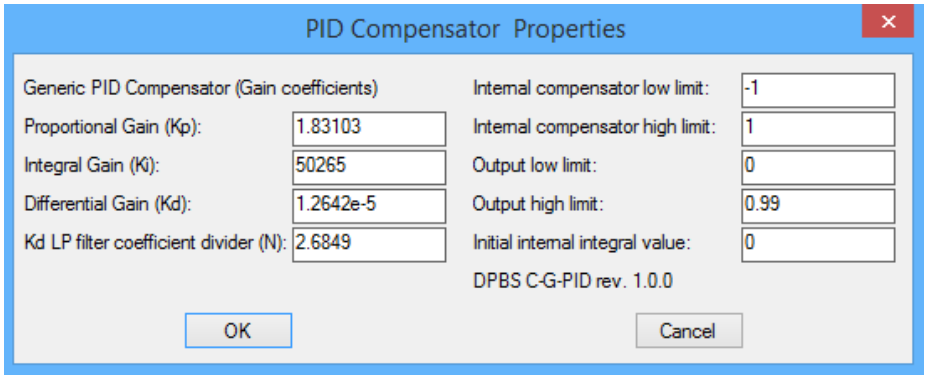


PID Compensator

Input pins:	**+Vset**	Set point value of the compensator (+).
	-Vsense	Sense input to the compensator (-).
	Reset	Reset input to reset the compensator.
	Rval	The reset value which will be set when the reset input pin = 1.
Output pins:	**Duty**	The compensator control output which can be connected to a duty cycle input of a converter.
	Err	Error output which is the difference between the sense and set inputs.

Dialog properties:

The PID compensator average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Proportional gain:

Enter the value of the proportional gain of the PID compensator.

Integral gain:

Enter the value of the integral gain of the PID compensator.

Proportional gain:

Enter the value of the differential gain of the PID compensator.

Integral gain:

Enter the value of the differential gain low-pass filter coefficient divider.

Internal low limit:

Enter the value of the internal low limit of the integral stage.

Internal high limit:

Enter the value of the internal high limit of the integral stage.

Output low limit:

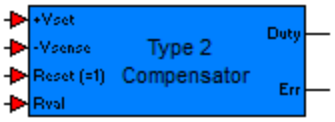
Enter the value of the output low limit of the compensator.

Output high limit:

Enter the value of the output high limit of the compensator.

Initial integral value:

Enter the value of the initial value of the internal integrator (before reset).

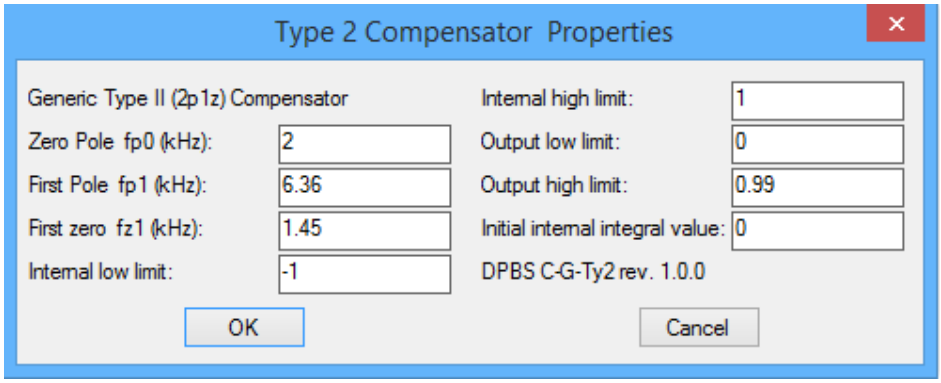


Type 2 Compensator

Input pins:	**+Vset**	Set point value of the compensator (+).
	-Vsense	Sense input to the compensator (-).
	Reset	Reset input to reset the compensator.
	Rval	The reset value which will be set when the reset input pin = 1.
Output pins:	**Duty**	The compensator control output which can be connected to a duty cycle input of a converter.
	Err	Error output which is the difference between the sense and set inputs.

Dialog properties:

The Type 2 compensator average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Zero pole, fp0:

Enter the value of the zero pole of the compensator in kHz.

First pole, fp1:

Enter the value of the first pole of the compensator in kHz.

First zero, fz1:

Enter the value of the first zero of the compensator in kHz..

Internal low limit:

Enter the value of the internal low limit of the integral stage.

Internal high limit:

Enter the value of the internal high limit of the integral stage.

Output low limit:

Enter the value of the output low limit of the compensator.

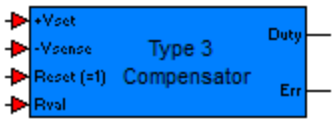
Output high limit:

Enter the value of the output high limit of the compensator.

Initial integral value:

Enter the value of the initial value of the internal integrator (before reset).

Contents – Real-time

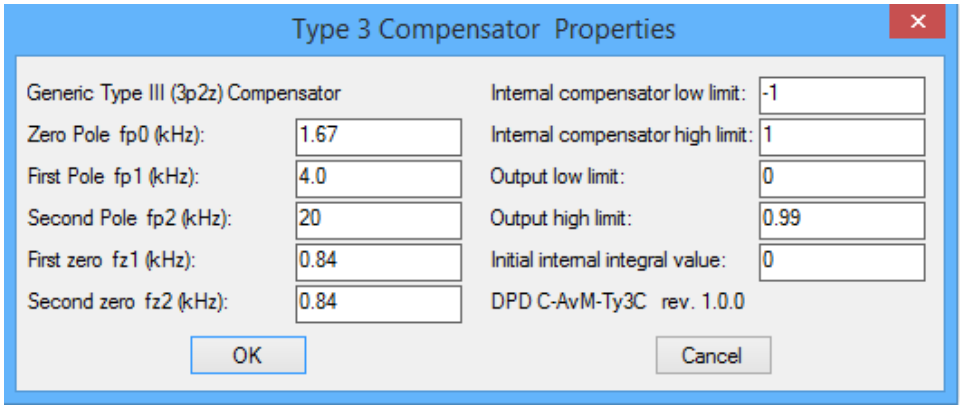


Type 3 Compensator

Input pins:	**+Vset**	Set point value of the compensator (+).
	-Vsense	Sense input to the compensator (-).
	Reset	Reset input to reset the compensator.
	Rval	The reset value which will be set when the reset input pin = 1.
Output pins:	**Duty**	The compensator control output which can be connected to a duty cycle input of a converter.
	Err	Error output which is the difference between the sense and set inputs.

Dialog properties:

The Type 3 compensator average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Zero pole, fp0:

Enter the value of the zero pole of the compensator in kHz.

First pole, fp1:

Enter the value of the first pole of the compensator in kHz.

Second pole, fp2:

Enter the value of the second pole of the compensator in kHz.

First zero, fz1:

Enter the value of the first zero of the compensator in kHz.

Second zero, fz2:

Enter the value of the second zero of the compensator in kHz.

Internal low limit:

Enter the value of the internal low limit of the integral stage.

Internal high limit:

Enter the value of the internal high limit of the integral stage.

Output low limit:

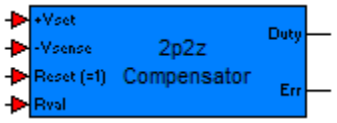
Enter the value of the output low limit of the compensator.

Output high limit:

Enter the value of the output high limit of the compensator.

Initial integral value:

Enter the value of the initial value of the internal integrator (before reset).

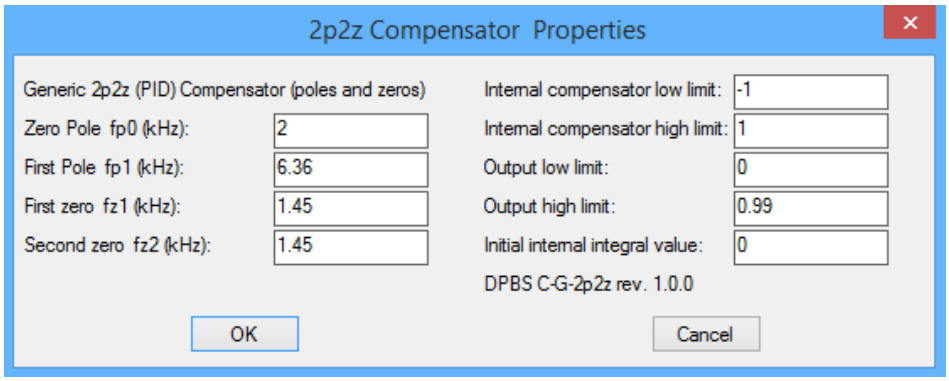


2p2z Compensator

Input pins:	**+Vset**	Set point value of the compensator (+).
	-Vsense	Sense input to the compensator (-).
	Reset	Reset input to reset the compensator.
	Rval	The reset value which will be set when the reset input pin = 1.
Output pins:	**Duty**	The compensator control output which can be connected to a duty cycle input of a converter.
	Err	Error output which is the difference between the sense and set inputs.

Dialog properties:

The 2p2z compensator average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Zero pole, fp0:

Enter the value of the zero pole of the compensator in kHz.

First pole, fp1:

Enter the value of the first pole of the compensator in kHz.

First zero, fz1:

Enter the value of the first zero of the compensator in kHz.

Second zero, fz2:

Enter the value of the second zero of the compensator in kHz

Internal low limit:

Enter the value of the internal low limit of the integral stage.

Internal high limit:

Enter the value of the internal high limit of the integral stage.

Output low limit:

Enter the value of the output low limit of the compensator.

Output high limit:

Enter the value of the output high limit of the compensator.

Initial integral value:

Enter the value of the initial value of the internal integrator (before reset).

Contents – Real-time



ANF-PLL

Analog Notch Filter Phase Lock Loop

Input pins: **Vin(t)** The input signal to the PLL.

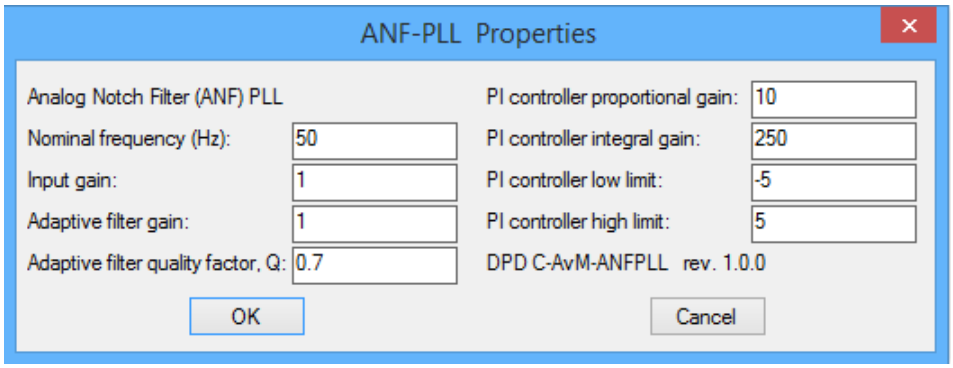
Output pins: **Vo(t)** The reconstructed sine-wave output signal of the PLL.

F (Hz) The measured frequency of the input signal in Hertz.

Theta (rad) The measured phase angle of the input signal in radians.

Dialog properties:

The ANF-PLL average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Nominal frequency:

Enter the value of the nominal frequency of the input signal in Hertz.

Input gain:

Enter the value of the input gain to the PLL.

Adaptive filter gain:

Enter the value of the gain of the internal adaptive (notch) filter.

Adaptive filter quality factor, Q:

Enter the value of the quality factor of the internal adaptive (notch) filter.

PI controller Proportional gain:

Enter the value of the proportional gain of the internal PI compensator.

PI controller Integral gain:

Enter the value of the integral gain of the internal PI compensator.

PI controller low limit:

Enter the value of the output low limit of the compensator.

PI controller high limit:

Enter the value of the output high limit of the compensator.



SRF-PLL

Synchronous Reference Frame Phase Lock Loop

Input pins: **Vin(t)** The input signal to the PLL.

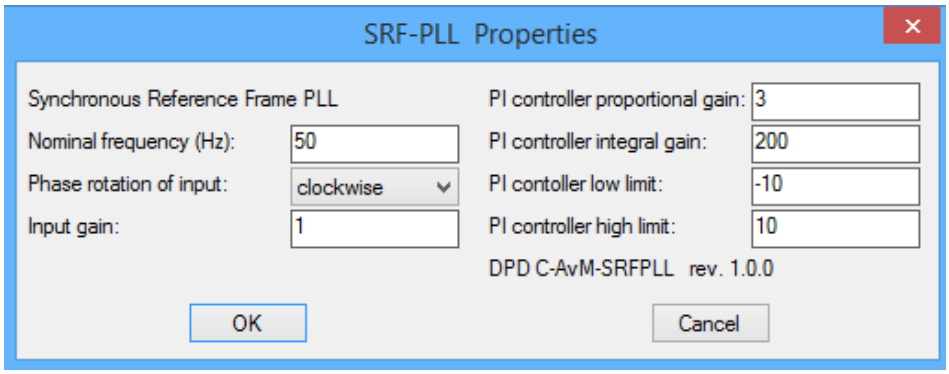
Output pins: **Vo(t)** The reconstructed sine-wave output signal of the PLL.

F (Hz) The measured frequency of the input signal in Hertz.

Theta (rad) The measured phase angle of the input signal in radians.

Dialog properties:

The SRF-PLL average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Nominal frequency:

Enter the value of the nominal frequency of the input signal in Hertz.

Phase rotation of input:

Select if the phase rotation of the input signal is clockwise or anti-clockwise.

Input gain:

Enter the value of the input gain to the PLL.

PI controller Proportional gain-:

Enter the value of the proportional gain of the internal PI compensator.

PI controller Integral gain:

Enter the value of the integral gain of the internal PI compensator.

PI controller low limit:

Enter the value of the output low limit of the compensator.

PI controller high limit:

Enter the value of the output high limit of the compensator.

Contents – Real-time



SOGI-PLL

Second Order Generalised Integrator Phase Lock Loop

Input pins: **Vin(t)** The input signal to the PLL.

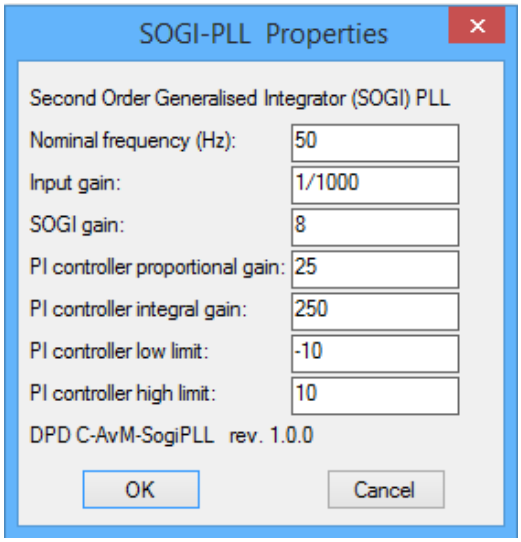
Output pins: **Vo(t)** The reconstructed sine-wave output signal of the PLL.

F (Hz) The measured frequency of the input signal in Hertz.

Theta (rad) The measured phase angle of the input signal in radians.

Dialog properties:

The SOGI-PLL average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Nominal frequency:

Enter the value of the nominal frequency of the input signal in Hertz.

Input gain:

Enter the value of the input gain to the PLL.

SOGI gain:

Enter the value of the gain of the SOGI stage.

PI controller Proportional gain:

Enter the value of the proportional gain of the internal PI compensator.

PI controller Integral gain:

Enter the value of the integral gain of the internal PI compensator.

PI controller low limit:

Enter the value of the output low limit of the compensator.

PI controller high limit:

Enter the value of the output high limit of the compensator.



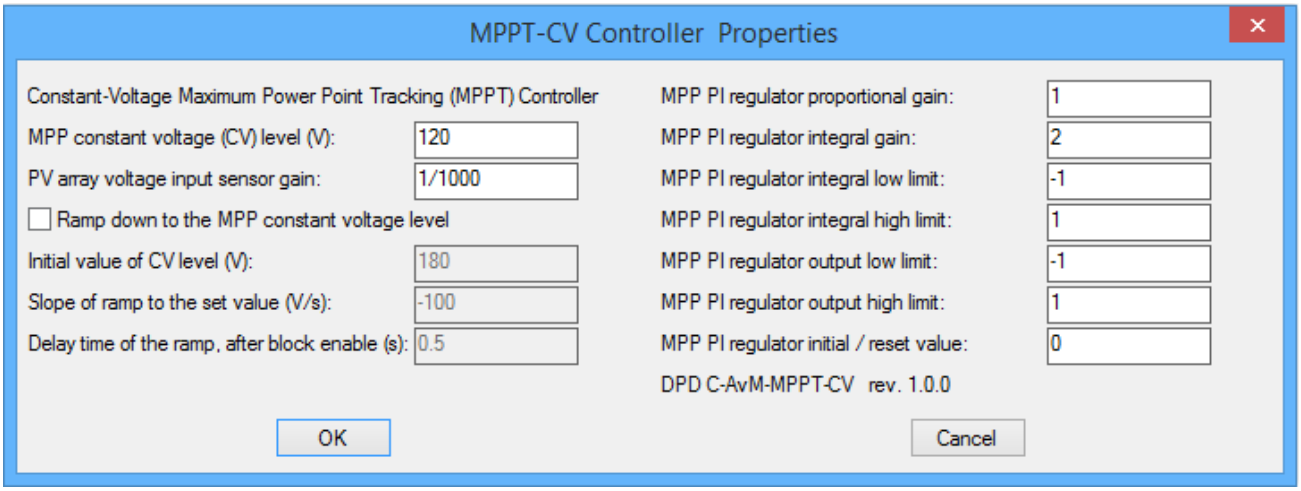
MPPT-CV

Maximum Power Point Tracking – Constant Voltage controller.

Input pins:	**ENreg**	Enable input to enable the MPPT regulation.
	Vpv	PV panel voltage input from sensor.
	Vref	Constant voltage regulation set point voltage (V).
Output pins:	**d**	Output control for constant voltage regulation.
	CV	The constant voltage regulation value (also under soft start).

Dialog properties:

The MPPT-CV controller average model block properties menu is shown in the following figure which appears when right-clicking on the block.



MPP constant voltage level:

Enter the value of the nominal frequency of the input signal in Hertz.

PV array voltage input sensor gain:

Enter the value of the input gain to the PLL.

Ramp down to the MPP constant voltage level:

Selecting this option sets a soft start on the CV regulation.

Initial value of CV level:

Enter the initial value of the ramp.

Slope of ramp to the set value:

Enter the ramp slope.

Delay time of the ramp after block enable.

Enter the desired delay time for the ramp down commencement in seconds after the regulation is enabled.

MPP PI controller proportional gain:

Enter the value of the proportional gain of the internal PI compensator.

MPP PI controller integral gain:

Enter the value of the integral gain of the internal PI compensator.

MPP PI controller low limit:

Enter the value of the internal integral low limit of the compensator.

MPP PI controller high limit:

Enter the value of the internal integral high limit of the compensator.

MPP PI controller low limit:

Enter the value of the output low limit of the internal compensator.

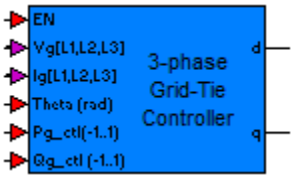
MPP PI controller high limit:

Enter the value of the output high limit of the internal compensator.

MPP PI regulator initial / reset value:

Enter the initial and reset value of the internal PI regulator.

Contents – Real-time



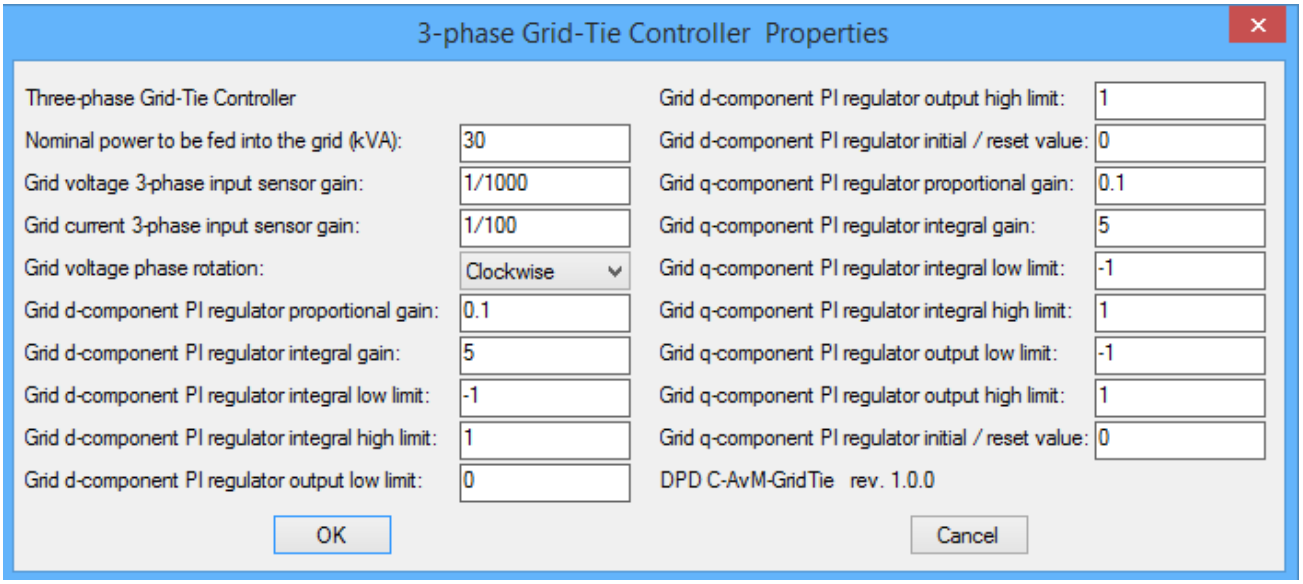
Three-phase Grid-Tie Controller

A controller for controlling the connection of a power converter to a grid supply using direct power control.

Input pins:	**Vin(t)**	The input signal to the PLL.
	Vg[L1,L2,L3]	The measured 3-phase grid voltage (after a sensor).
	Ig[L1,L2,L3]	The measured 3-phase grid current (after a sensor).
	Theta (rad)	The phase angle of the grid voltage from a PLL.
	Pg_ctl	The active power control input for the controller.
	Qg_ctl	The reactive power control input for the controller.
Output pins:	d	The direct axis control output to the converter.
	q	The quadrature axis control output to the converter.

Dialog properties:

The 3-phase grid-tie controller average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Nominal power to be fed into the grid (kVA):
Enter the nominal power to be fed into the grid (power rating of the grid converter).

Grid voltage 3-phase input sensor gain:
Enter the gain of the input voltage sensor to the Vg pin.

Grid current 3-phase input sensor gain:
Enter the gain of the input current sensor to the Ig pin.

Grid voltage Phase rotation:
Select if the phase rotation of the input signal is clockwise or anti-clockwise.

Grid d-component PI regulator Proportional gain:
Enter the value of the proportional gain of the internal PI compensator.

Grid d-component PI regulator Integral gain:
Enter the value of the integral gain of the internal PI compensator.

Grid d-component PI regulator internal low limit:
Enter the value of the internal low limit of the compensator.

Grid d-component PI regulator internal high limit:
Enter the value of the internal high limit of the compensator.

Grid d-component PI regulator output low limit:
Enter the value of the output low limit of the compensator.

Grid d-component PI regulator output high limit:
Enter the value of the output high limit of the compensator.

Grid d-component PI regulator initial / reset value:
Enter the initial and reset value of the PI compensator for the d-axis component..

Grid q-component PI regulator Proportional gain:
Enter the value of the proportional gain of the internal PI compensator.

Grid q-component PI regulator Integral gain:
Enter the value of the integral gain of the internal PI compensator.

Grid q-component PI regulator internal low limit:
Enter the value of the internal low limit of the compensator.

Grid q-component PI regulator internal high limit:
Enter the value of the internal high limit of the compensator.

Grid q-component PI regulator output low limit:
Enter the value of the output low limit of the compensator.

Grid q-component PI regulator output high limit:
Enter the value of the output high limit of the compensator.

Grid q-component PI regulator initial / reset value:
Enter the initial and reset value of the PI compensator for the q-axis component..

Contents – Real-time

Average Models – Support Blocks

The support blocks provide various blocks to assist in developing control loops for real-time simulation diagrams.



Generic Sensor (1-phase)

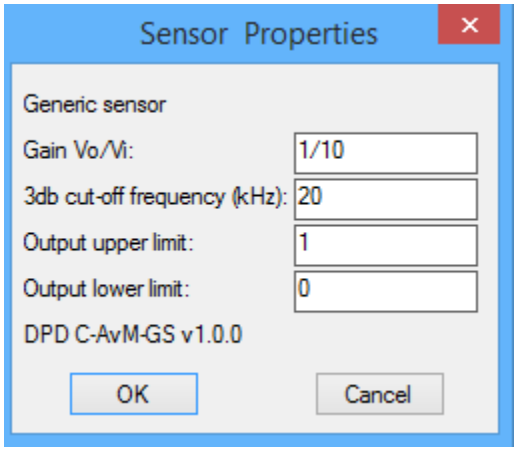
A model of a typical sensor used in digital power applications.

Input pins: **Vi** Input Voltage (V) or other parameter.

Output pins: **Vo** The output voltage (V) or other parameter.

Dialog properties:

The generic sensor average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Gain Vo/Vi:

Enter the value of the DC sensor gain.

3dB cut-off frequency:

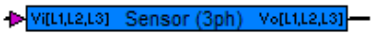
Enter the value of the 3dB cut-off frequency of the sensor.

Output upper limit:

Enter the value of the output high limit of the sensor.

Output lower limit:

Enter the value of the output low limit of the sensor.



Generic Sensor (3-phase)

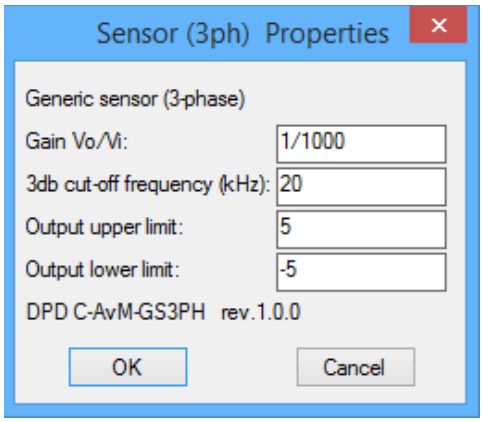
A model of a typical sensor used in digital power applications.

Input pins: **Vi[L1,L2,L3]** Input Voltage (V) or other parameter.

Output pins: **Vo[L1,L2,L3]** The output voltage (V) or other parameter.

Dialog properties:

The 3-phase generic sensor average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Gain Vo/Vi:

Enter the value of the DC sensor gain.

3dB cut-off frequency:

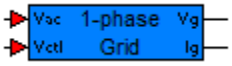
Enter the value of the 3dB cut-off frequency of the sensor.

Output upper limit:

Enter the value of the output high limit of the sensor.

Output lower limit:

Enter the value of the output low limit of the sensor.



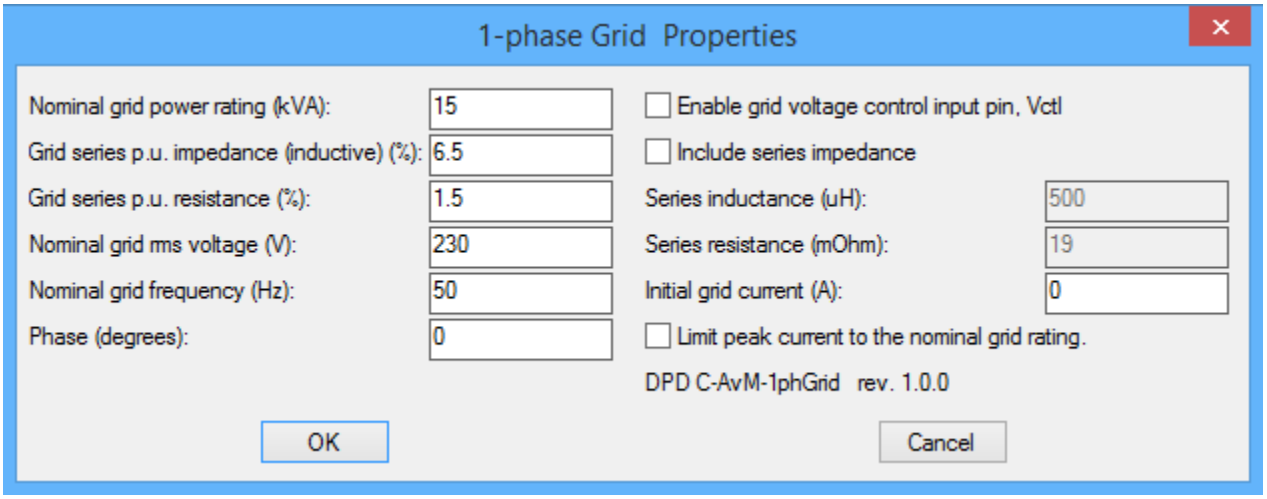
Grid (1-phase)

A model of a single-phase AC grid supply with grid impedance.

Input pins:	**Vac**	Input Voltage (V) of any connection to the grid.
	Vctl	Optional control input to control the grid source voltage from -1 to 1.
Output pins:	**Vg**	The output source voltage (V) of the grid.
	Ig	The grid current output (A).

Dialog properties:

The 1-phase grid average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Nominal Grid power rating (kVA):

Enter the nominal power rating of the grid in kVA.

Grid series p.u. impedance (inductive):

Enter the grid supply series inductive impedance in per unit terms given as a percentage.

Grid series p.u. resistance:

Enter the grid supply series resistance in per unit terms given as a percentage.

Nominal grid rms voltage:

Enter the nominal rms voltage of the grid in volts.

Nominal grid frequency:

Enter the nominal grid supply frequency in Hertz.

Phase degrees:

Enter the initial phase of the grid supply.

Enable grid voltage control input:

Select this to enable the grid voltage to be controlled at the input pin Vctl. In this way, varying or distorted grid supplies can be simulated.

Include series impedance:

Select this to include an RL series impedance to the grid supply. This can also model the impedance of cabling.

Series inductance:

Enter the value of the series inductance in micro-Henrys.

Series resistance:

Enter the value of the series resistance in milli-ohms.

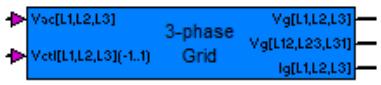
Initial grid current:

Enter the value of the initial current of the grid.

Limit peak current to the nominal grid rating:

Select this to limit the currents flowing through the grid to the nominal rating.

Contents – Real-time



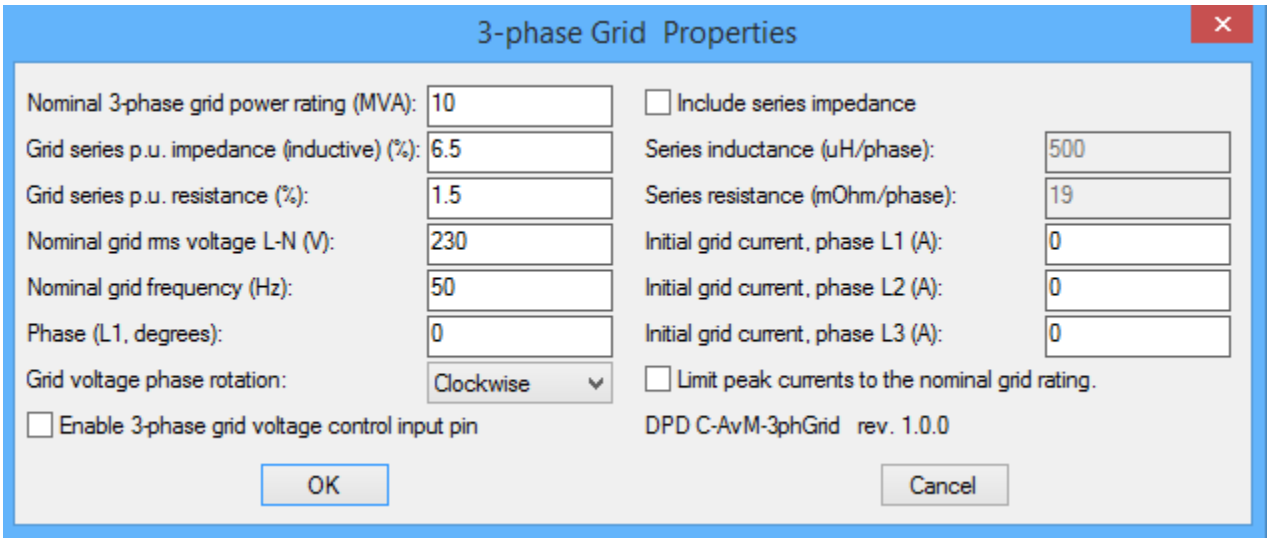
Grid (3-phase)

A model of a three-phase AC grid.

Input pins:	**Vac[L1,L2,L3]**	Input Voltage (V) of any connection to the grid.
	Vctl[L1,L2,L3]	Optional control input to control the grid source voltage (-1..1).
Output pins:	**Vg[L1,L2,L3]**	The output line-neutral source voltage (V) of the grid.
	Vg[L12,L23,L31]	The output line-line source voltage (V) of the grid.
	Ig[L1,L2,L3]	The 3-phase grid current output (A).

Dialog properties:

The 3-phase grid average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Nominal Grid power rating (MVA):

Enter the nominal power rating of the grid in MVA.

Grid series p.u. impedance (inductive):

Enter the grid supply series inductive impedance in per unit terms given as a percentage.

Grid series p.u. resistance:

Enter the grid supply series resistance in per unit terms given as a percentage.

Nominal grid rms voltage:

Enter the nominal rms line-neutral voltage of the grid in volts.

Nominal grid frequency:

Enter the nominal grid supply frequency in Hertz.

Phase degrees, L1:

Enter the initial phase of the L1 phase voltage of the grid supply.

Grid voltage phase rotation:

Select between clockwise and anti-clockwise rotation of the output phases.

Enable 3-phase grid voltage control input:

Select this to enable the grid voltage to be controlled at the input pin Vctl. In this way, varying, unbalanced or distorted grid supplies can be simulated.

Include series impedance:

Select this to include an RL series impedance to the grid supply. This can also model the impedance of cabling.

Series inductance:

Enter the value of the series inductance in micro-Henrys / phase.

Series resistance:

Enter the value of the series resistance in milli-ohms / phase.

Initial grid current. L1, L2, L3:

Enter the value of the initial current of the grid for each of the 3 phases.

Limit peak current to the nominal grid rating:

Select this to limit the currents flowing through the grid to the nominal rating.



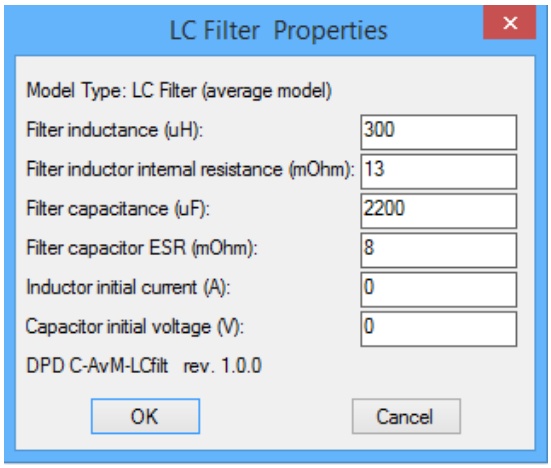
LC filter (1-phase)

A code-generable model of the LC filter.

Input pins:	**Vin**	Input Voltage (V) to the filter..
	Io	The filter output current input (A) into the model.
Output pins:	**Vo**	The output voltage (V) of the filter.
	Iin	The input current (A) of the filter.
	iC	The filter capacitor current (A).

Dialog properties:

The LC Filter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Filter inductance:

Enter the value of the filter inductance in micro-Henrys.

Filter inductor internal resistance:

Enter the value of the internal resistance of the filter inductor in milli-ohms.

Filter capacitance:

Enter the value of the filter capacitance in micro-Farads.

Filter capacitor internal resistance:

Enter the value of the internal resistance of the filter capacitor in milli-ohms.

Inductor initial current:

Enter the value of the initial current of the filter inductor in amperes.

Capacitor initial voltage:

Enter the value of the initial voltage of the filter capacitor in volts.



LCL filter (1-phase)

A code-generable model of the LCL filter.

Input pins: **Vin** Input Voltage (V) to the filter..

Vo The output voltage (V) of the filter input to the model.

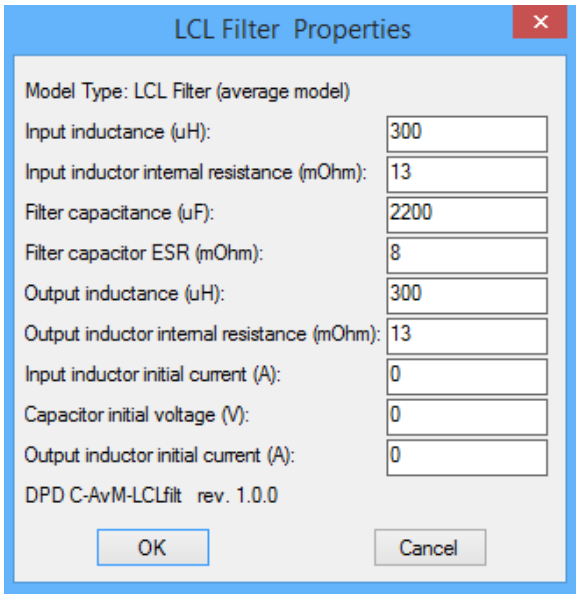
Output pins: **Io** The filter output current input (A).

Iin The input current (A) of the filter.

iC The filter capacitor current (A).

Dialog properties:

The LCL Filter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Filter inductance:

Enter the value of the filter inductance in micro-Henrys.

Filter inductor internal resistance:

Enter the value of the internal resistance of the filter inductor in milli-ohms.

Filter capacitance:

Enter the value of the filter capacitance in micro-Farads.

Filter capacitor internal resistance:

Enter the value of the internal resistance of the filter capacitor in milli-ohms.

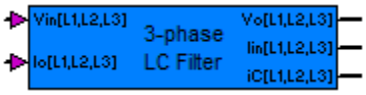
Inductor initial current:

Enter the value of the initial current of the filter inductor in amperes.

Capacitor initial voltage:

Enter the value of the initial voltage of the filter capacitor in volts.

Contents – Real-time



LC filter (3-phase)

A code-generable model of the 3-phase LC filter.

Input pins: **Vin[L1,L2,L3]** Input 3-phase line-neutral voltage (V) to the filter..

Io[L1,L2,L3] The 3-phase filter output current input (A) into the model.

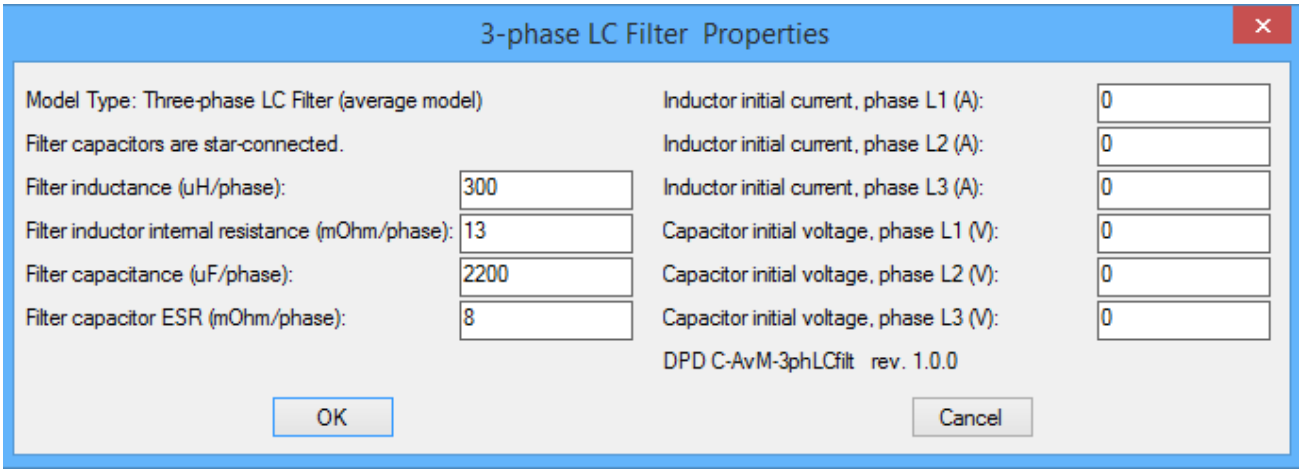
Output pins: **Vo[L1,L2,L3]** The 3-phase output voltage (V) of the filter.

Iin[L1,L2,L3] The 3-phase input current (A) of the filter.

iC[L1,L2,L3] The 3-phase filter capacitor current (A).

Dialog properties:

The 3-phase LC Filter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Filter inductance:

Enter the value of the filter inductance in micro-Henrys.

Filter inductor internal resistance:

Enter the value of the internal resistance of the filter inductor in milli-ohms.

Filter capacitance:

Enter the value of the filter capacitance in micro-Farads.

Filter capacitor internal resistance:

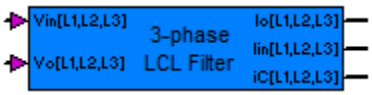
Enter the value of the internal resistance of the filter capacitor in milli-ohms.

Inductor initial current L1, L2, L3:

Enter the value of the initial current of each phase of the filter inductor in amperes.

Capacitor initial voltage L1, L2, L3:

Enter the value of the initial voltage of each phase of the filter capacitor in volts.



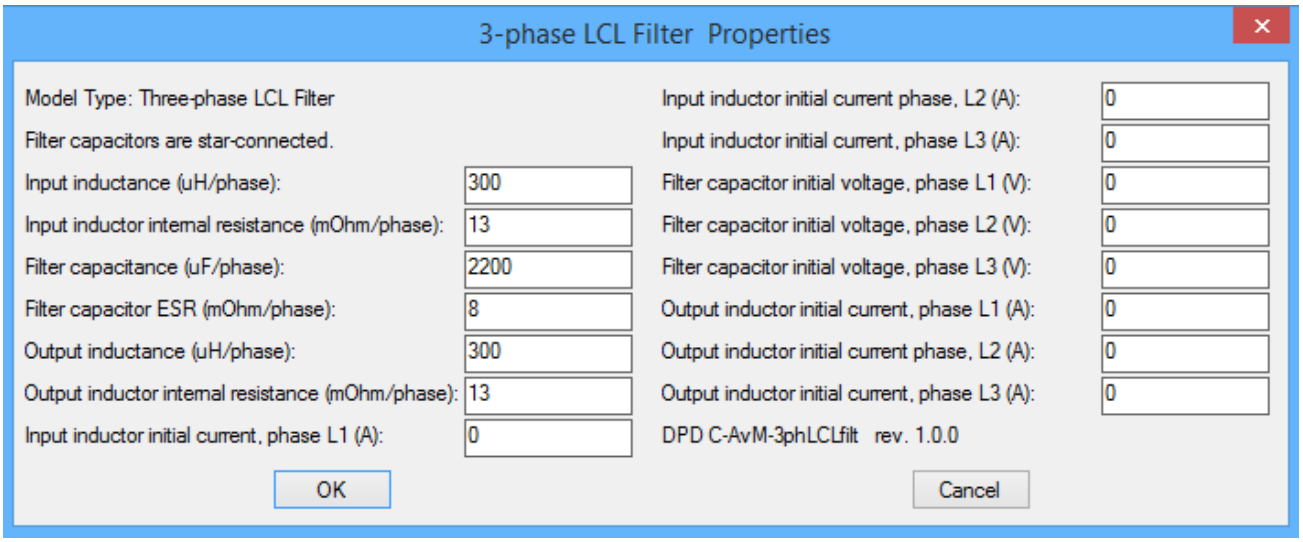
LCL filter (3-phase)

A code-generable model of the 3-phase LCL filter.

Input pins:	**Vin[L1,L2,L3]**	Input 3-phase voltage (V) to the filter..
	Vo[L1,L2,L3]	The 3-phase filter output voltage input (V) into the model.
Output pins:	**Io**	The 3-phase output current (A) of the filter.
	Iin	The 3-phase input current (A) of the filter.
	iC	The 3-phase filter capacitor current (A).

Dialog properties:

The 3-phase LCL Filter average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Filter inductance:

Enter the value of the filter inductance in micro-Henrys.

Filter inductor internal resistance:

Enter the value of the internal resistance of the filter inductor in milli-ohms.

Filter capacitance:

Enter the value of the filter capacitance in micro-Farads.

Filter capacitor internal resistance:

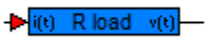
Enter the value of the internal resistance of the filter capacitor in milli-ohms.

Inductor initial current L1, L2, L3:

Enter the value of the initial current of each phase of the filter inductor in amperes.

Capacitor initial voltage L1, L2, L3:

Enter the value of the initial voltage of each phase of the filter capacitor in volts.



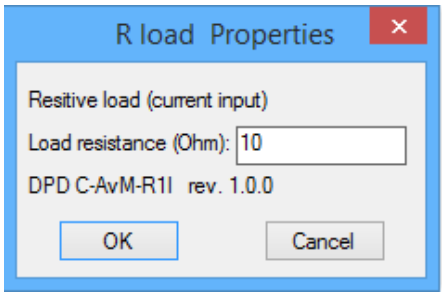
Resistive load (1-phase, Current input)

Input pins: **i(t)** Input current (A) into the load.

Output pins: **v(t)** The output voltage (V) across the load resistance.

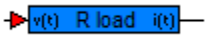
Dialog properties:

The resistive load average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Load resistance:

Enter the value of the load resistance in Ohms.



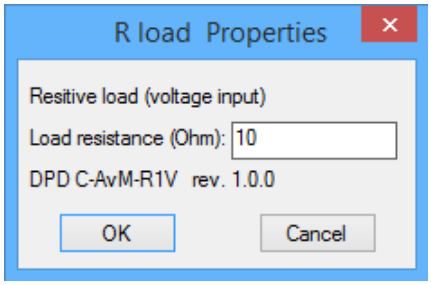
Resistive load (1-phase, Voltage input)

Input pins: **v(t)** The voltage (V) across the load resistance.

Output pins: **i(t)** The resistive load current output (A).

Dialog properties:

The resistive load average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Load resistance:

Enter the value of the load resistance in Ohms.



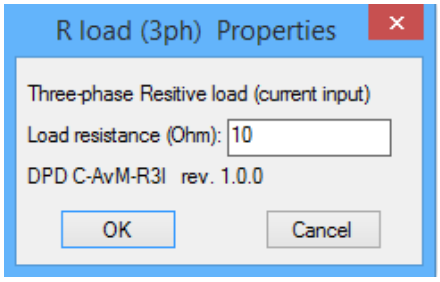
Resistive load (3-phase, Current input)

Input pins: **i[L1,L2,L3]** Input 3-phase current (A) into the load.

Output pins: **v[L1,L2,L3]** The output 3-phase voltage (V) across the load resistance.

Dialog properties:

The 3-phase resistive load average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Load resistance:

Enter the value of the load resistance in Ohms.



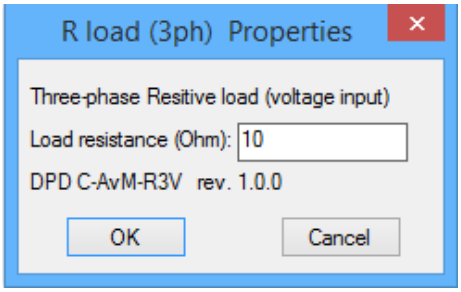
Resistive load (3-phase, Voltage input)

Input pins: **v[L1,L2,L3]** The 3-phase voltage (V) across the load resistance.

Output pins: i**[L1,L2,L3]** The 3-phase resistive load current (A) output.

Dialog properties:

The 3-phase resistive load average model block properties menu is shown in the following figure which appears when right-clicking on the block.



Load resistance:

Enter the value of the load resistance in Ohms.

Contents – Real-time

Chapter 5 – Tools

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[Main Contents]

Block Reference - Tools

The tools section of Embed/Digital Power Designer consists of a series of tools which can be used by analog designers to directly convert familiar analog circuits into digital filters and compensators.

The blocks in this section are therefore designed to be tools to assist in the development of digital power control algorithms. The blocks can also be used together with blocks from the simulation section to create simulation diagrams.

The tools in this section can also be used to convert between various formats of the coefficients e.g. from analog to digital or from PID gains to poles and zeros etc.

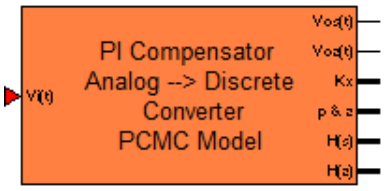
Frequency analysis tools are also available as described in this chapter.

Block Convention

The blocks within the tools environment are colour-coded in orange in order to distinguish them from simulation and code-generable blocks. In general, bitmaps are used with an orange background. The blocks can be customized if so desired by CTL + right clicking on the block to bring up the compound block properties dialog.

The blocks in this section are designed to be used as tools and are not code-generable.

Analog Converters - Compensators

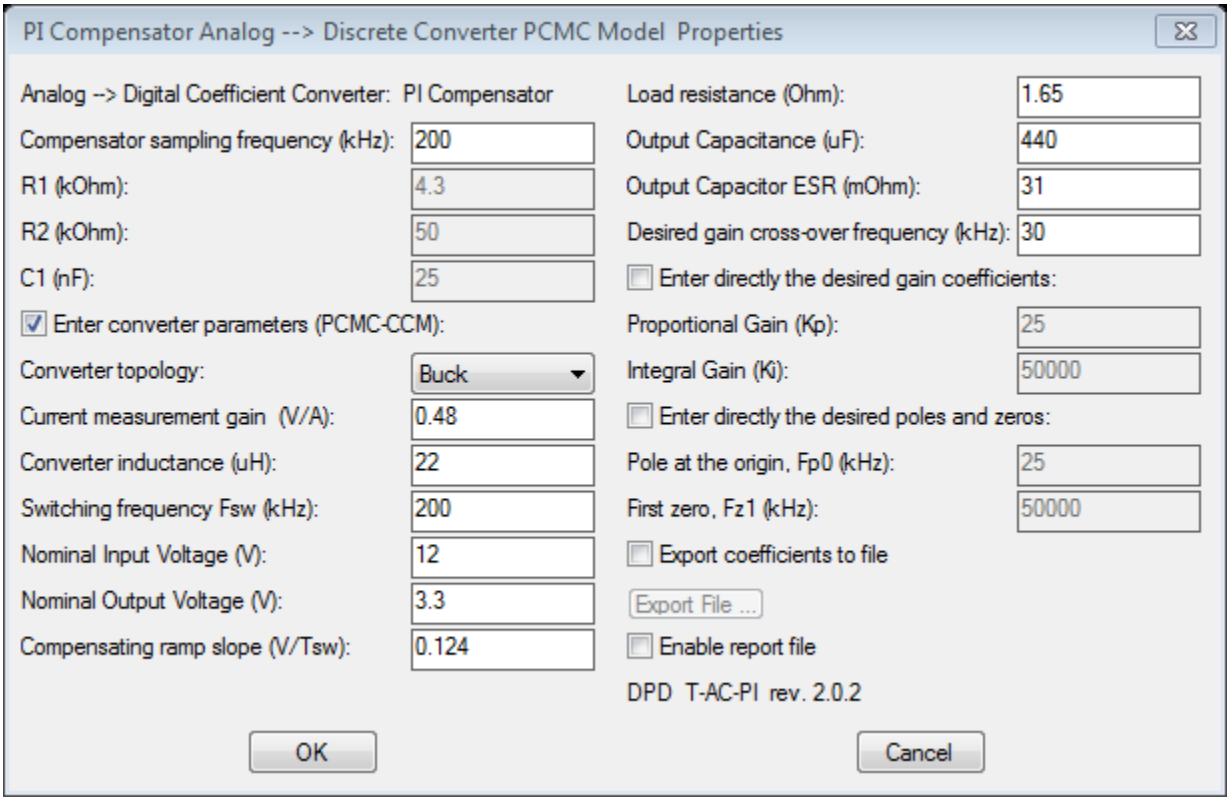


PI Compensator

Input pins:	**Vi(t)**	Input signal (optional)
Output pins:	**Vo(s)**	Vout (s-domain or continuous) which can be used in simulation.
	Vo(z)	Vout (z-domain or discrete) which can be used in simulation
	Kx	The gain coefficients output display (struct).
	p&z	Equivalent poles and zeros output display (struct).
	H(s)	Compensator coefficients in the s-domain (struct).
	H(z)	Compensator coefficients in the z-domain (struct).

Dialog properties:

The PI compensator block properties menu is shown in the following figure which appears when right-clicking on the block.



Compensator sampling frequency:

Enter the value of the sampling frequency (for a digital filter using z-coefficients).

R1:

Enter the value of the block circuit schematic resistance R1 in kilo-Ohms.

R2:

Enter the value of the block circuit schematic resistance R2 in kilo-Ohms

C1:

Enter the value of the block circuit schematic resistance C1 in nano-Farads

Enter converter parameters (PCMC-CCM):

Select this check box if you choose to calculate the required coefficients using parameters based upon the converter power stage design. The parameters will be valid for Peak current mode control (PCMC) in continuous conduction mode (CCM).

Converter Topology:

The choices here are:

1. Buck
2. Boost
3. Buck-boost

For other topologies, one of the above choices can be used. For example, for a half-bridge, full-bridge, push-pull or forward topology, the buck topology can be selected. For a flyback topology, the buck-boost topology can be selected here.

Current Measurement gain:

Enter the gain of the current measurement network (sensor) in V/A.

Converter Inductance:

Insert the value of the converter inductance in micro-Henries.

Switching Frequency, Fsw:

Insert the converter switching frequency in kHz.

Nominal Input Voltage:

Enter the nominal input voltage of the converter in Volts.

Nominal Output Voltage:

Enter the nominal output voltage of the converter in Volts.

Compensating Ramp Slope:

Enter the desired value of the slope compensation ramp in V / switching period.

Load Resistance:

Insert the value of the nominal load resistance in Ohms.

Output Capacitance:

Insert the value of the output capacitance in microfarads.

Output Capacitor ESR:

Insert the value of the output capacitor equivalent series resistance (ESR) in Ohms.

Desired gain cross-over frequency:

Enter the value of the desired gain cross-over frequency (bandwidth of the control loop) in kHz.

Enter directly the desired gain coefficients:

Check this box if the previous input parameters are to be ignored and enter directly the gain parameters as below.

Proportional gain, Kp:

Enter the value of the proportional gain.

Integral gain, Ki:

Enter the value of the integral gain.

Enter directly the desired poles and zeros:

Check this box if the previous input parameters and gain coefficients are to be ignored and enter directly the poles and zeros as below.

Pole at the origin, Fp0:

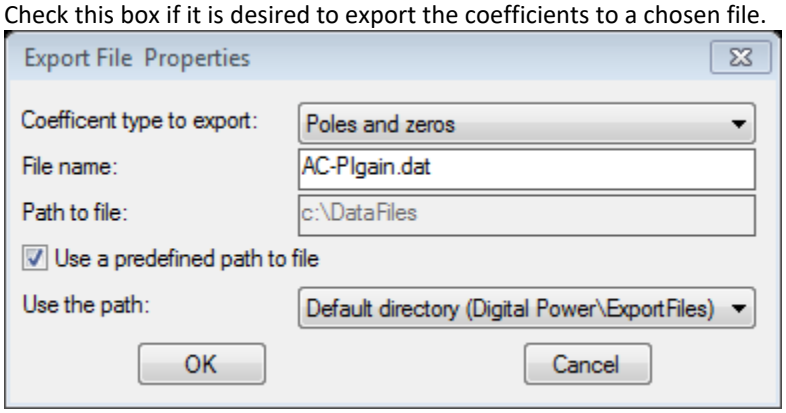
Enter the value of the pole of the first-order transfer function (at the origin).

First zero, Fz1:

Enter the value of the zero of the transfer function.

Export coefficients to file:

Check this box if it is desired to export the coefficients to a chosen file.



Coefficient type to export:

Select the type of coefficients to export. The available selection is:

1. Poles and zeros
2. PI gains
3. S-coefficients
4. Z-coefficients

Export file name:

Enter the full file name of the export file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

Select this if the file is located in one of the pre-defined paths.

Use the path:

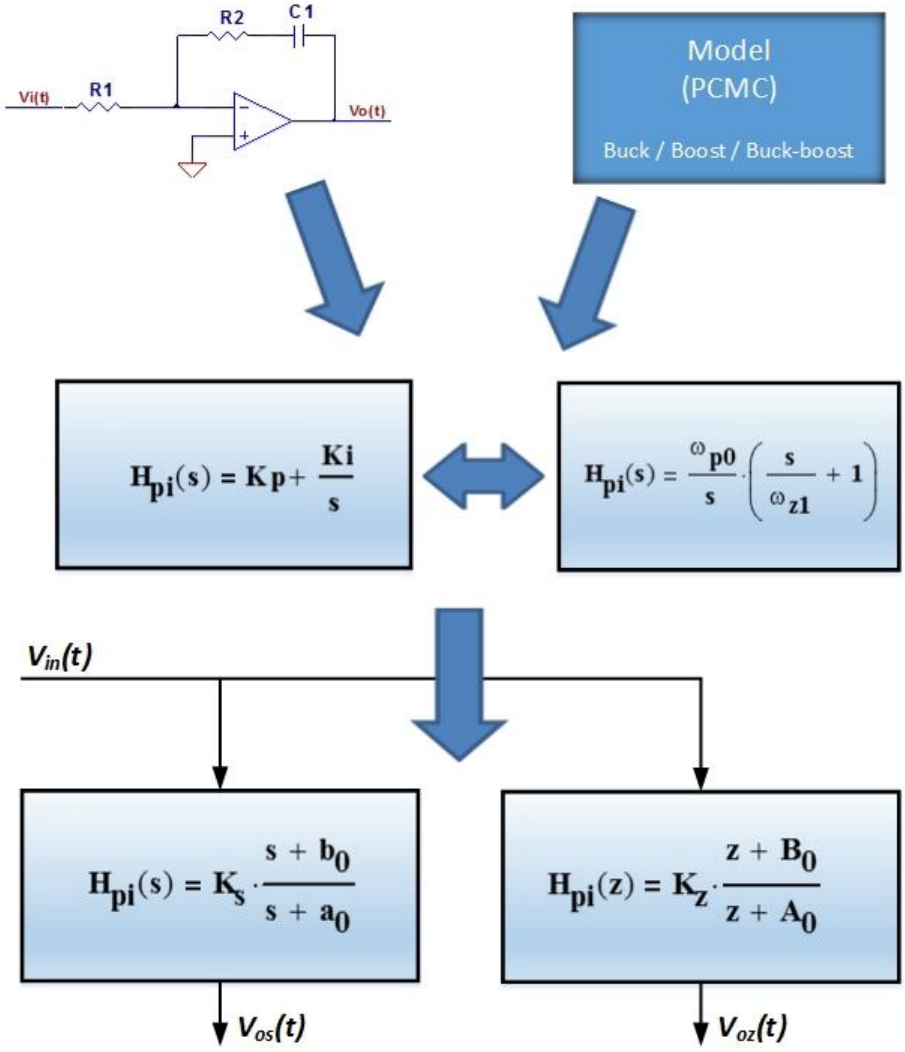
The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

Enable report file:

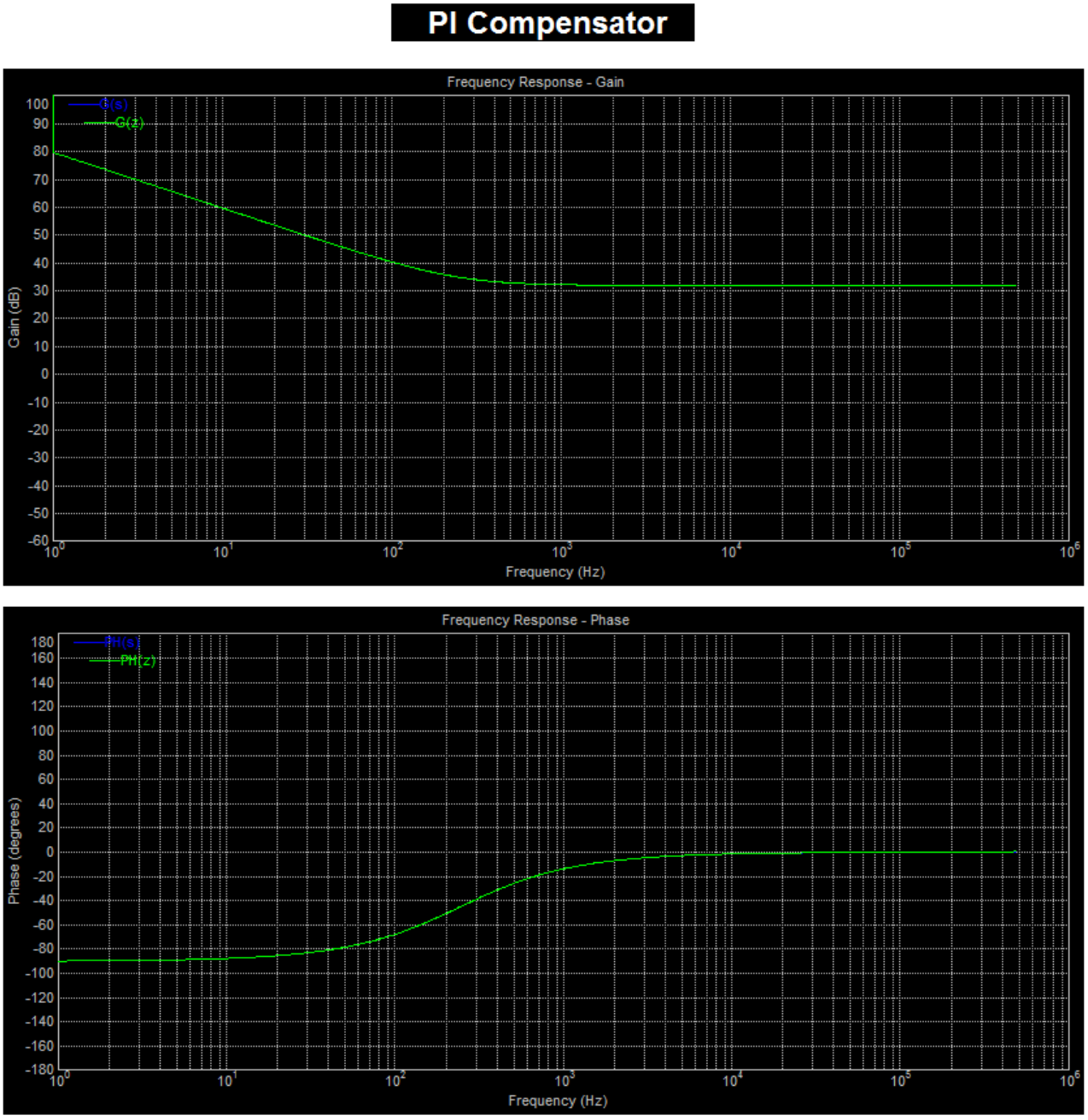
Select this option if a text report file is desired which will be saved in the same directory as this diagram.

The following figure shows the flow of converting the coefficients within the PI tool. The coefficients can be generated from the analog circuit component values. The model is based upon peak current-mode control and can create the required PI coefficients from that model as a first pass in the compensator design.

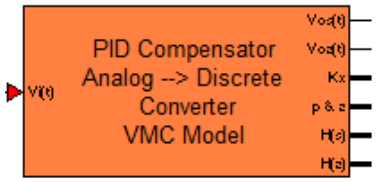


The block can also be used in simulation with one time-dependent input and two time dependent outputs; one using the compensator in the analog domain, the other in the discrete domain.

The frequency response of the PI tool is given in the following diagram which shows a comparison of the analog compensator response in blue with the discrete compensator response in green, using the internally generated bilinear (Tustin) transformed coefficients.



Contents - Tools

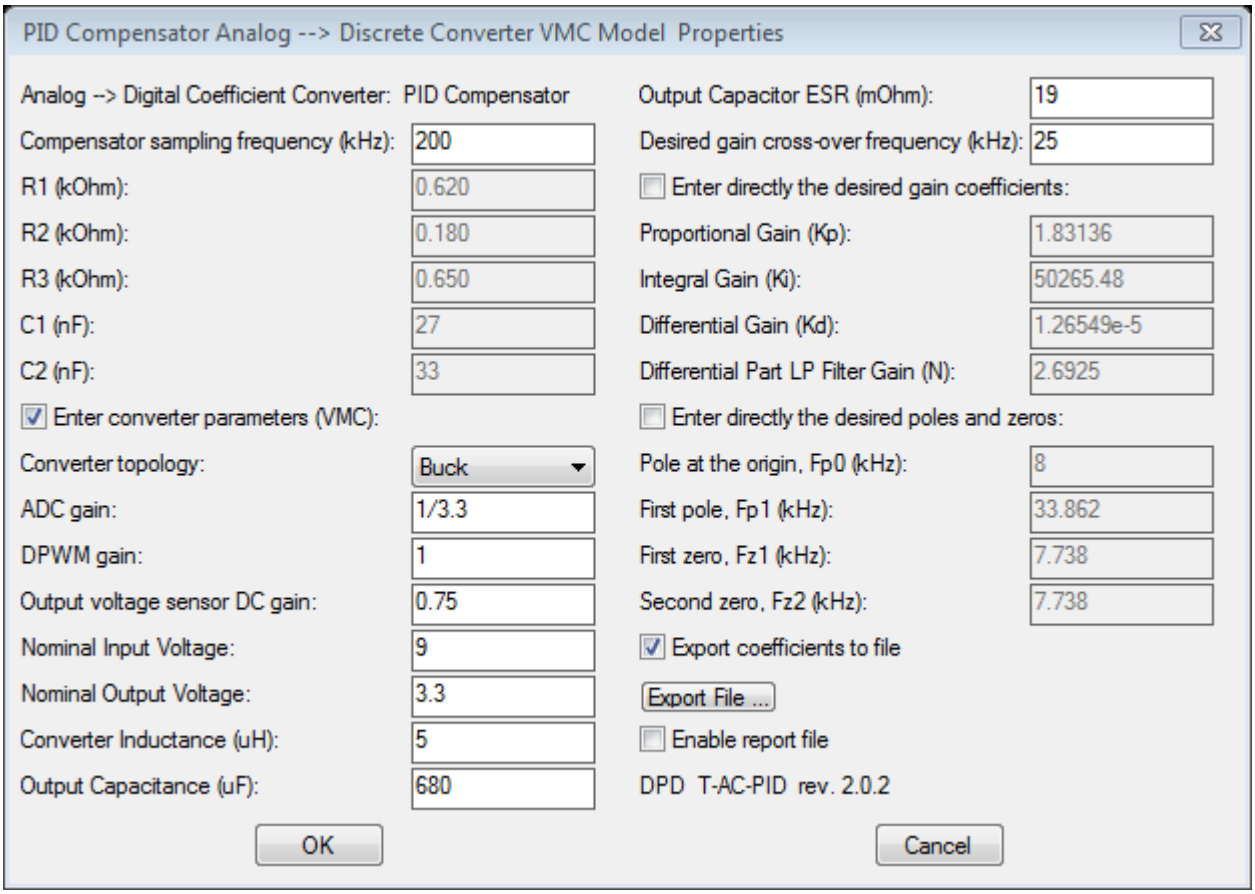


PID Compensator (2p2z)

Input pins:	**Vi(t)**	Input signal (optional)
Output pins:	**Vo(s)**	Vout (s-domain or continuous) which can be used in simulation.
	Vo(z)	Vout (z-domain or discrete) which can be used in simulation
	Kx	The gain coefficients output display (struct).
	p&z	Equivalent poles and zeros output display (struct).
	H(s)	Compensator coefficients in the s-domain (struct).
	H(z)	Compensator coefficients in the z-domain (struct).

Dialog properties:

The PID compensator block properties menu is shown in the following figure which appears when right-clicking on the block.



Compensator sampling frequency:

Enter the value of the sampling frequency (for a digital filter using z-coefficients).

R1:

Enter the value of the block circuit schematic resistance R1 in kilo-Ohms.

R2:

Enter the value of the block circuit schematic resistance R2 in kilo-Ohms.

R3:

Enter the value of the block circuit schematic resistance R3 in kilo-Ohms.

C1:

Enter the value of the block circuit schematic resistance C1 in nano-Farads.

C2:

Enter the value of the block circuit schematic resistance C2 in nano-Farads.

Enter converter parameters (VMC):

Select this check box if you choose to calculate the required coefficients using parameters based upon the converter power stage design. The parameters will be valid for voltage mode control (VMC) in continuous conduction mode (CCM).

Converter Topology:

The choices here are:

1. Buck
2. Boost
3. Buck-boost

For other topologies, one of the above choices can be used. For example, for a half-bridge, full-bridge, push-pull or forward topology, the buck topology can be selected. For a flyback topology, the buck-boost topology can be selected here.

ADC gain:

Enter the gain of the current measurement network (sensor) in V/A.

DPWM gain:

Enter the effective gain of the digital PWM modulator in V/V.

Converter Inductance:

Insert the value of the converter inductance in microHenries.

Switching Frequency, Fsw:

Insert the converter switching frequency in kHz.

Nominal Input Voltage:

Enter the nominal input voltage of the converter in Volts.

Nominal Output Voltage:

Enter the nominal output voltage of the converter in Volts.

Output Capacitance:

Insert the value of the output capacitance in microfarads.

Output Capacitor ESR:

Insert the value of the output capacitor equivalent series resistance (ESR) in Ohms.

Desired gain cross-over frequency:

Enter the value of the desired gain cross-over frequency (bandwidth of the control loop) in kHz.

Enter directly the desired gain coefficients:

Check this box if the previous input parameters are to be ignored and enter directly the gain parameters as below.

Proportional gain, Kp:

Enter the value of the proportional gain.

Integral gain, Ki:

Enter the value of the integral gain.

Differential gain, Kd:

Enter the value of the differential gain.

Differential part LP filter gain, N:

Enter the value of the low-pass filter gain divider of the differential gain.

Enter directly the desired poles and zeros:

Check this box if the previous input parameters are to be ignored and enter directly the poles and zeros of the compensator as below.

Pole at the origin, Fp0:

Enter the value of the pole at the origin of the second-order transfer function.

First pole, Fp1:

Enter the value of the pole of the second order transfer function.

First zero, Fz1:

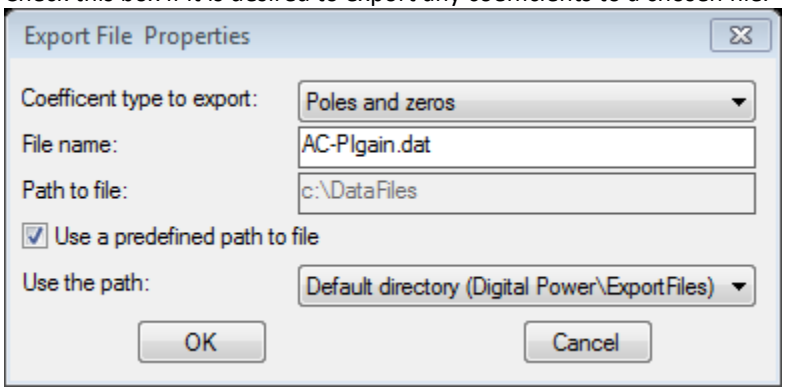
Enter the value of the first zero of the second-order transfer function.

Second zero, Fz2:

Enter the value of the second zero of the second order transfer function.

Export coefficients to file:

Check this box if it is desired to export any coefficients to a chosen file.



Coefficient type to export:

Select the type of coefficients to export. The available selection is:

1. Poles and zeros
2. PID gains
3. S-coefficients
4. Z-coefficients

Export file name:

Enter the full file name of the export file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

Select this if the file is located in one of the pre-defined paths.

Use the path:

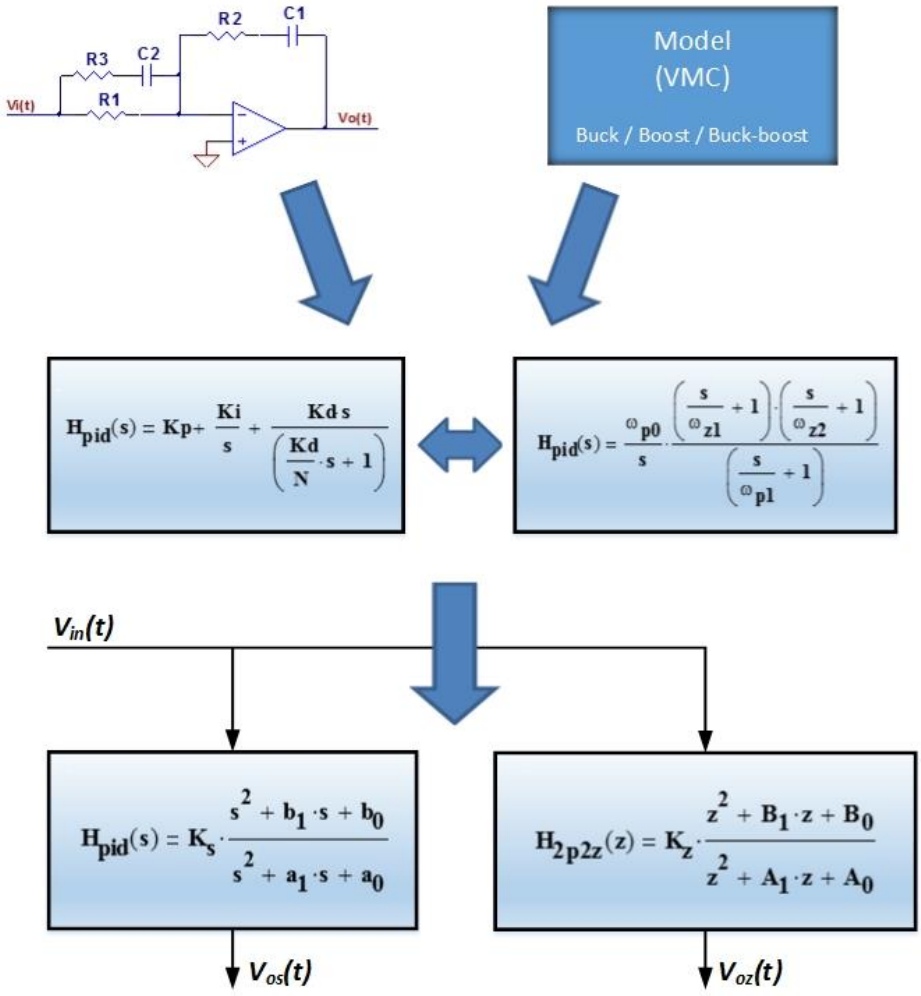
The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

Enable report file:

Select this option if a text report file is desired which will be saved in the same directory as this diagram.

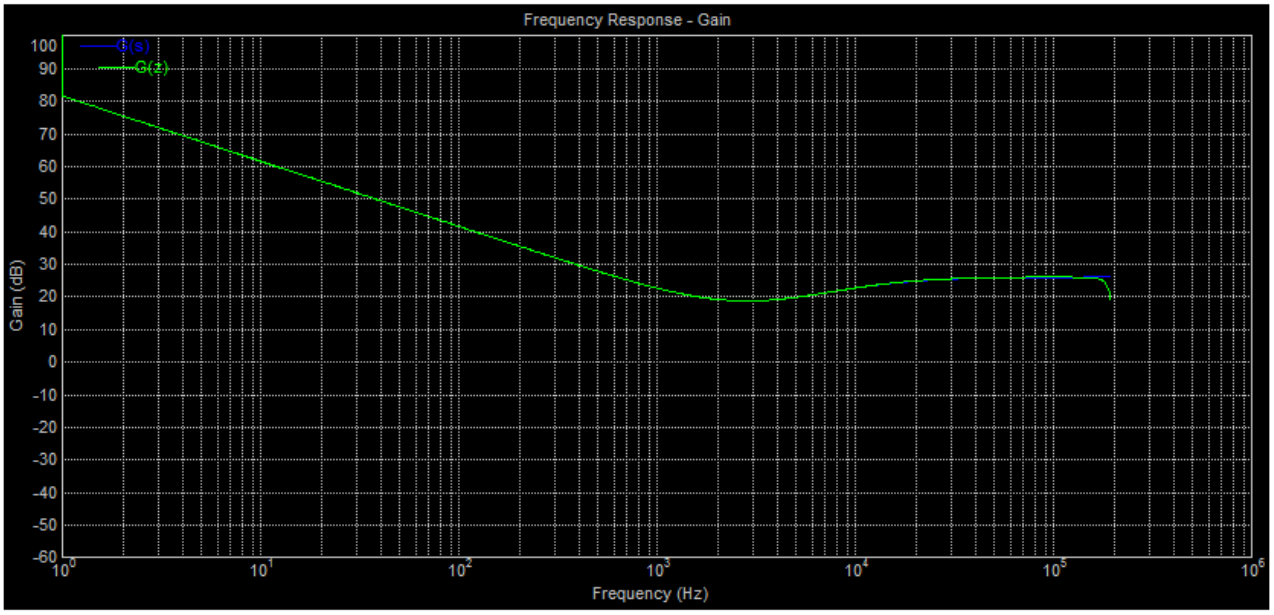
The following figure shows the flow of converting the coefficients within the PID conversion tool. The coefficients can be generated from the analog circuit component values. The model is based upon peak-current mode control and can create the required PID coefficients from that model as a first pass in the compensator design.

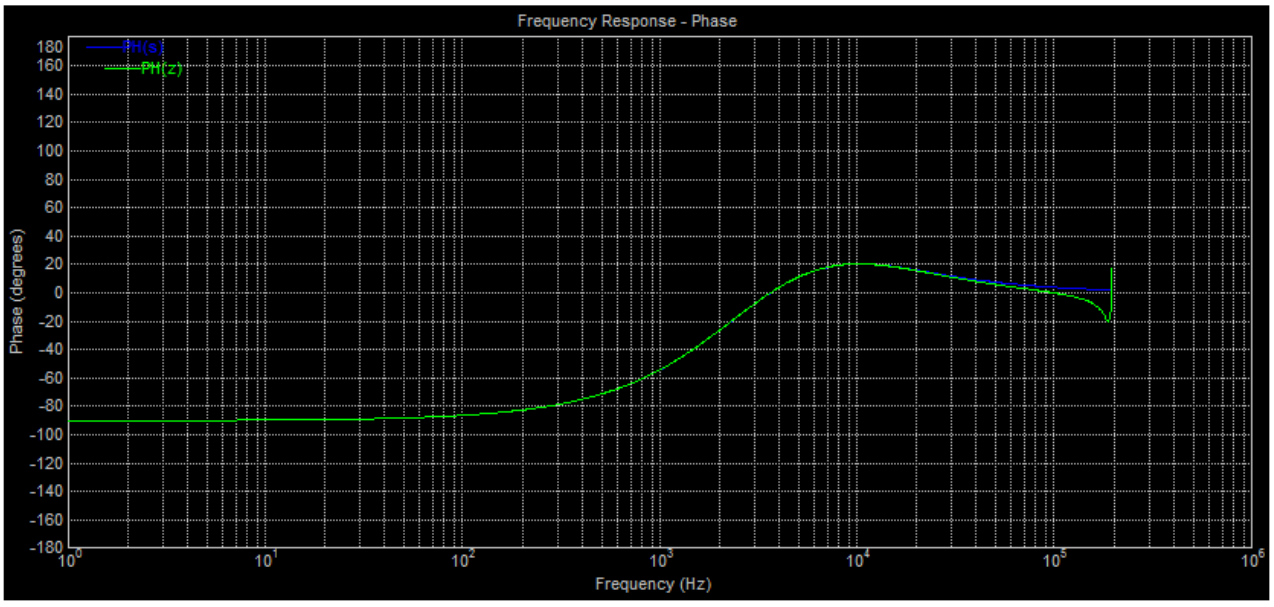


The block can also be used in simulation with one time-dependent input and two time dependent outputs; one using the compensator in the analog domain, the other in the discrete domain.

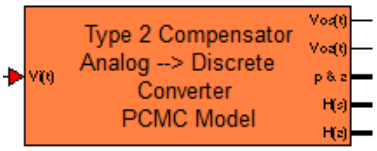
The frequency response of the PID tool (up to the switching frequency) is given in the following diagram which shows a comparison of the analog compensator response in blue with the discrete compensator response in green, using the internally generated bilinear (Tustin) transformed coefficients.

PID (2p2z) Compensator





Contents - Tools

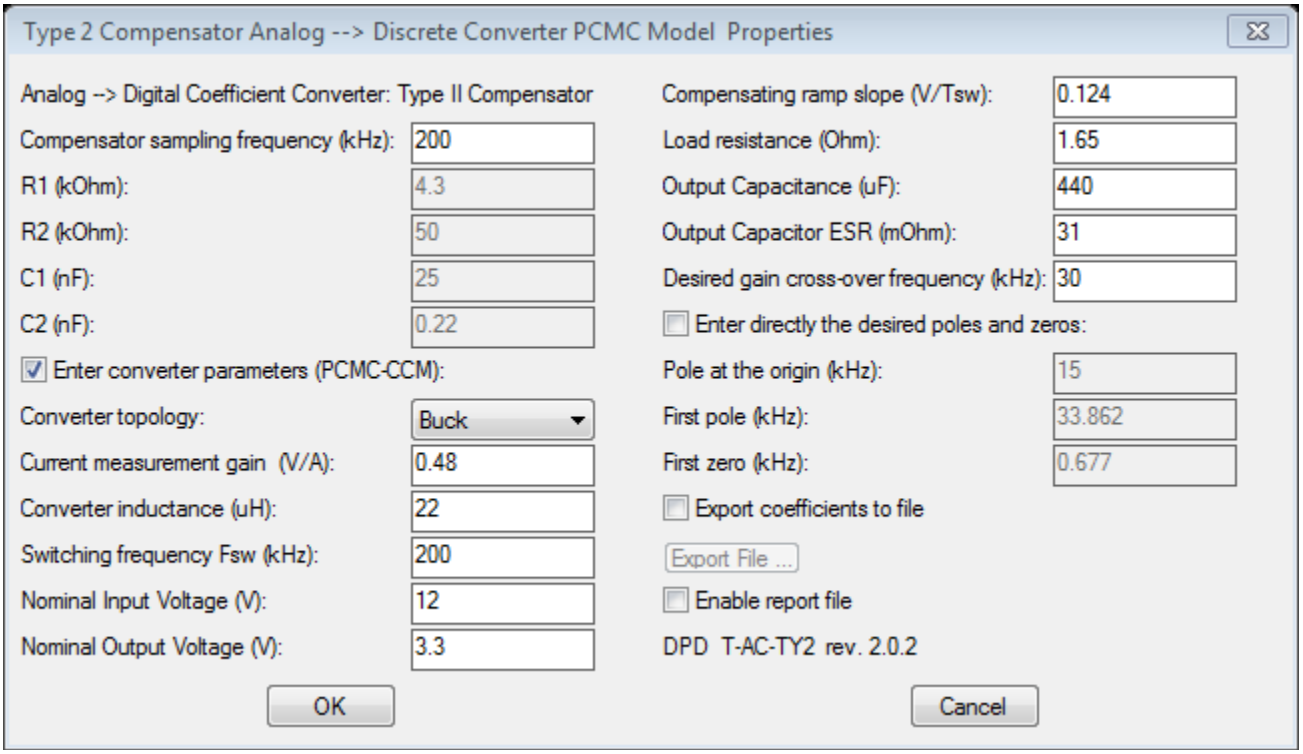


Type II Compensator

Input pins:	**Vi(t)**	Input signal (optional)
Output pins:	**Vo(s)**	Vout (s-domain or continuous) which can be used in simulation.
	Vo(z)	Vout (z-domain or discrete) which can be used in simulation
	Kx	The gain coefficients output display (struct).
	p&z	Equivalent poles and zeros output display (struct).
	H(s)	Compensator coefficients in the s-domain (struct).
	H(z)	Compensator coefficients in the z-domain (struct).

Dialog properties:

The Type II compensator block properties menu is shown in the following figure which appears when right-clicking on the block.



Compensator sampling frequency:

Enter the value of the sampling frequency (for a digital filter using z-coefficients).

R1:

Enter the value of the block circuit schematic resistance R1 in kilo-Ohms.

R2:

Enter the value of the block circuit schematic resistance R2 in kilo-Ohms

C1:

Enter the value of the block circuit schematic resistance C1 in nano-Farads

C2:

Enter the value of the block circuit schematic resistance C2 in nano-Farads

Enter converter parameters (PCMC-CCM):

Select this check box if you choose to calculate the required coefficients using parameters based upon the converter power stage design. The parameters will be valid for Peak current mode control (PCMC) in continuous conduction mode (CCM).

Converter Topology:

The choices here are:

1. Buck
2. Boost
3. Buck-boost

For other topologies, one of the above choices can be used. For example, for a half-bridge, full-bridge, push-pull or forward topology, the buck topology can be selected. For a flyback topology, the buck-boost topology can be selected here.

Current Measurement gain:

Enter the gain of the current measurement network (sensor) in V/A.

Converter Inductance:

Insert the value of the converter inductance in microHenries.

Switching Frequency, Fsw:

Insert the converter switching frequency in kHz.

Nominal Input Voltage:

Enter the nominal input voltage of the converter in Volts.

Nominal Output Voltage:

Enter the nominal output voltage of the converter in Volts.

Compensating Ramp Slope:

Enter the desired value of the slope compensation ramp in V / switching period.

Load Resistance:

Insert the value of the nominal load resistance in Ohms.

Output Capacitance:

Insert the value of the output capacitance in microfarads.

Output Capacitor ESR:

Insert the value of the output capacitor equivalent series resistance (ESR) in Ohms.

Desired gain cross-over frequency:

Enter the value of the desired gain cross-over frequency (bandwidth of the control loop) in kHz.

Enter directly the desired poles and zeros:

Check this box if the previous input parameters are to be ignored and enter directly the poles and zeros as below.

Pole at the origin, Fp0:

Enter the value of the pole at the origin in kHz.

First pole, Fp1:

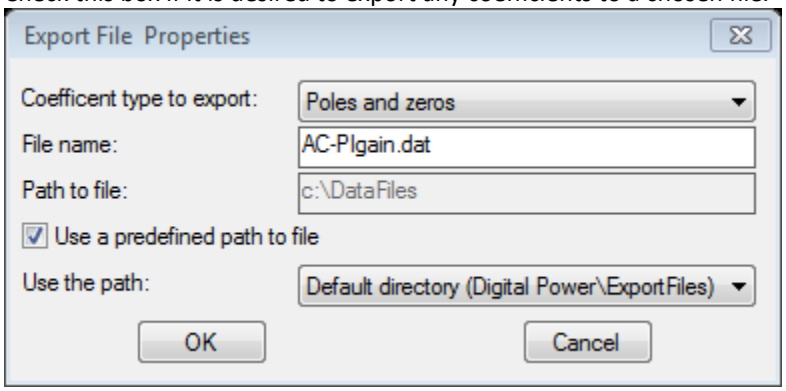
Enter the value of the first pole of the compensator in kHz.

First zero, Fz1:

Enter the value of the first zero of the compensator in kHz.

Export coefficients to file:

Check this box if it is desired to export any coefficients to a chosen file.



Coefficient type to export:

Select the type of coefficients to export. The available selection is:

1. Poles and zeros
2. S-coefficients
3. Z-coefficients

Export file name:

Enter the full file name of the export file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

Select this if the file is located in one of the pre-defined paths.

Use the path:

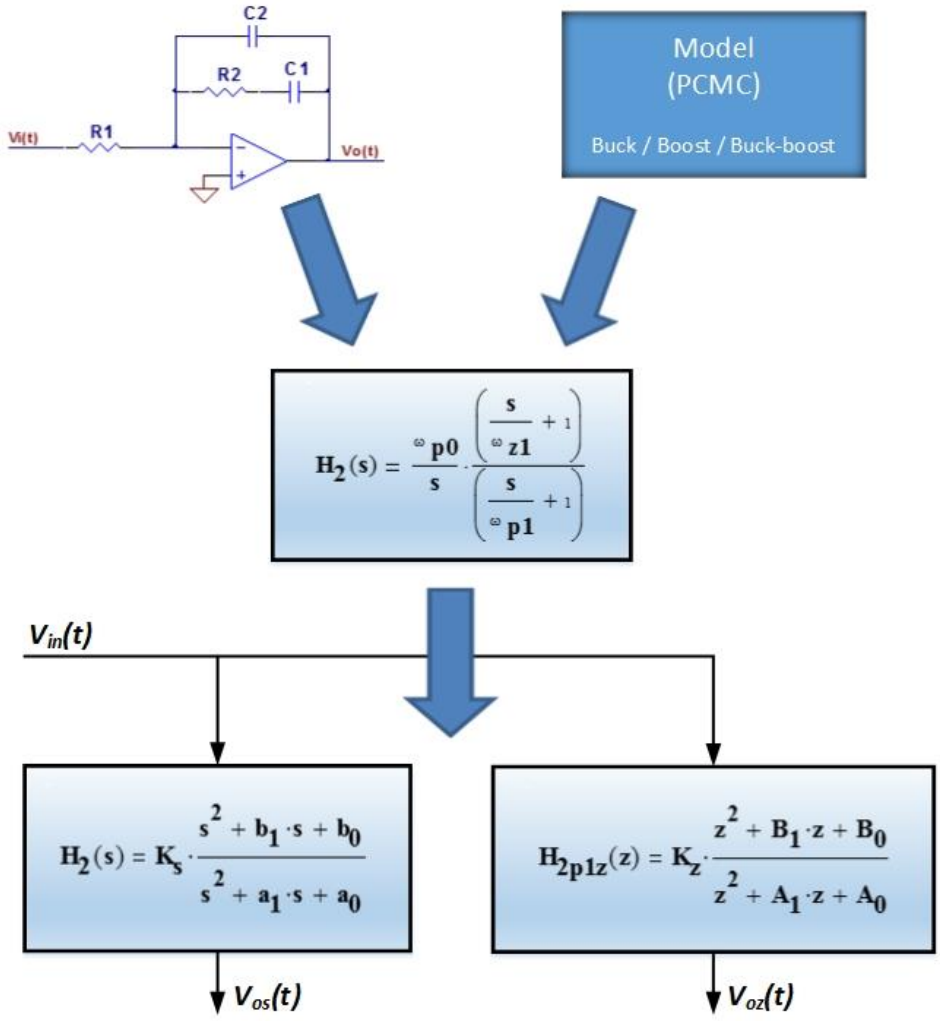
The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

Enable report file:

Select this option if a text report file is desired which will be saved in the same directory as this diagram.

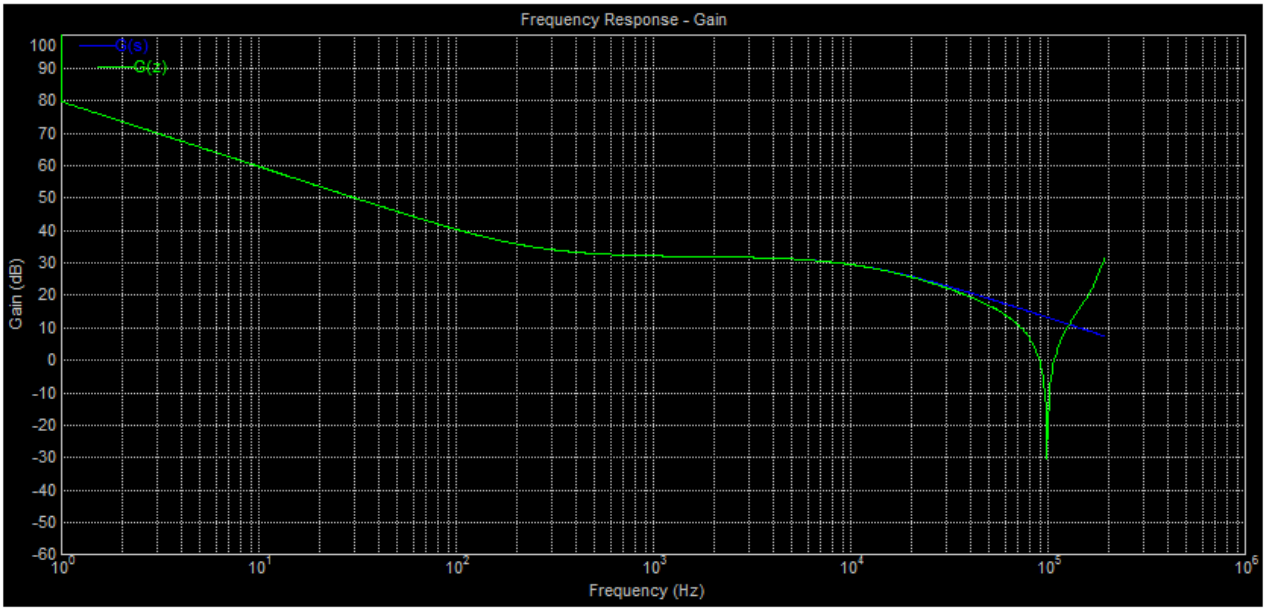
The following figure shows the flow of converting the coefficients within the type 2 compensator conversion tool. The coefficients can be generated from the analog circuit component values. The model is based upon peak current-mode control and can create the required type 2 coefficients from that model as a first pass in the compensator design.

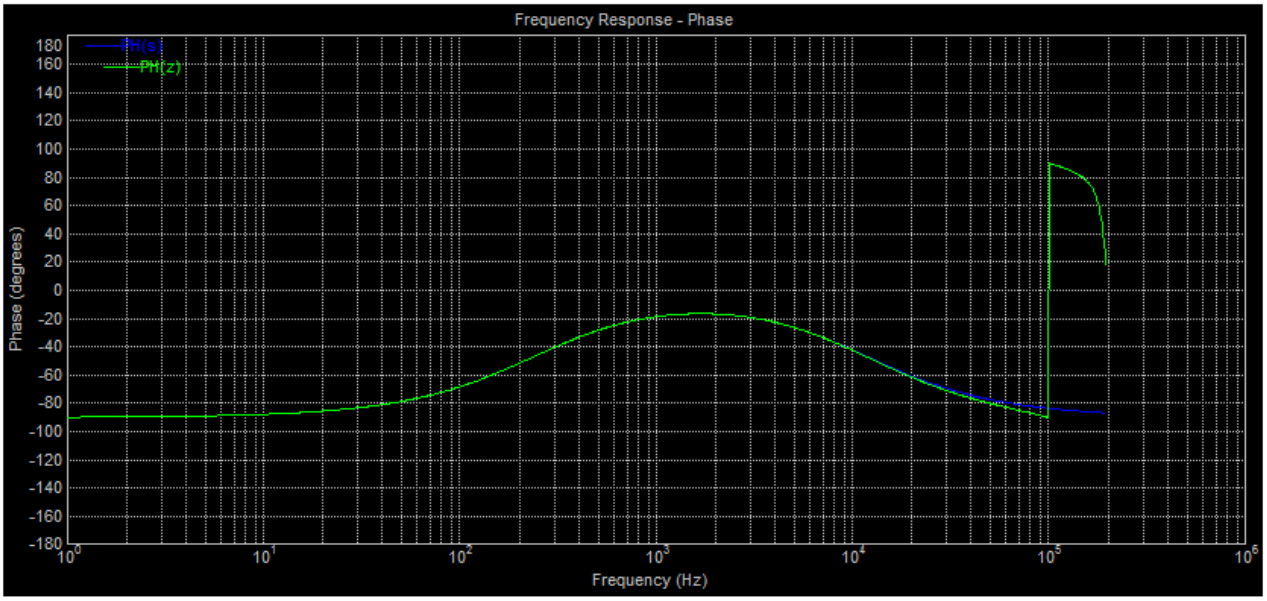


The block can also be used in simulation with one time-dependent input and two time dependent outputs; one using the compensator in the analog domain, the other in the discrete domain.

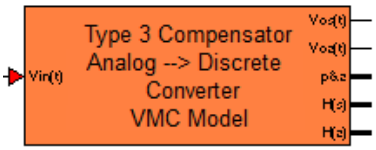
The frequency response of the type 2 compensator tool is given in the following diagram which shows a comparison of the analog compensator response in blue with the discrete compensator response in green, using the internally generated bilinear (Tustin) transformed coefficients.

Type 2 Compensator





Contents - Tools

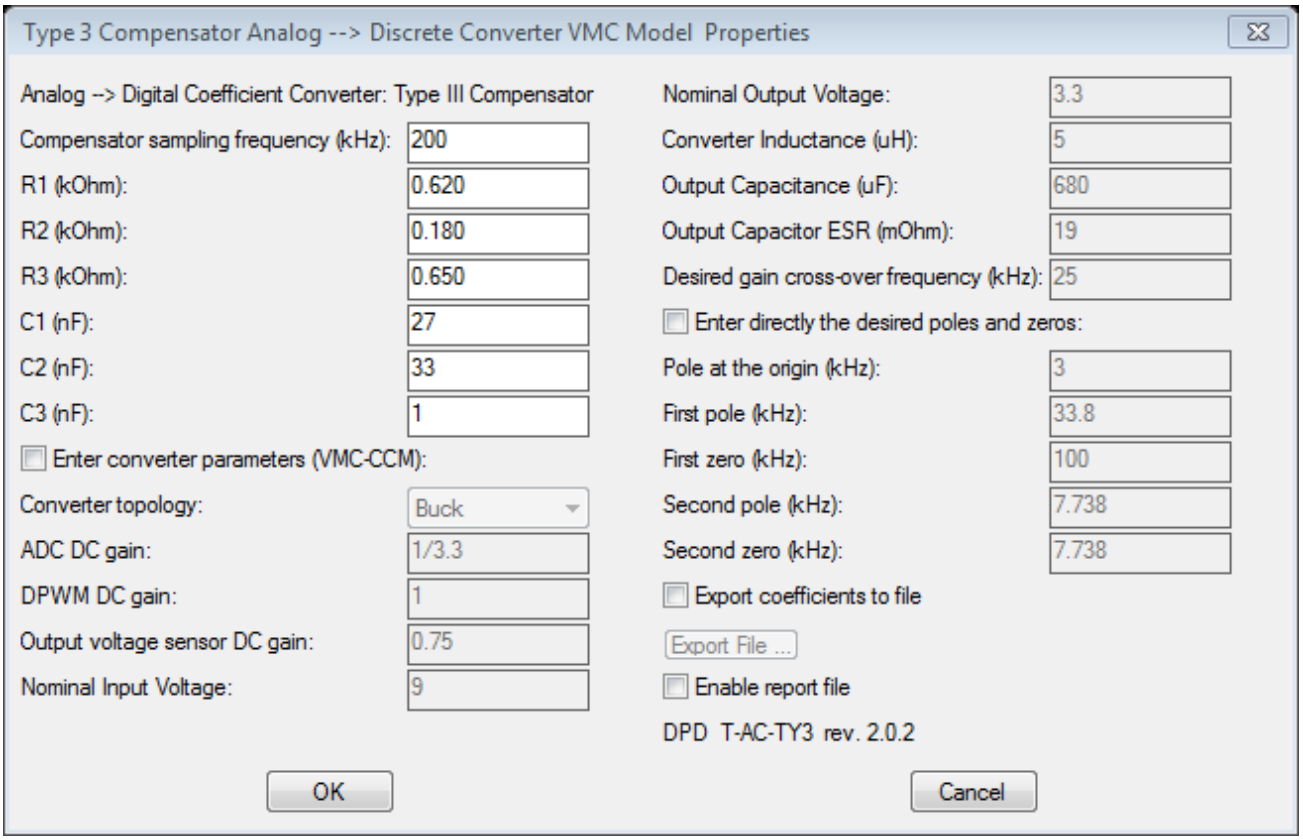


Type III Compensator

Input pins:	**Vi(t)**	Input signal (optional)
Output pins:	**Vo(s)**	Vout (s-domain or continuous) which can be used in simulation.
	Vo(z)	Vout (z-domain or discrete) which can be used in simulation
	Kx	The gain coefficients output display (struct).
	p&z	Equivalent poles and zeros output display (struct).
	H(s)	Compensator coefficients in the s-domain (struct).
	H(z)	Compensator coefficients in the z-domain (struct).

Dialog properties:

The Type III compensator block properties menu is shown in the following figure which appears when right-clicking on the block.



Compensator sampling frequency:

Enter the value of the sampling frequency (for a digital filter using z-coefficients).

R1:

Enter the value of the block circuit schematic resistance R1 in kilo-Ohms.

R2:

Enter the value of the block circuit schematic resistance R2 in kilo-Ohms

R3:

Enter the value of the block circuit schematic resistance R3 in kilo-Ohms

C1:

Enter the value of the block circuit schematic resistance C1 in nano-Farads

C2:

Enter the value of the block circuit schematic resistance C2 in nano-Farads.

C3:

Enter the value of the block circuit schematic resistance C3 in nano-Farads.

Enter converter parameters (VMC):

Select this check box if you choose to calculate the required coefficients using parameters based upon the converter power stage design. The parameters will be valid for voltage mode control (VMC) in continuous conduction mode (CCM).

Converter Topology:

The choices here are:

1. Buck
2. Boost
3. Buck-boost

For other topologies, one of the above choices can be used. For example, for a half-bridge, full-bridge, push-pull or forward topology, the buck topology can be selected. For a flyback topology, the buck-boost topology can be selected here.

ADC gain:

Enter the gain of the current measurement network (sensor) in V/A.

DPWM gain:

Enter the effective gain of the digital PWM modulator in V/V.

Converter Inductance:

Insert the value of the converter inductance in microHenries.

Switching Frequency, Fsw:

Insert the converter switching frequency in kHz.

Nominal Input Voltage:

Enter the nominal input voltage of the converter in Volts.

Nominal Output Voltage:

Enter the nominal output voltage of the converter in Volts.

Output Capacitance:

Insert the value of the output capacitance in microfarads.

Output Capacitor ESR:

Insert the value of the output capacitor equivalent series resistance (ESR) in Ohms.

Desired gain cross-over frequency:

Enter the value of the desired gain cross-over frequency (bandwidth of the control loop) in kHz.

Enter directly the desired poles and zeros:

Check this box if the previous input parameters are to be ignored and enter directly the poles and zeros as below.

Pole at the origin, Fp0:

Enter the value of the pole at the origin in kHz.

First pole, Fp1:

Enter the value of the first pole of the compensator in kHz.

First zero, Fz1:

Enter the value of the first zero of the compensator in kHz.

First pole, Fp2:

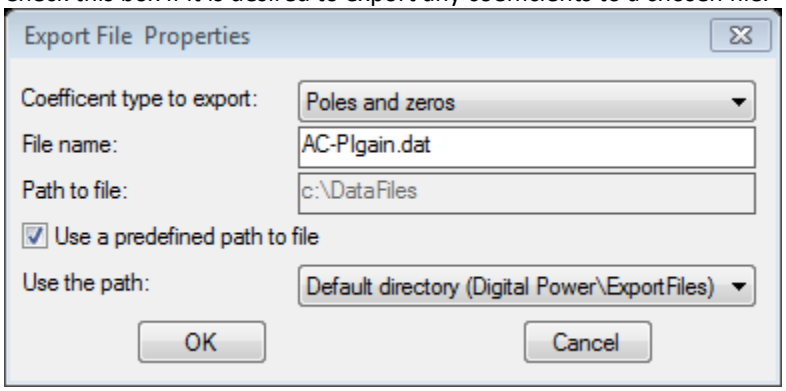
Enter the value of the second pole of the compensator in kHz.

First zero, Fz2:

Enter the value of the second zero of the compensator in kHz.

Export coefficients to file:

Check this box if it is desired to export any coefficients to a chosen file.



Coefficient type to export:

Select the type of coefficients to export. The available selection is:

1. Poles and zeros
2. S-coefficients
3. Z-coefficients

Export file name:

Enter the full file name of the export file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

Select this if the file is located in one of the pre-defined paths.

Use the path:

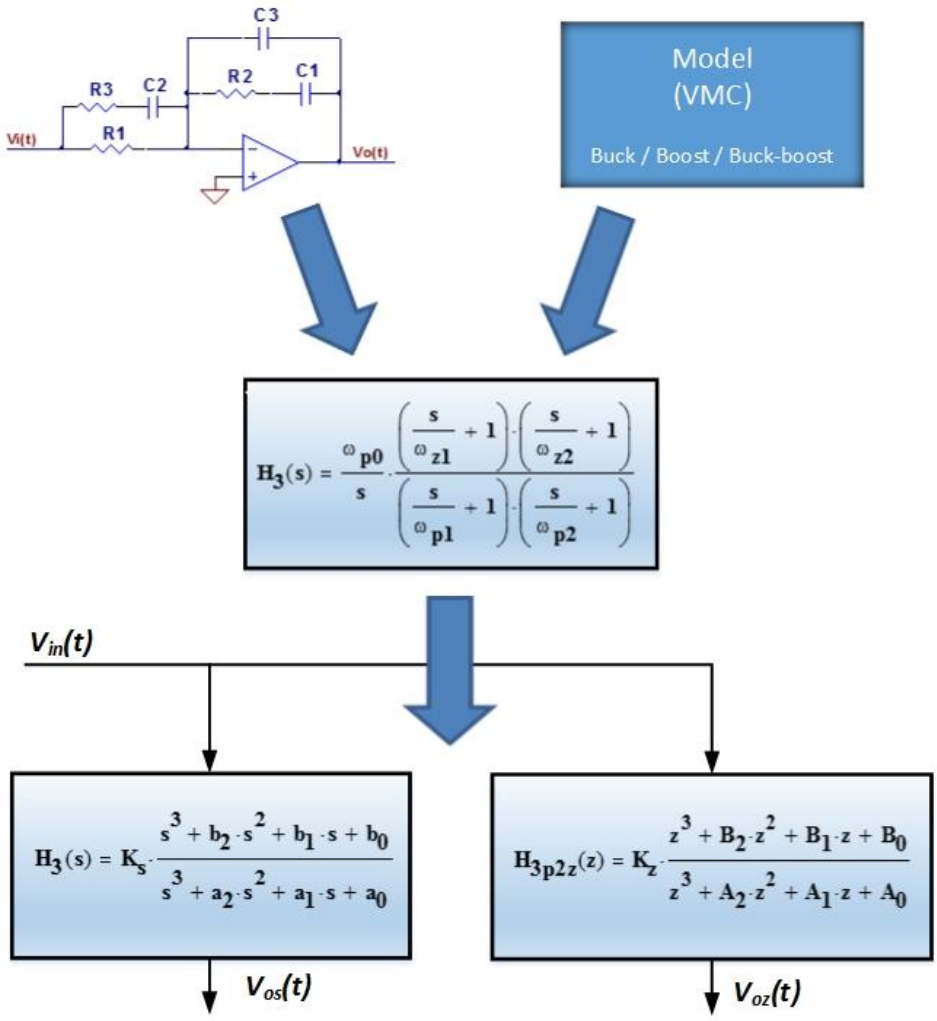
The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

Enable report file:

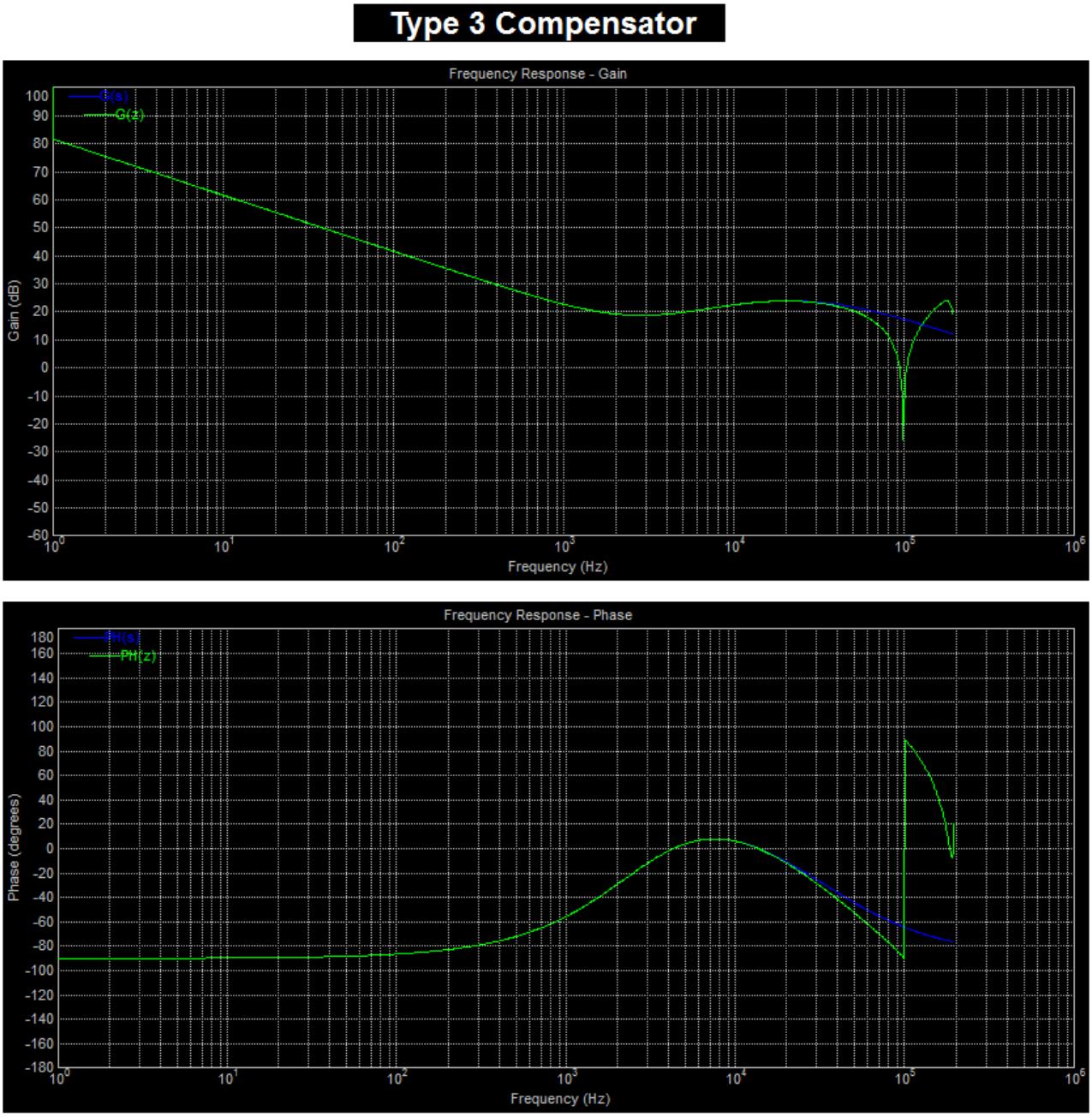
Select this option if a text report file is desired which will be saved in the same directory as this diagram.

The following figure shows the flow of converting the coefficients within the Type 3 compensator conversion tool. The coefficients can be generated from the analog circuit component values. The model is based upon voltage-mode control and can create the required type 3 coefficients from that model as a first pass in the compensator design.



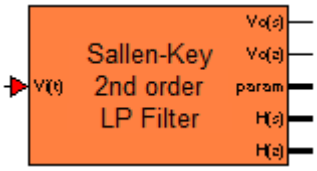
The block can also be used in simulation with one time-dependent input and two time dependent outputs; one using the compensator in the analog domain, the other in the discrete domain.

The frequency response of the type 3 compensator tool is given in the following diagram which shows a comparison of the analog compensator response in blue with the discrete compensator response in green, using the internally generated bilinear (Tustin) transformed coefficients.



Contents - Tools

Analog Converters - Filters

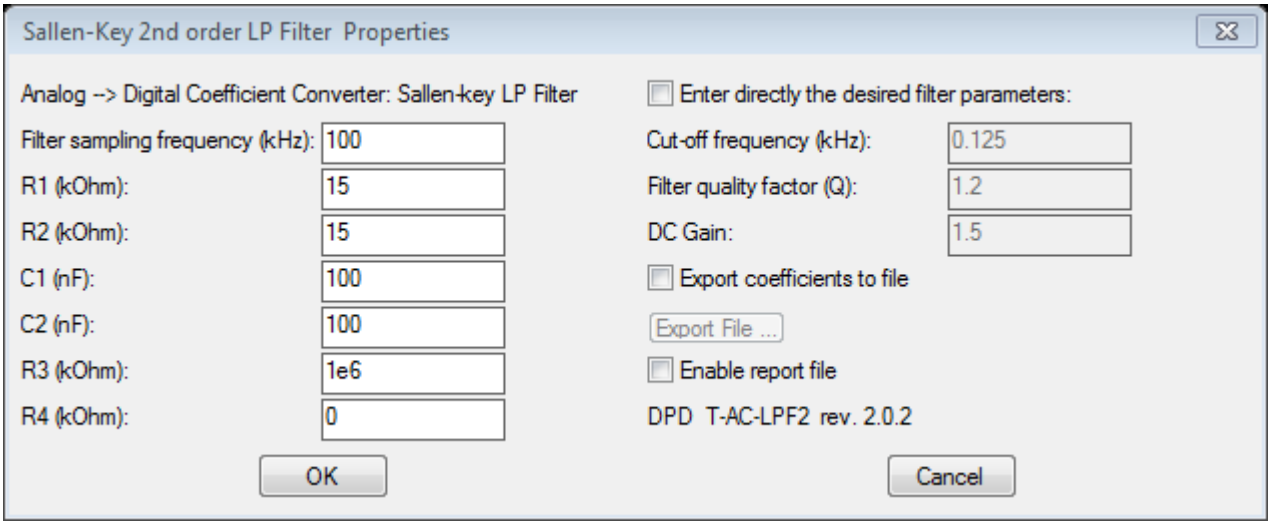


Sallen-key 2nd-order Low-pass Filter

Input pins:	**Vi(t)**	Input signal (optional)
Output pins:	**Vo(s)**	Vout (s-domain or continuous) which can be used in simulation.
	Vo(z)	Vout (z-domain or discrete) which can be used in simulation.
	param	Filter parameters output display (struct).
	H(s)	Filter coefficients in the s-domain (struct).
	H(z)	Filter coefficients in the z-domain (struct).

Dialog properties:

The Sallen-key low-pass filter block properties menu is shown in the following figure which appears when right-clicking on the block.



Filter sampling frequency:

Enter the value of the sampling frequency (for a digital filter using z-coefficients).

R1:

Enter the value of the block circuit schematic resistance R1 in kilo-Ohms.

R2:

Enter the value of the block circuit schematic resistance R2 in kilo-Ohms

C1:

Enter the value of the block circuit schematic resistance C1 in nano-Farads

C2:

Enter the value of the block circuit schematic resistance C2 in nano-Farads

R3:

Enter the value of the block circuit schematic resistance R3 in kilo-Ohms.

R4:

Enter the value of the block circuit schematic resistance R4 in kilo-Ohms

Enter directly the desired filter parameters:

Check this box if the previous circuit values are to be ignored and enter directly the filter parameters as below.

Center Frequency, Fo:

Enter the value of the required cut-off frequency in kHz of the low-pass filter.

Filter quality factor, Q:

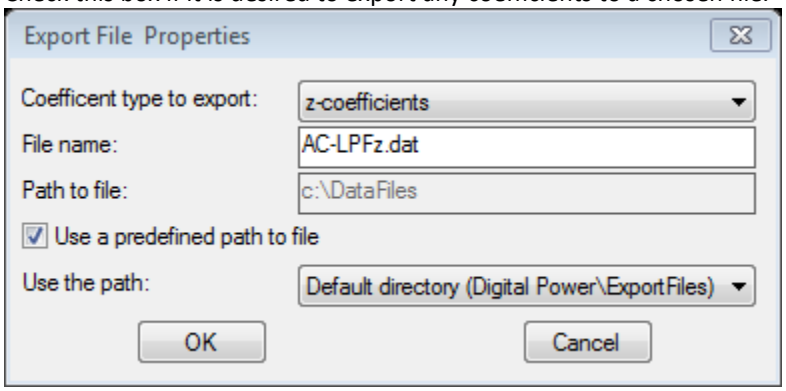
Enter the value of the required filter quality factor, Q.

DC gain, Ks:

Enter the required value of the low-frequency gain of the low-pass filter.

Export coefficients to file:

Check this box if it is desired to export any coefficients to a chosen file.



Coefficient type to export:

Select the type of coefficients to export. The available selection is:

1. S-coefficients
2. Z-coefficients

Export file name:

Enter the full file name of the export file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

Select this if the file is located in one of the pre-defined paths.

Use the path:

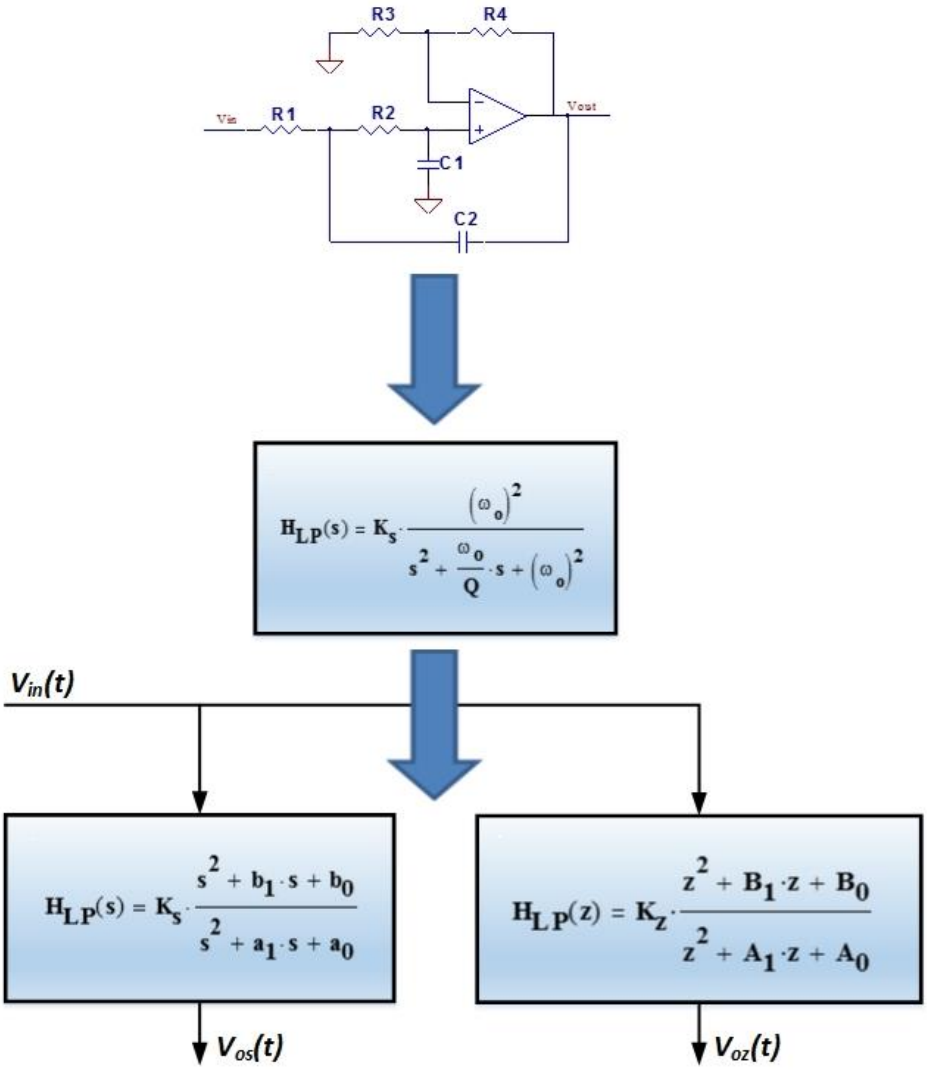
The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

Enable report file:

Select this option if a text report file is desired which will be saved in the same directory as this diagram.

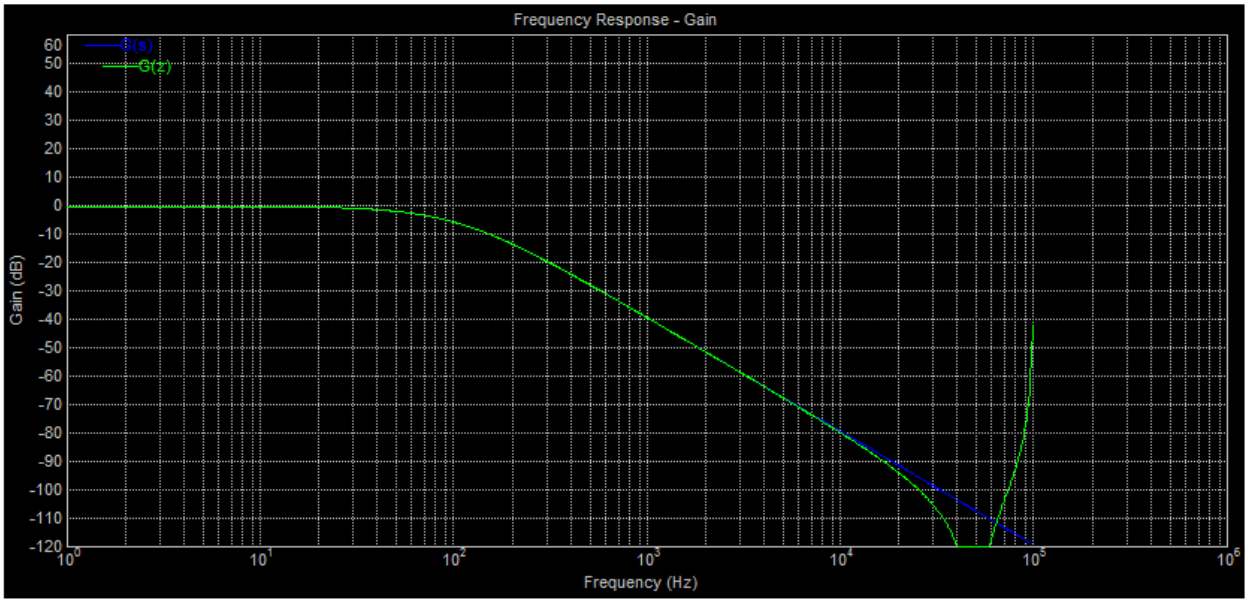
The following figure shows the flow of converting the coefficients within the Sallen-Key low-pass filter conversion tool. The coefficients can be generated from the analog circuit component values.

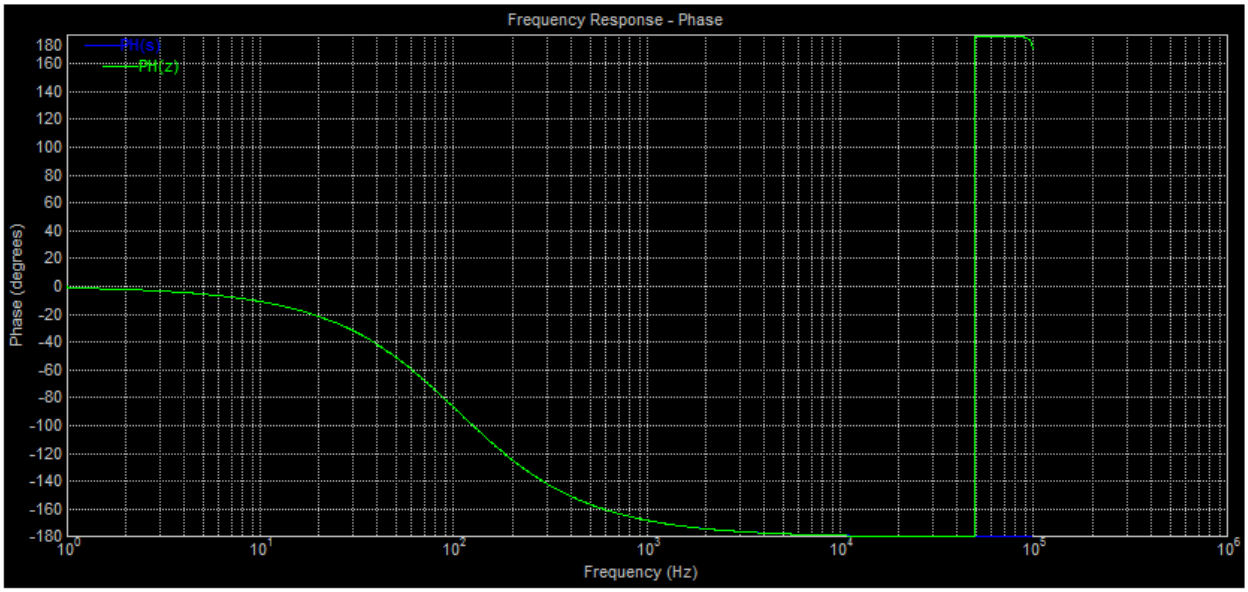


The block can also be used in simulation with one time-dependent input and two time dependent outputs; one using the filter in the analog domain, the other in the discrete domain.

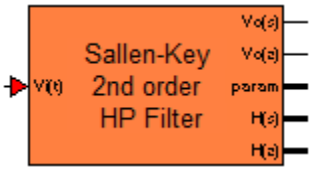
The frequency response of the Sallen-Key low-pass filter is given in the following diagram which shows a comparison of the analog filter response in blue with the discrete filter response in green, using the internally generated bilinear (Tustin) transformed coefficients.

Sallen-Key Low-pass Filter





Contents - Tools

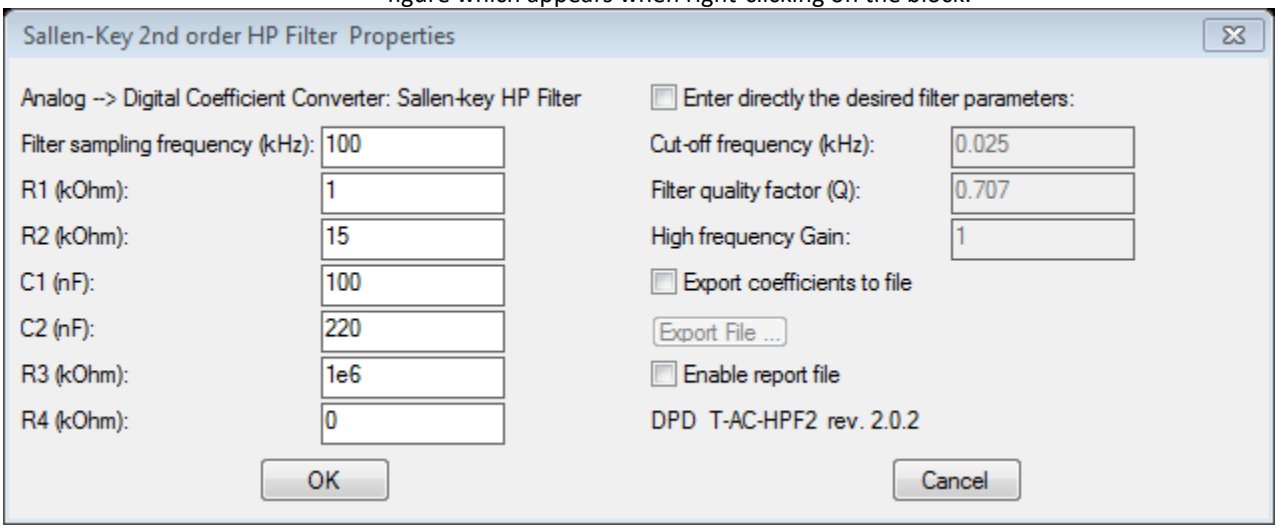


Sallen-key 2nd-order High-pass Filter

Input pins:	**Vi(t)**	Input signal (optional)
Output pins:	**Vo(s)**	Vout (s-domain or continuous) which can be used in simulation.
	Vo(z)	Vout (z-domain or discrete) which can be used in simulation.
	param	Filter parameters output display (struct).
	H(s)	Filter coefficients in the s-domain (struct).
	H(z)	Filter coefficients in the z-domain (struct).

Dialog properties:

The Sallen-key high-pass filter block properties menu is shown in the following figure which appears when right-clicking on the block.



Filter sampling frequency:

Enter the value of the sampling frequency (for a digital filter using z-coefficients).

R1:

Enter the value of the block circuit schematic resistance R1 in kilo-Ohms.

R2:

Enter the value of the block circuit schematic resistance R2 in kilo-Ohms

C1:

Enter the value of the block circuit schematic resistance C1 in nano-Farads

C2:

Enter the value of the block circuit schematic resistance C2 in nano-Farads

R3:

Enter the value of the block circuit schematic resistance R3 in kilo-Ohms.

R4:

Enter the value of the block circuit schematic resistance R4 in kilo-Ohms

Enter directly the desired filter parameters:

Check this box if the previous circuit values are to be ignored and enter directly the filter parameters as below.

Center Frequency, Fo:

Enter the value of the required cut-off frequency in kHz of the high-pass filter.

Filter quality factor, Q:

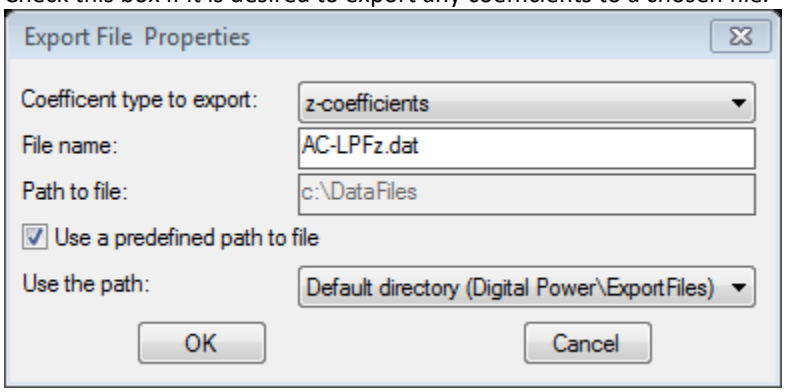
Enter the value of the required filter quality factor, Q.

High frequency gain, Ks:

Enter the required value of the high-frequency gain of the high-pass filter.

Export coefficients to file:

Check this box if it is desired to export any coefficients to a chosen file.



Coefficient type to export:

Select the type of coefficients to export. The available selection is:

1. S-coefficients
2. Z-coefficients

Export file name:

Enter the full file name of the export file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

Select this if the file is located in one of the pre-defined paths.

Use the path:

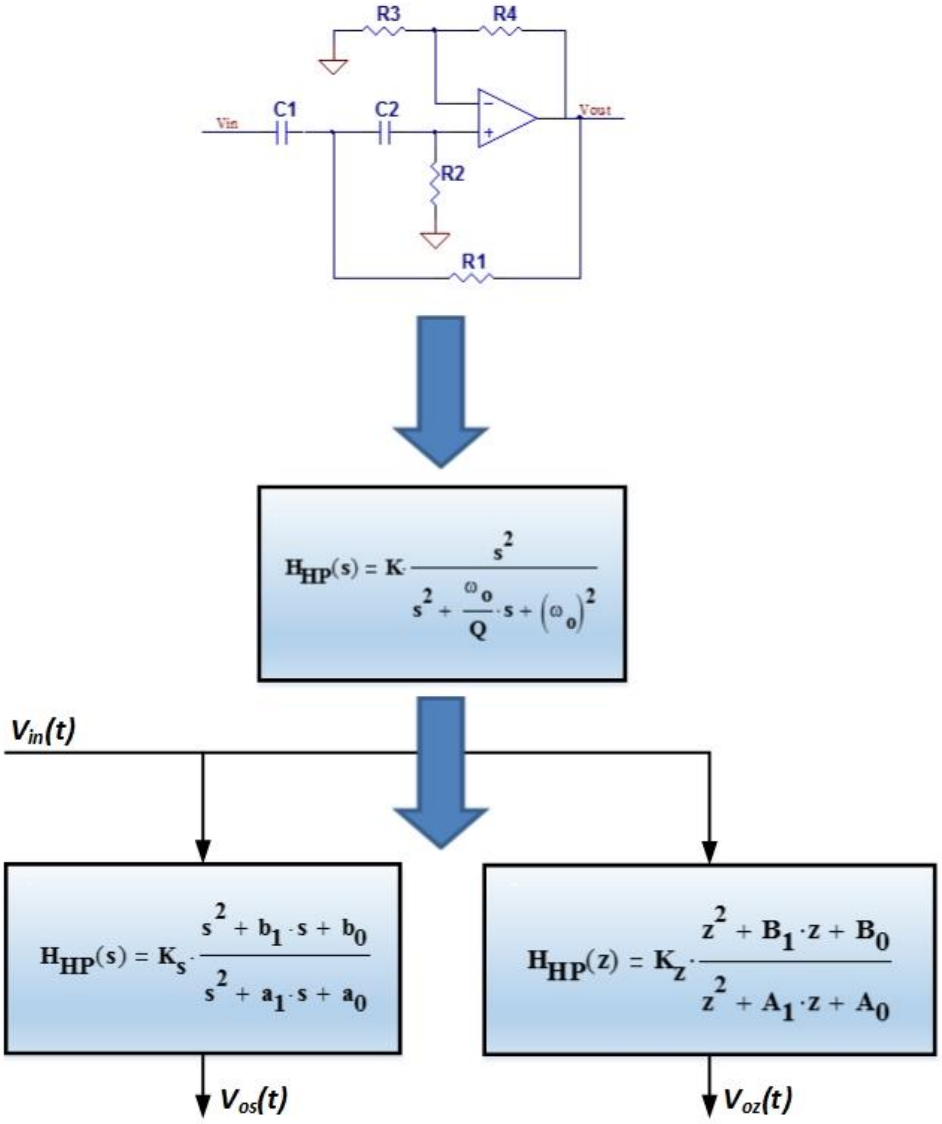
The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

Enable report file:

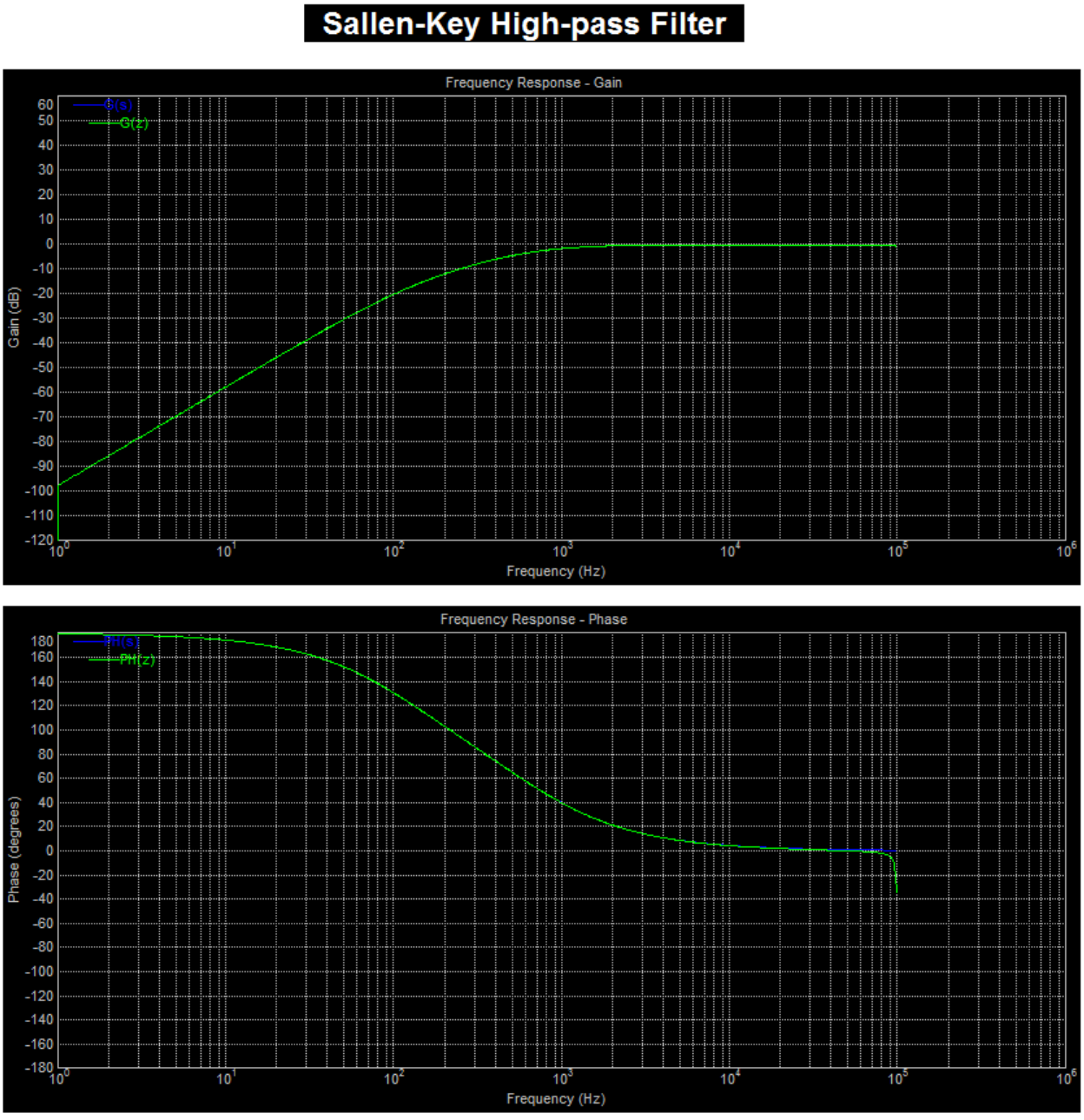
Select this option if a text report file is desired which will be saved in the same directory as this diagram.

The following figure shows the flow of converting the coefficients within the Sallen-Key high-pass filter conversion tool. The coefficients can be generated from the analog circuit component values.



The block can also be used in simulation with one time-dependent input and two time dependent outputs; one using the filter in the analog domain, the other in the discrete domain.

The frequency response of the Sallen-Key high-pass filter is given in the following diagram which shows a comparison of the analog filter response in blue with the discrete filter response in green, using the internally generated bilinear (Tustin) transformed coefficients.



Contents - Tools

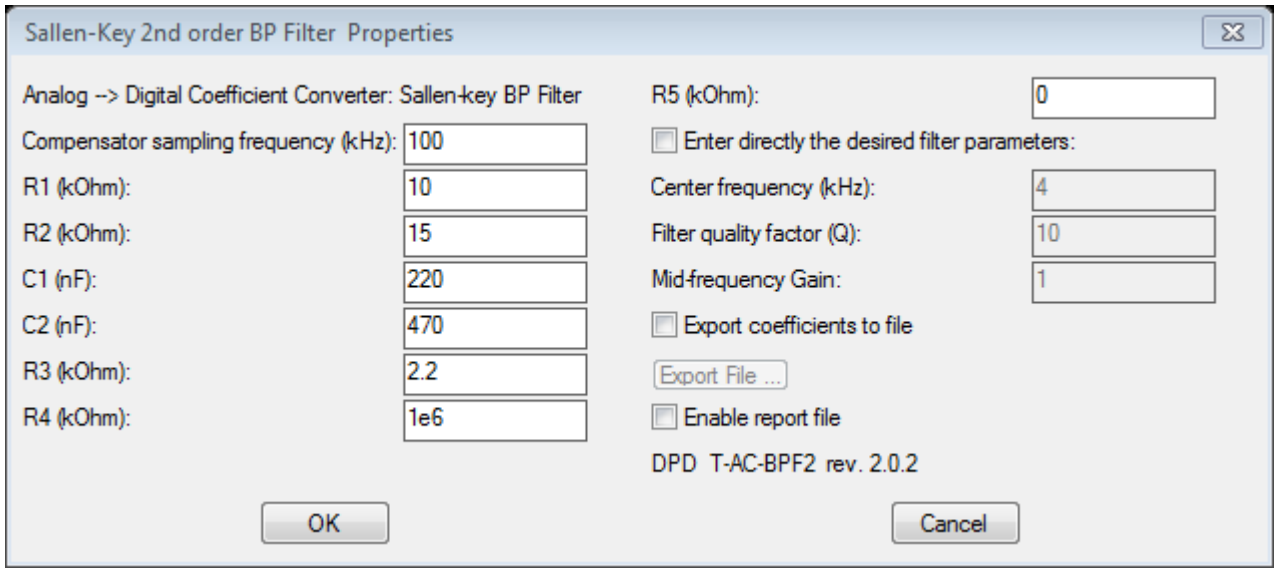


Sallen-key 2nd-order Band-pass Filter

Input pins:	**Vi(t)**	Input signal (optional)
Output pins:	**Vo(s)**	Vout (s-domain or continuous) which can be used in simulation.
	Vo(z)	Vout (z-domain or discrete) which can be used in simulation.
	param	Filter parameters output display (struct).
	H(s)	Filter coefficients in the s-domain (struct).
	H(z)	Filter coefficients in the z-domain (struct).

Dialog properties:

The Sallen-key band-pass filter block properties menu is shown in the following figure which appears when right-clicking on the block.



Filter sampling frequency:

Enter the value of the sampling frequency (for a digital filter using z-coefficients).

R1:

Enter the value of the block circuit schematic resistance R1 in kilo-Ohms.

R2:

Enter the value of the block circuit schematic resistance R2 in kilo-Ohms

C1:

Enter the value of the block circuit schematic resistance C1 in nano-Farads

C2:

Enter the value of the block circuit schematic resistance C2 in nano-Farads

R3:

Enter the value of the block circuit schematic resistance R3 in kilo-Ohms.

R4:

Enter the value of the block circuit schematic resistance R4 in kilo-Ohms

R5:

Enter the value of the block circuit schematic resistance R5 in kilo-Ohms.

Enter directly the desired filter parameters:

Check this box if the previous circuit values are to be ignored and enter directly the filter parameters as below.

Center Frequency:

Enter the value of the required center frequency in kHz of the band-pass filter.

Filter quality factor:

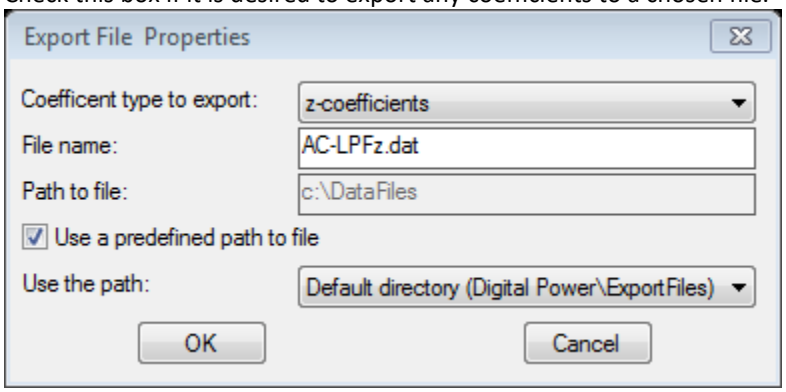
Enter the value of the required filter quality factor, Q.

Mid-frequency gain:

Enter the required value of the mid-frequency gain of the band-pass filter.

Export coefficients to file:

Check this box if it is desired to export any coefficients to a chosen file.



Coefficient type to export:

Select the type of coefficients to export. The available selection is:

1. S-coefficients
2. Z-coefficients

Export file name:

Enter the full file name of the export file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

Select this if the file is located in one of the pre-defined paths.

Use the path:

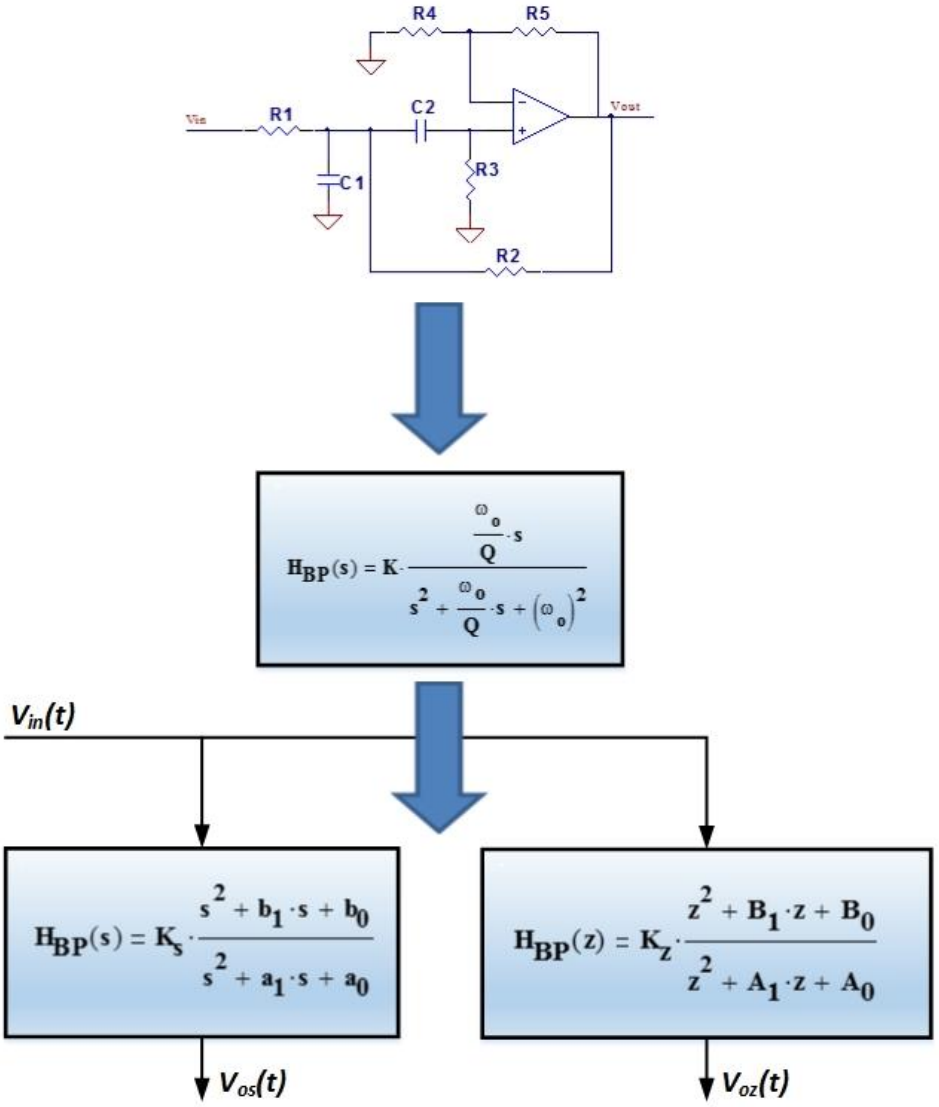
The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

Enable report file:

Select this option if a text report file is desired which will be saved in the same directory as this diagram.

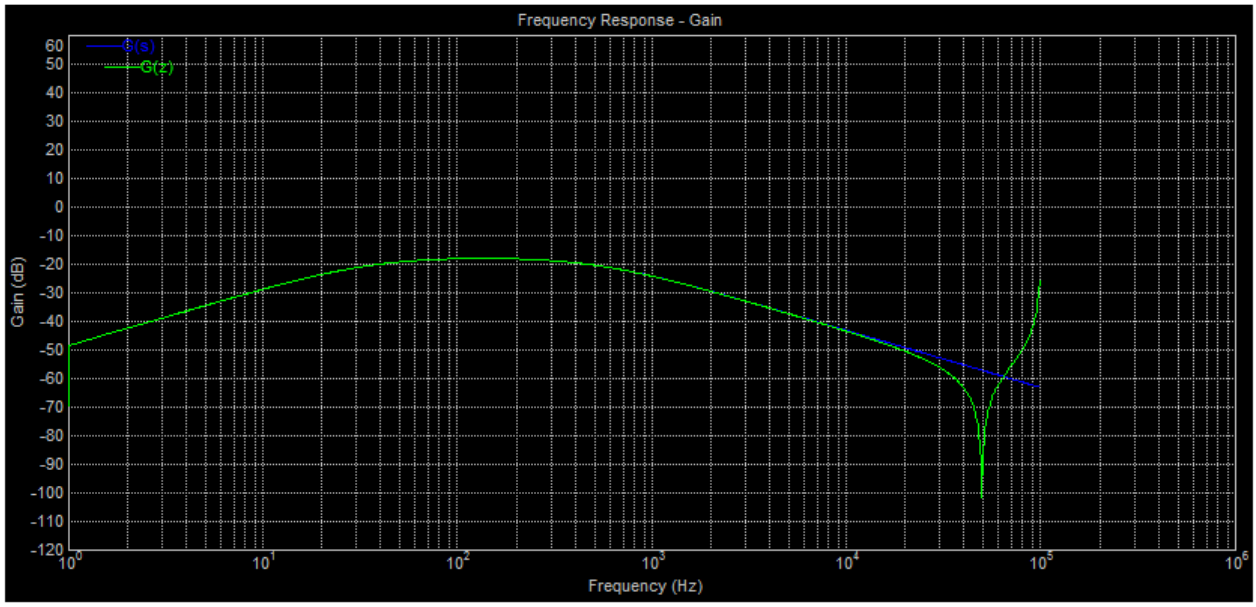
The following figure shows the flow of converting the coefficients within the Sallen-Key band-pass filter conversion tool. The coefficients can be generated from the analog circuit component values.

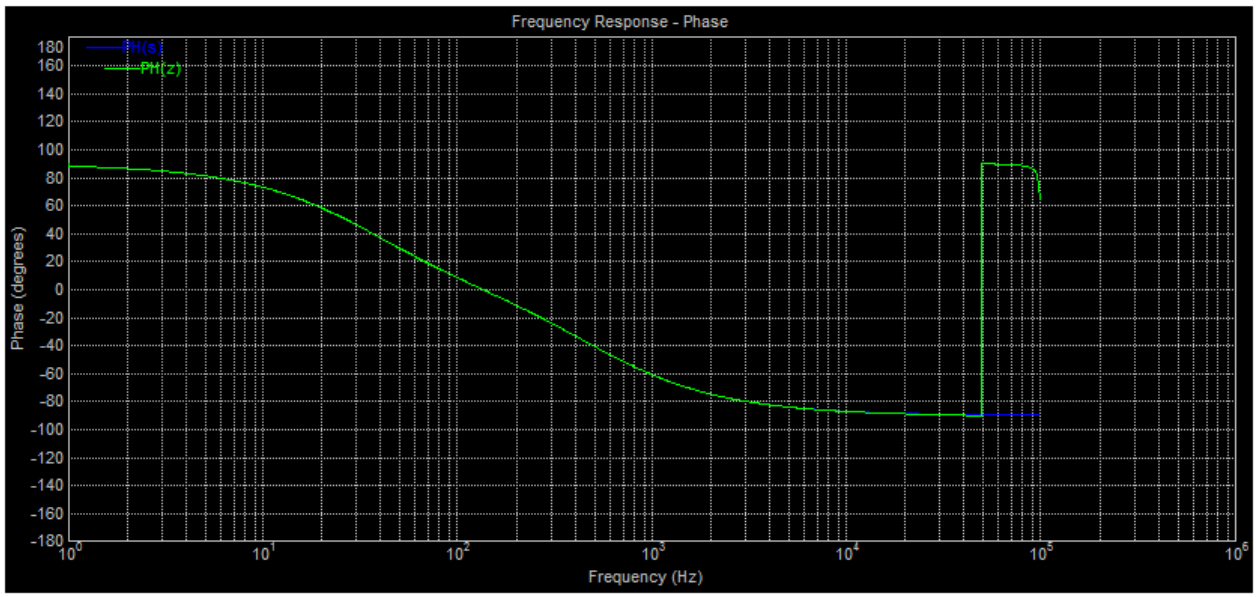


The block can also be used in simulation with one time-dependent input and two time dependent outputs; one using the filter in the analog domain, the other in the discrete domain.

The frequency response of the Sallen-Key band-pass filter is given in the following diagram which shows a comparison of the analog filter response in blue with the discrete filter response in green, using the internally generated bilinear (Tustin) transformed coefficients.

Sallen-Key Band-pass Filter

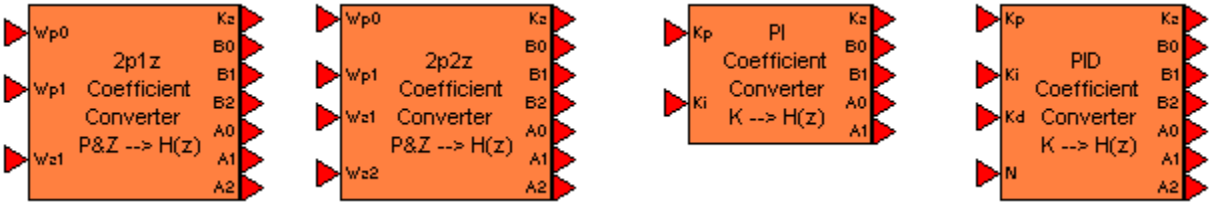




Contents - Tools

Coefficient Converters

2p1z, 2p2z, 3p2z, 3p3z, PI, PID Coefficient Converters



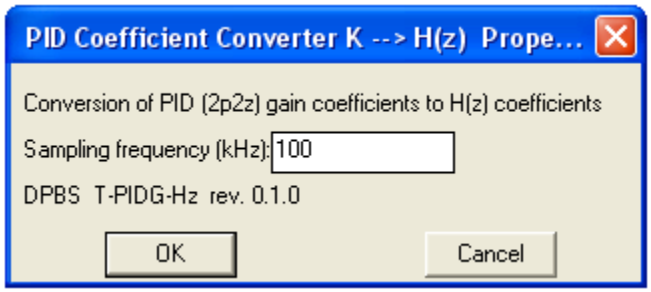
There are six different coefficient converter tools currently in the block set. The direct coefficient converter tools are intended to be used in diagrams where interactive simulations can be performed to observe the converter control behaviour when changing the compensator coefficients during the simulation. The blocks directly translate from the familiar poles and zeros or PID gain coefficients to the more unfamiliar discrete z-coefficients. They would normally be used in conjunction with the compensators with pins from the codegen section. The output z-coefficients are of a form consistent with Embed/Digital Power Designer as:

$$H_3(z) = K_z \cdot \frac{z^3 + B_2 \cdot z^2 + B_1 \cdot z + B_0}{z^3 + A_2 \cdot z^2 + A_1 \cdot z + A_0}$$

Input pins:	**Wpx**	Input pole (radians) which would normally be connected from a slider.
	Wzx	Input zero (radians) which would normally be connected from a slider.
	Kx	PID gain which would normally be connected from a slider.
Output pins:	**Kz**	Discrete z-coefficients gain
	Bx	Numerator discrete z-coefficients
	Ax	Denominator discrete z-coefficients

Dialog properties:

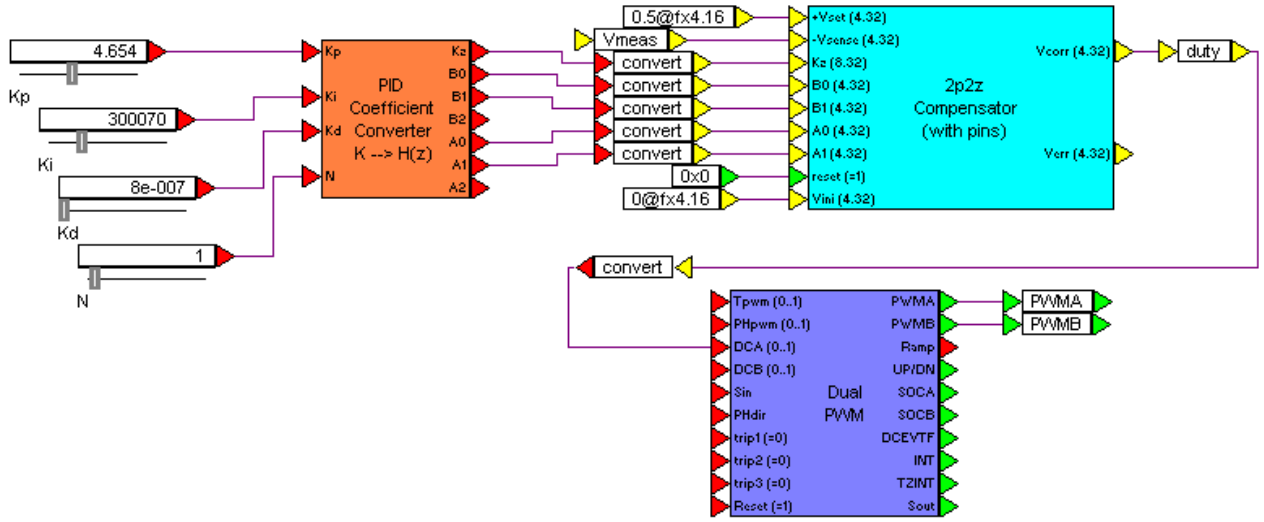
The coefficient converter blocks properties menu is shown in the following figure which appears when right-clicking on any of the coefficient converter blocks.



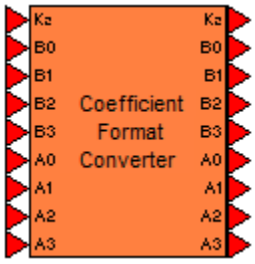
Sampling frequency (kHz):

Enter the value of the desired sampling frequency. Note that changing the sampling frequency will result in changing the z-coefficients and this value is very important for correct coefficient conversion.

An example of the use (connection within a diagram) of the coefficient converter tools is as follows:



Contents - Tools



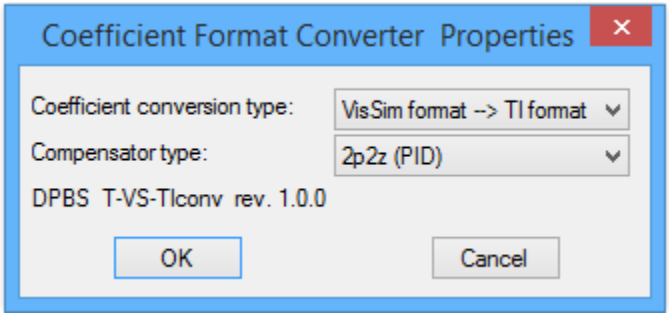
Coefficient Format Converter

The coefficient format converter converts to and from the coefficient format used within the digital power designer block set and the Texas Instruments (TI) format used within their documentation and software.

Input pins:	**Kz**	Gain input of the coefficient to be converted.
	Bx	Numerator coefficient to be converted.
	Ax	Denominator coefficient to be converted.
Output pins:	**Kz**	Converted gain coefficient output.
	Bx	Converted numerator coefficient output
	Ax	Converted denominator coefficient output

Dialog properties:

The coefficient format converter block properties menu is shown in the following figure which appears when right-clicking on the coefficient format converter block.



Coefficient conversion type:

Enter the conversion direction.

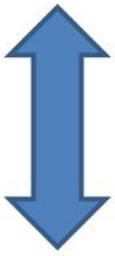
Compensator type:

Select from:

1. 1p1z (PI)
2. 2p1z (Type 2)
3. 2p2z (PID)
4. 3p2z (Type 3)
5. 3p3z

The bidirectional conversion takes the form:

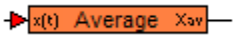
$$H_{VS}(z) = K_z \cdot \frac{z^n + \ldots + B_2 \cdot z^2 + B_1 \cdot z + B_0}{z^n + \ldots + A_2 \cdot z^2 + A_1 \cdot z + A_0}$$



$$H_{TI}(z) = \cdot \frac{B_0 + B_1 \cdot z^{-1} + B_2 \cdot z^{-2} + \ldots + B_n \cdot z^{-n}}{1 - A_1 \cdot z^{-1} - A_2 \cdot z^{-2} - \ldots - A_n \cdot z^{-n}}$$

Measurements

The measurements sub- section contains tools in order to perform measurements on waveforms typically used in digital power applications.



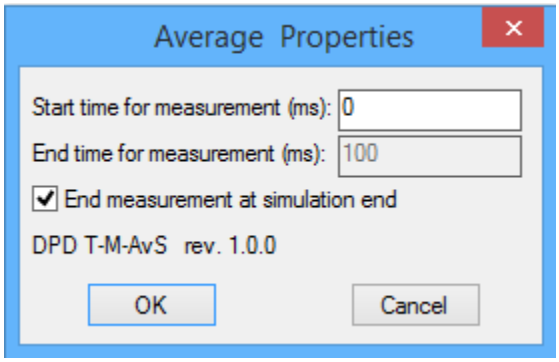
Average

Input pin: x**(t)** Input signal to be measured.

Output pin: **Xav** Average measurement output.

Dialog properties:

The average block properties menu is shown in the following figure which appears when right-clicking on the block.

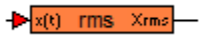


Start time for measurement:

Give the starting time in milli-seconds to begin the measurement.

End time for measurement:

Give the end time in milli-seconds to terminate the measurement or otherwise one can select to end the measurement at the end of the simulation.



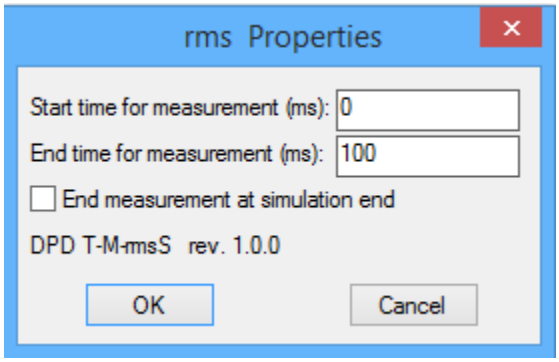
Rms

Input pin: x**(t)** Input signal to be measured.

Output pin: **Xrms** Root-mean-square measurement output.

Dialog properties:

The rms block properties menu is shown in the following figure which appears when right-clicking on the block.



Start time for measurement:

Give the starting time in milli-seconds to begin the measurement.

End time for measurement:

Give the end time in milli-seconds to terminate the measurement or otherwise one can select to end the measurement at the end of the simulation.



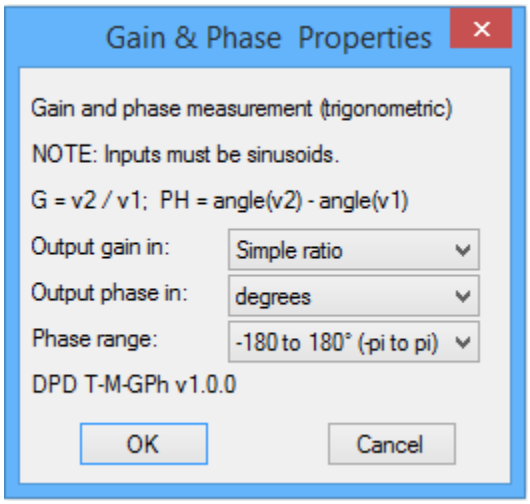
Gain and Phase

The gain and phase measurement of two sinewaves.

Input pins:	EN	Enable input pin to dynamically enable the measurement.
	v1(t)	Input v1(t) sinewave.
	v2(t)	Input v2(t) sinewave.
Output pins:	**G**	Gain output in the selected units.
	PH	Phase output in the selected units.

Dialog properties:

The gain and phase block properties menu is shown in the following figure which appears when right-clicking on the block.



Output gain in:

Choices here are a simple gain ratio or in dB.

Output phase in:

Choices here are in radians or degrees.

Phase range:

Select the range for the phase measurement.



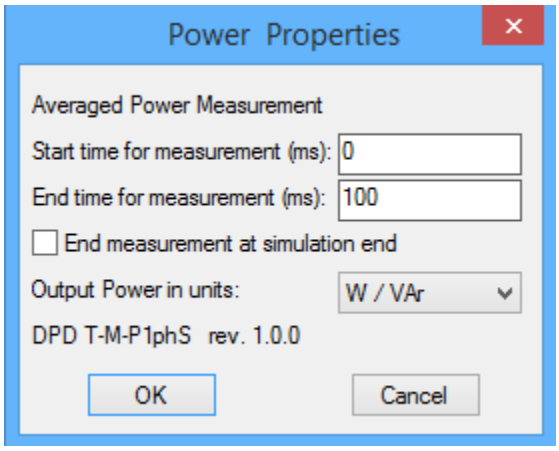
Power

This block performs an average power measurement over the specified time period.

Input pins:	**v(t)**	Line voltage in Volts.
	i(t)	Line current in amps.
Output pins:	**P**	Active power output in the selected units.
	Q	Reactive power output in the selected units.

Dialog properties:

The power measurement block properties menu is shown in the following figure which appears when right-clicking on the block.



Start time for measurement:

Give the starting time in milli-seconds to begin the measurement.

End time for measurement:

Give the end time in milli-seconds to terminate the measurement or otherwise one can select to end the measurement at the end of the simulation.

Output power in units:

Select the units for the output active and reactive powers.



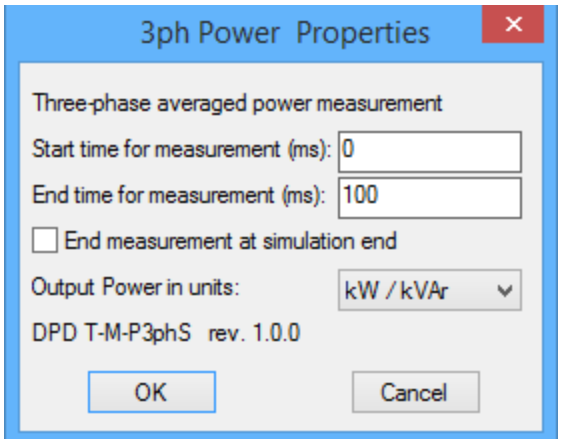
Three-phase Power

This block performs an average 3-phase power measurement over the specified time period.

Input pins:	**v[L1,L2,L3]**	Three-phase line-neutral phase voltages.
	i[L1,L2,L3]	Three-phase line currents.
Output pins:	**P**	Active power output in the selected units.
	Q	Reactive power output in the selected units.

Dialog properties:

The 3-phase power block properties menu is shown in the following figure which appears when right-clicking on the block.



Start time for measurement:

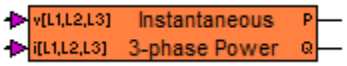
Give the starting time in milli-seconds to begin the measurement.

End time for measurement:

Give the end time in milli-seconds to terminate the measurement or otherwise one can select to end the measurement at the end of the simulation.

Output power in units:

Select the units for the output active and reactive powers.



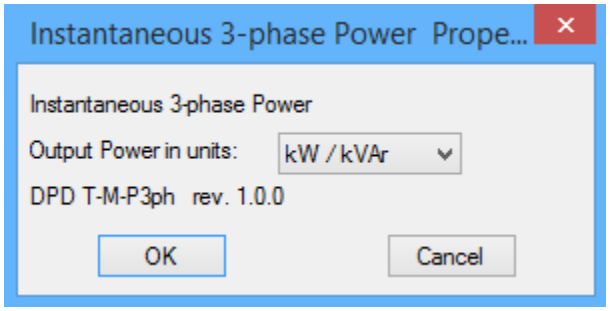
Instantaneous Power – 3 phase

Calculates the 3-phase instantaneous power.

Input pins:	**v[L1,L2,L3]**	Three-phase line-neutral phase voltages.
	i[L1,L2,L3]	Three-phase line currents.
Output pins:	**P**	Active power output in the selected units.
	Q	Reactive power output in the selected units.

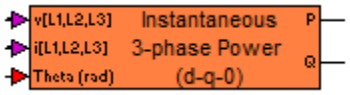
Dialog properties:

The instantaneous power block properties menu is shown in the following figure which appears when right-clicking on the block.



Output power in units:

Select the units for the output active and reactive powers.



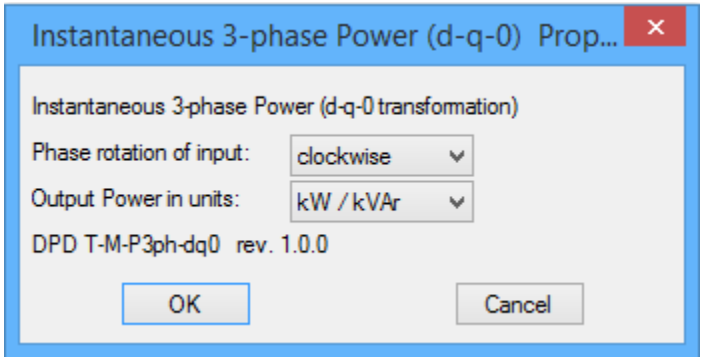
Instantaneous Power – 3 phase (d-q-0)

Calculates the 3-phase instantaneous power using the d-q-0 transformation.

Input pins:	**v[L1,L2,L3]**	Three-phase line-neutral phase voltages.
	i[L1,L2,L3]	Three-phase line currents.
	Theta	The electrical angle input in radians.
Output pins:	**P**	Active power output in the selected units.
	Q	Reactive power output in the selected units.

Dialog properties:

The instantaneous power block properties menu is shown in the following figure which appears when right-clicking on the block.



Phase rotation of input:

Select the phase rotation of the 3-phase input voltages and currents.

Output power in units:

Select the units for the output active and reactive powers.



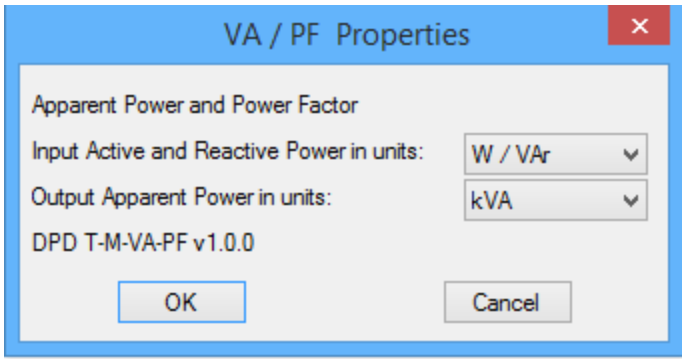
VA / Power Factor

Calculates the apparent power and power factor.

Input pins:	**P**	Active power input.
	Q	Reactive power input.
Output pins:	**VA**	Apparent power output in the selected units.
	PF	Power Factor output.

Dialog properties:

The VA/PF block properties menu is shown in the following figure which appears when right-clicking on the block.

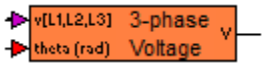


Input active and reactive powers in units:

Select the units for the input active and reactive powers.

Output apparent power in units:

Select the units for the output apparent powers.



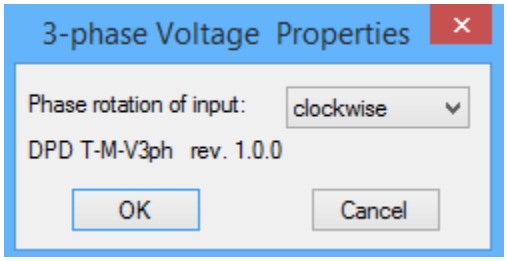
3-phase Voltage

Calculates the instantaneous effective 3-phase voltage.

Input pins:	**v[L1,L2,L3]**	Three-phase line-neutral phase voltages.
	Theta	The electrical angle input in radians.
Output pins:	**V**	Effective voltage output.

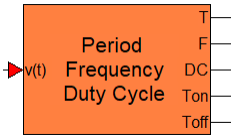
Dialog properties:

The 3-phase voltage block properties menu is shown in the following figure which appears when right-clicking on the block.



Phase rotation of input:

Select the phase rotation of the 3-phase input voltages and currents.



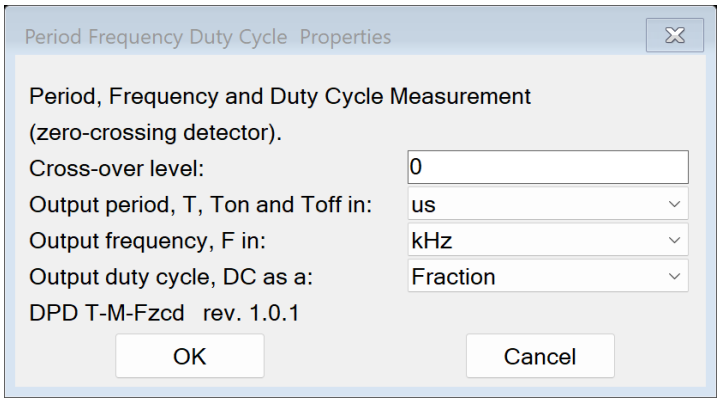
Period, Frequency, Duty-cycle

Calculates the period, frequency and duty cycle of an arbitrary waveform using a cross-over detector.

Input pins:	**v(t)**	Input waveform.
Output pins:	**T**	Period output in the selected units.
	F	Frequency output in the selected units.
	DC	Duty cycle output.
	Ton	Turn-on (high) time.
	Toff	Turn-off (low) time.

Dialog properties:

The period, frequency, duty cycle block properties menu is shown in the following figure which appears when right-clicking on the block.



Cross-over level:

Select level at which the internal cross-detector activates for the measurements.

Output the period T, in:

Select the units for the period, turn-on time and turn-off time output values.

Output frequency, F in:

Select the units for the frequency output value.

Output duty cycle, DC as:

Select the mode to output the duty cycles as a fraction or percentage.



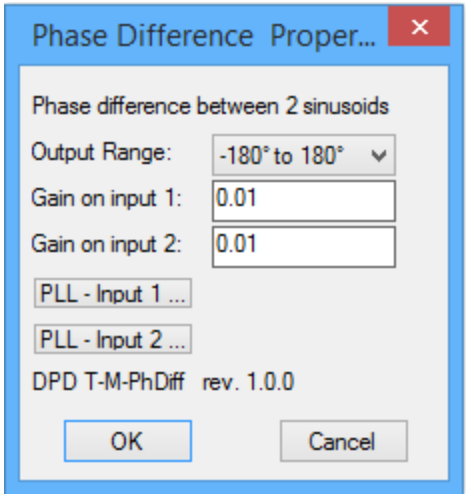
Phase Difference

Calculates the phase difference of two incoming sine-waves by using dual Second-Order Generalised Integrator Phase Lock Loops (SOGI-PLLs). The frequencies of the two input signals are therefore as a consequence calculated.

Input pins:	**v1(t)**	Input signal 1.
	v2(t)	Input signal 2.
Output pins:	**Phase**	Phase value output as a difference between the two input waveforms.
	F1 (Hz)	The frequency of input signal 1.
	F2 (Hz)	The frequency of input signal 2.

Dialog properties:

The phase difference block properties menu is shown in the following figure which appears when right-clicking on the block.



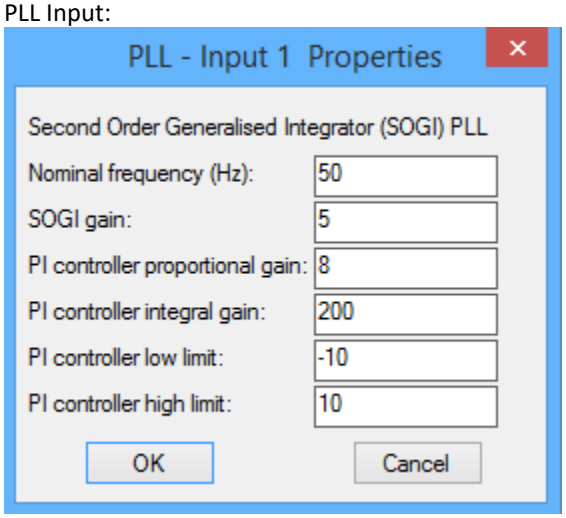
Output range:

Select the range of the phase difference output in degrees.

Gain on inputs 1 and 2:

Give a gain on the incoming input signals feeding the PLLs.

PLL Input:



Nominal frequency:

Set the nominal frequency of the input signals in Hz.

SOGI gain:

Set the gain of the SOGI PLL stage.

PI controller proportional gain:

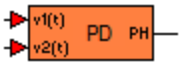
Set the internal PI controller proportional gain.

PI controller integral gain:

Set the internal PI controller integral gain.

PI controller low and high limits:

Set the internal PI controller internal integral limits.



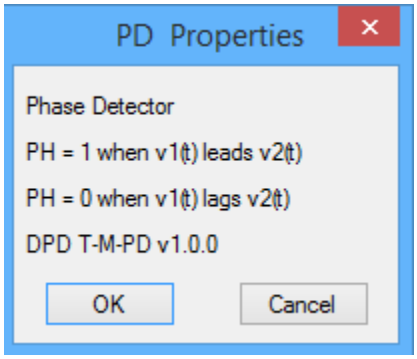
Phase Detector

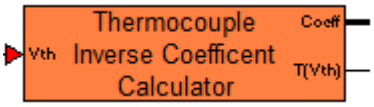
Determines if one input signal is lagging or leading the other input signal.

Input pins:	**v1(t)**	Input sine-wave 1.
	v2(t)	Input sine-wave 2.
Output pins:	**PH**	Output for leading or lagging phase.

Dialog properties:

The phase-detector block properties menu is shown in the following figure which appears when right-clicking on the block.





Thermocouple Inverse Coefficient Calculator

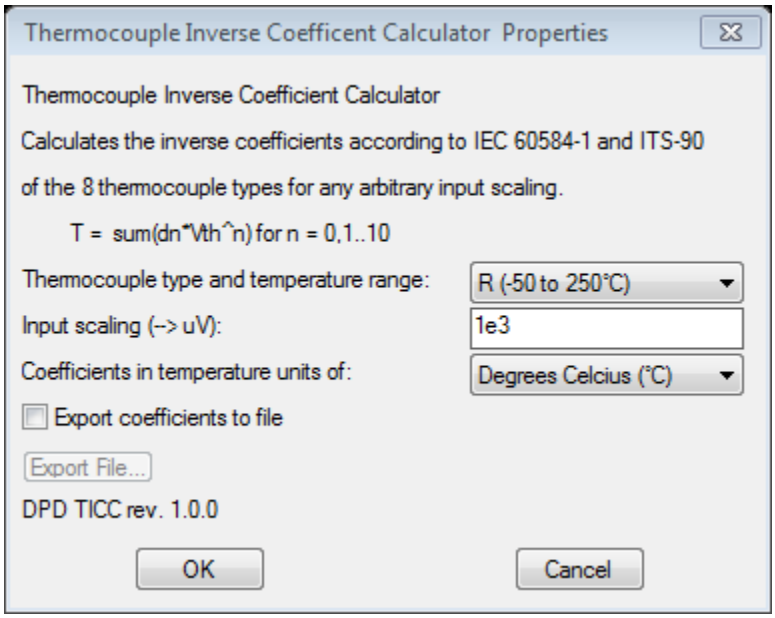
This block calculates the inverse thermocouple coefficients of the 8 standard thermocouple types according to IEC 60584-1 and ITS-90 for any arbitrary input scaling according to:

$$T = sum(d_n * V_{th}^n) \quad for\ \ n = 0{,}1..10$$

Input pins:	**Vth**	The thermal voltage input of the thermocouple
Output pins:	**Coeff**	Output struct with the thermocouple coefficients.
	T(Vth)	Temperature output corresponding to the thermal voltage input and selected thermocouple type.

Dialog properties:

The thermocouple inverse coefficient calculator block properties menu is shown in the following figure which appears when right-clicking on the block.



Thermocouple type and temperature range:

The possible selections here are.

1. J (-210 to 0°C)
2. J (0 to 760°C)
3. J (760 to 1200°C)
4. K (-210 to 0°C)
5. K (0 to 500°C)
6. K (500 to 1372°C)
7. T (-200 to 0°C)
8. T (0 to 400°C)
9. E (-270 to 0°C)
10. E (0 to 1000°C)
11. N (-200 to 0°C)
12. N (0 to 600°C)
13. N (600 to 1300°C)
14. B (250 to 700°C)

15. B (700 to 1820°C)
16. R (-50 to 250°C)
17. R (250 to 1064°C)
18. R (1064 to 1664.5°C)
19. R (1664.5 to 1786.1°C)
20. S (-50 to 250°C)
21. S (250 to 1064°C)
22. S (1064 to 1664.5°C)
23. S (1664.5 to 1786.1°C)

Input scaling (→ uV):

Set the input scaling necessary in order to transform the input value will be translated to micro-volts.

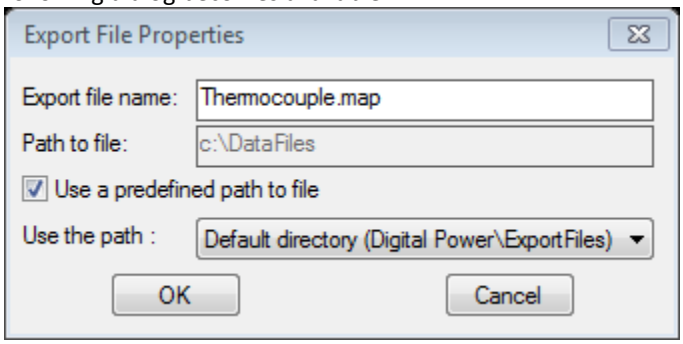
Coefficients in temperature units of:

The possible selections here are:

1. Degrees Celsius (°C)
2. Degrees Fahrenheit (°F)
3. Kelvin (K)

Export coefficients to file:

If selected, the thermocouple coefficients can be exported to a file and the following dialog becomes available:



Export file name:

Enter the full file name of the export file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

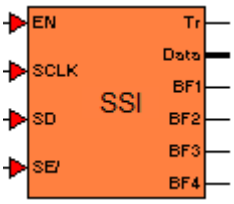
Select this if the file is located in one of the pre-defined paths.

Use the path:

The pre-defined paths are:

1. Same directory as the embed diagram directory
2. User directory (Digital Power\User\files)
3. Default directory (Digital Power\ExportFiles)

Communications



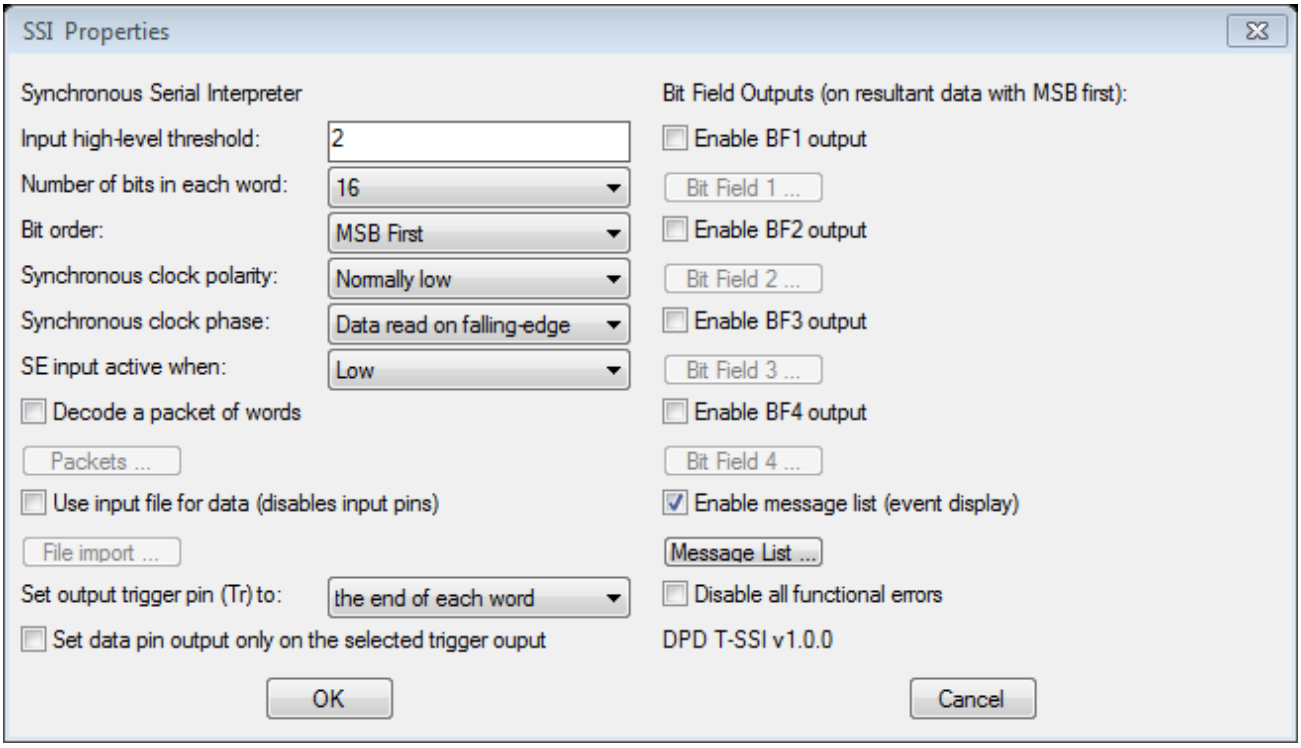
Synchronous Serial Interpreter

Interprets synchronous serial data and particularly for a SPI communication interface. There are a large amount of configuration selections in order to interpret serial data. This data can be generated in Altair Embed diagrams such as using the SPI Emulators blocks in the MCU Peripherals of the Simulation section of this user guide or by importing data from popular logic analyzers.

Input pins:	**EN**	Enable input. When ≥ 1, the interpreter will start interpreting the input data.
	SCLK	Serial clock input.
	SD	Serial data input.
	SE/	Sync input (or slave transmit enable).
Output pins:	**Tr**	Trigger output configured internally in the block dialog.
	Data	Data output (can be triggered)
	BF1	First Bit field output as configured internally in the block dialog.
	BF2	Second Bit field output as configured internally in the block dialog.
	BF3	Third Bit field output as configured internally in the block dialog.
	BF4	Fourth Bit field output as configured internally in the block dialog.

Dialog properties:

The SSI block properties menu is shown in the following figure which appears when right-clicking on the block.



Input high-level threshold:

Set the threshold value for the input data.

Number of bits in each word:

Set the word size from 1 to 32 bits.

Bit order:

Set the bit order to either MSB first or LSB first.

Synchronous clock polarity:

The available selections here are:

1. Normally low
2. Normally high

Synchronous clock phase:

The available selections here are:

1. Data read on rising edge
2. Data read on falling edge

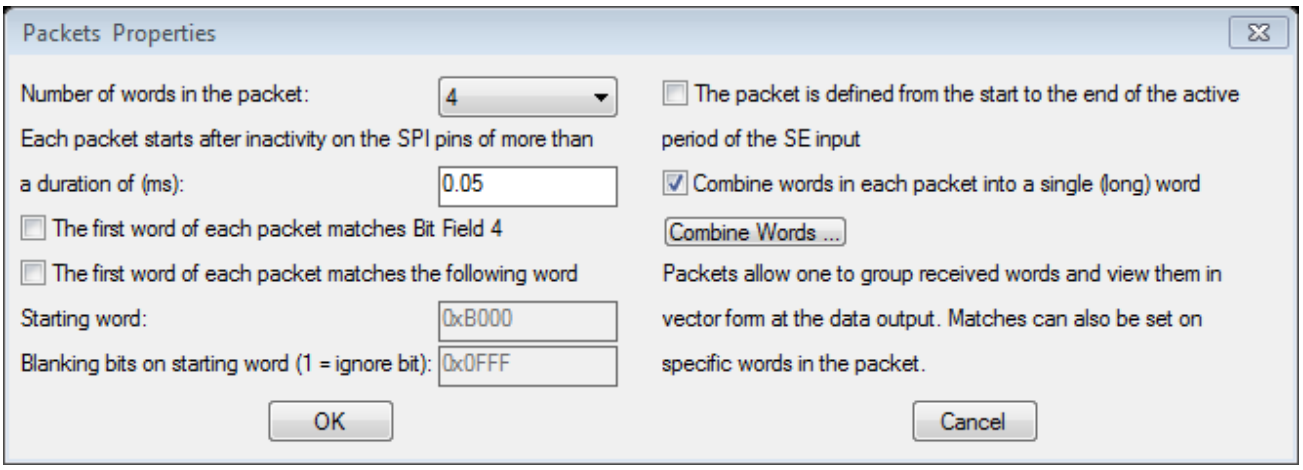
SE input active when:

The selection options here are:

1. Low
2. High
3. Not used

Decode a packet of words:

Check this if a packet of words is to be decoded. The following dialog will become available:



Number of words in the packet:

Select the package size from 1 to 16 words.

Each packet starts after inactivity on the SPI pins of more than a duration of (ms):

If the packet is not defined by the SE input or by a unique first word, then enter the required delay of bus inactivity before a packet is defined to start.

The first word of each packet matches Bit Field 4:

If this option is selected, then the requirements of the first word of the packet will be defined in the Bit Field 4 dialog.

The first word of each packet matches the following word:

If this option is selected, then the requirements of the first word of the packet will be defined by the following:

Starting word:

Enter the required value of the byte or word or otherwise which defines the start of the string (can be DEC, HEX or ASCII).
Values in decimal format need to be entered in the simple numbering format: 12.
Values in hexadecimal format need to be entered in the format: 0xC.
Values in ASCII format need to be entered in the format: “C”.

Blanking bits on starting word (1 = ignore bit):

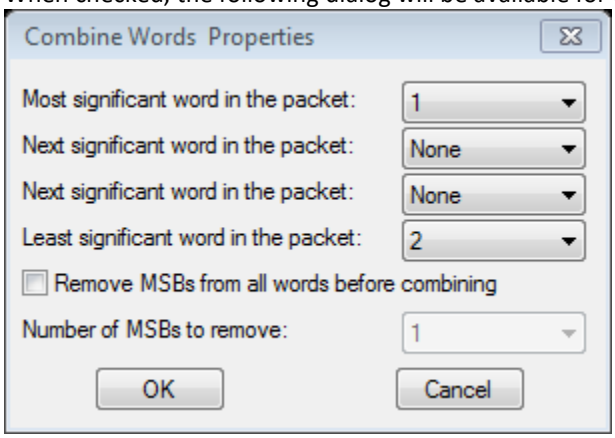
Enter the bits to be ignored in the starting word.

The packet is defined from the start to the end of the active period of the SE input:

Select this option if the packet starts with the change of the SE input and ends with the return of the SE input to its idle state.

Combine words in each packet:

When checked, the following dialog will be available for configuration:



Most significant word in the packet:

Select the word which will form the Most Significant part of the combined word.

Next significant word in the packet:

Select the word which will form the Next Significant part of the combined word.

Next significant word in the packet:

Select the word which will form the Third Significant part of the combined word.

Least significant word in the packet:

Select the word which will form the Least Significant part of the combined word.

Remove MSbs from all words before combining:

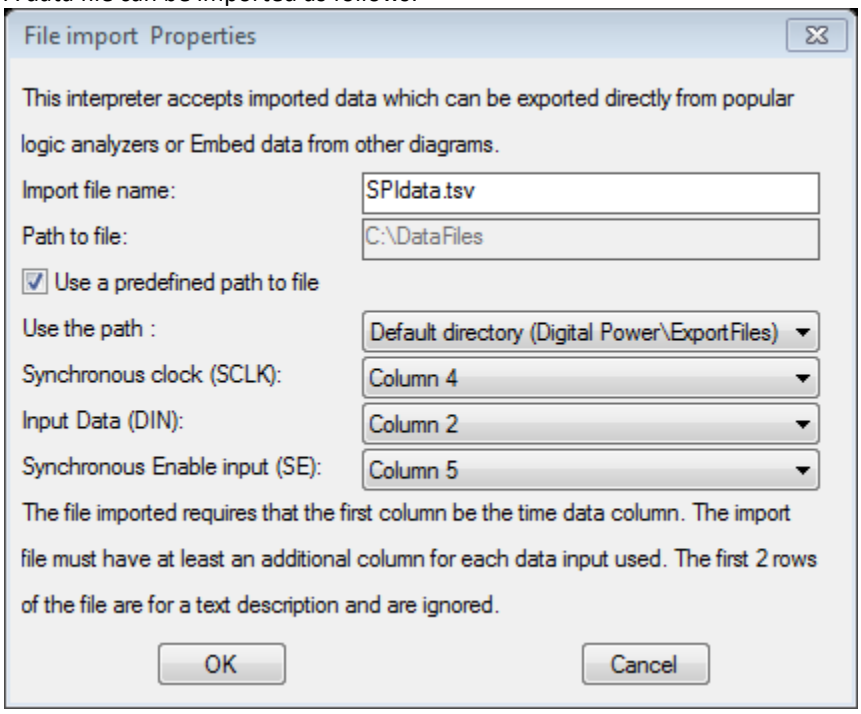
Select this if some of the bits in the words to be combined are coding bits and not data bits.

Number of MSbs to remove:

Select the number of most significant bits to be removed or ignored.

Use input file for data (disables input pins):

A data file can be imported as follows:



Import file name:

Enter the full file name of the import file.

Path to file:

Enter the file path (if not pre-defined below).

Use a predefined path to file:

Select this if the file is located in one of the pre-defined paths.

Use the path:

The pre-defined paths are:

4. Same directory as the embed diagram directory
5. User directory (Digital Power\User\files)
6. Default directory (Digital Power\ExportFiles)

Synchronous clock (SCLK):

Select which column in the import file which contains the synchronous clock data. Column 1 is always the time column.

Input Data (DIN):

Select which column in the import file which contains the synchronous data-in data.

Synchronous enable (SE):

Select which column in the import file which contains the synchronous enable data (if present).

Set the output trigger pin (Tr) to:

The are many possible selection options as detailed below:

1. the start of each word
2. the end of each word
3. start match of each packet

4. the end of each packet
5. a match on BF1
6. a match on BF2
7. a match on BF3
8. a match on BF4
9. a match on BF1 OR 2
10. a match on BF1,2 OR 3
11. a match on BF1,2,3 OR 4
12. a match on BF1 AND 2
13. a match on BF1,2 AND 3
14. a match on BF1,2,3 AND 4
15. BF1 and 2 OR BF3 and 4
16. the trigger of BF1
17. the trigger of BF2
18. the trigger of BF3
19. the trigger of BF4

The trigger output pin (Tr) willgo high (= 1) on the occurance of the selected trigger event.

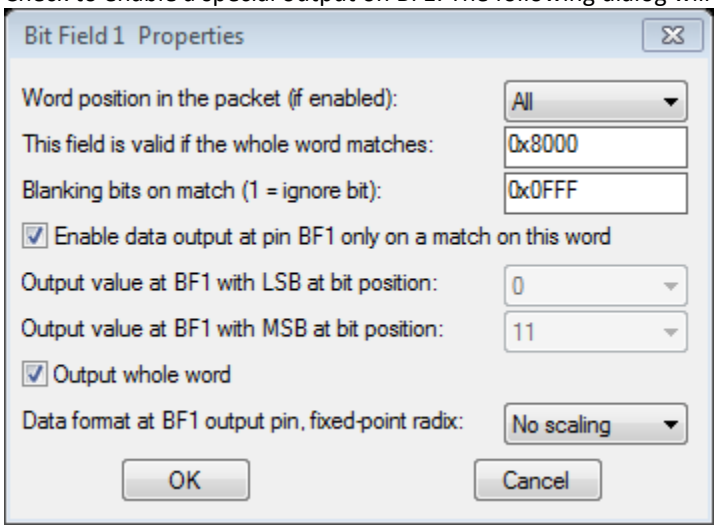
Set data pin output only on the selected trigger output:

When checked, the data at the output pin Data will be output only when the trigger as defined above occurs.

Bit Field Outputs:

Enable BF1 output:

Check to enable a special output on BF1. The following dialog will become available:



Word position in the packet (if packets are enabled):

Select the word in the packet to be analysed in this field dialog.

This field is valid if the whole word matches:

Enter the value of the byte or word or other which is to be compared and matched in this bit field. The value entered can be decimal, hexadecimal or ASCII.

Blanking bits on the match (1 = ignore bit):

Select any bits to be ignored in the field matching.

Enable data output at pin BF1 only on a match on this word:

Check this if the BF1 pin is to output only the fields of the matched words (e.g. the blanking bits can be used so that only words of a certain coding are outputted).

Output value at BF1 with LSB in position:

Select the position of the LSB of the required output field at BF1.

Output value at BF1 with MSB in position:

Select the position of the MSB of the required output field at BF1.

Output whole word:

Select this if the whole word is to be outputted at BF1 (the above LSB and MSB positions will be ignored).

Enable BF2 output:

Check to enable a special output on BF2. This bit field can be configured using an identical dialog to BF1 above and independently of BF1.

Enable BF3 output:

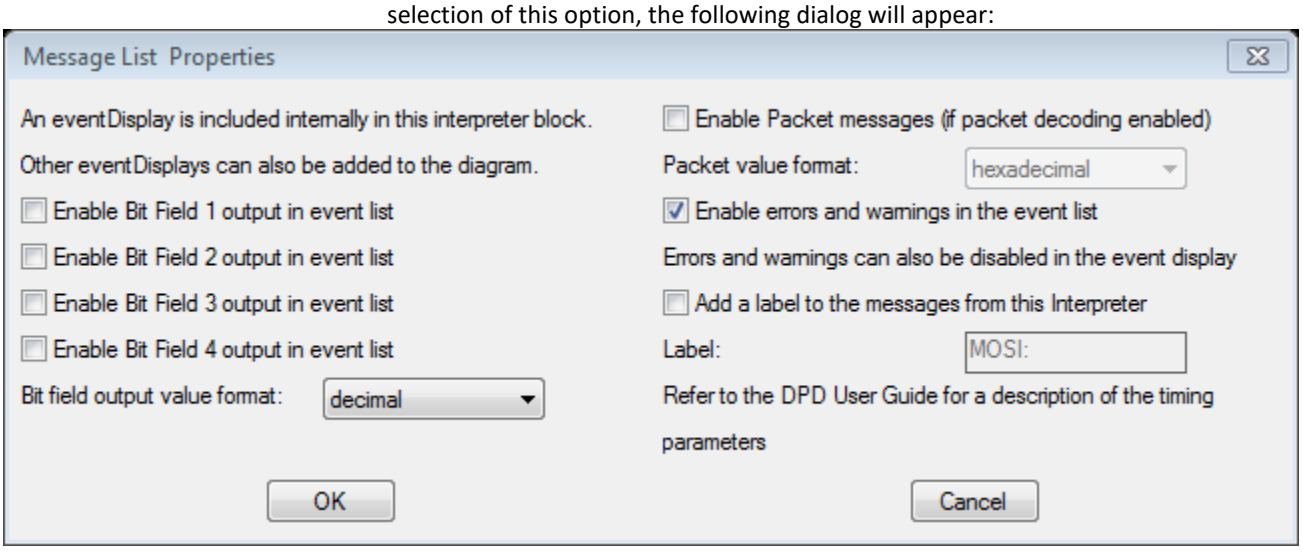
Check to enable a special output on BF3. This bit field can be configured using an identical dialog to BF1 above and independently of BF1.

Enable BF4 output:

Check to enable a special output on BF4. This bit field can be configured using an identical dialog to BF1 above and independently of BF1.

Enable Message List (Event display):

Check to enable the message list event display. One event display can be found internally in the block. Any number of event displays can be added to a diagram. On selection of this option, the following dialog will appear:



Enable Bit Field 1, 2, 3, 4 outputs in event list:

Select which Bit Fields output(s) are to be reported in the message list.

Bit Field output value format:

Select the output format of the bit fields in the message list. The options are:

1. decimal
2. hexadecimal
3. binary
4. ASCII
5. Decimal and hexadecimal

6. Decimal and binary
7. Decimal and ASCII
8. Decimal and hexadecimal and ASCII
9. scaled decimal

Enable Packet messages (if packets are enabled):

Select this if packets are enabled and packet messages are desired in the message list.

Packet value format:

In this case, the possible selections are:

1. decimal
2. hexadecimal
3. binary
4. ASCII

Enable errors and warnings in the event list:

Select this to enable errors and warnings in the event display. The errors and warnings can also be individually disabled in the event display.

Add a label to the messages from this interpreter:

Multiple interpreters may be used in the same diagram (for example for a MOSI and for a MISO decoding). All messages will be displayed on any one event display. In this case, a name can be given here to determine the source of the message.

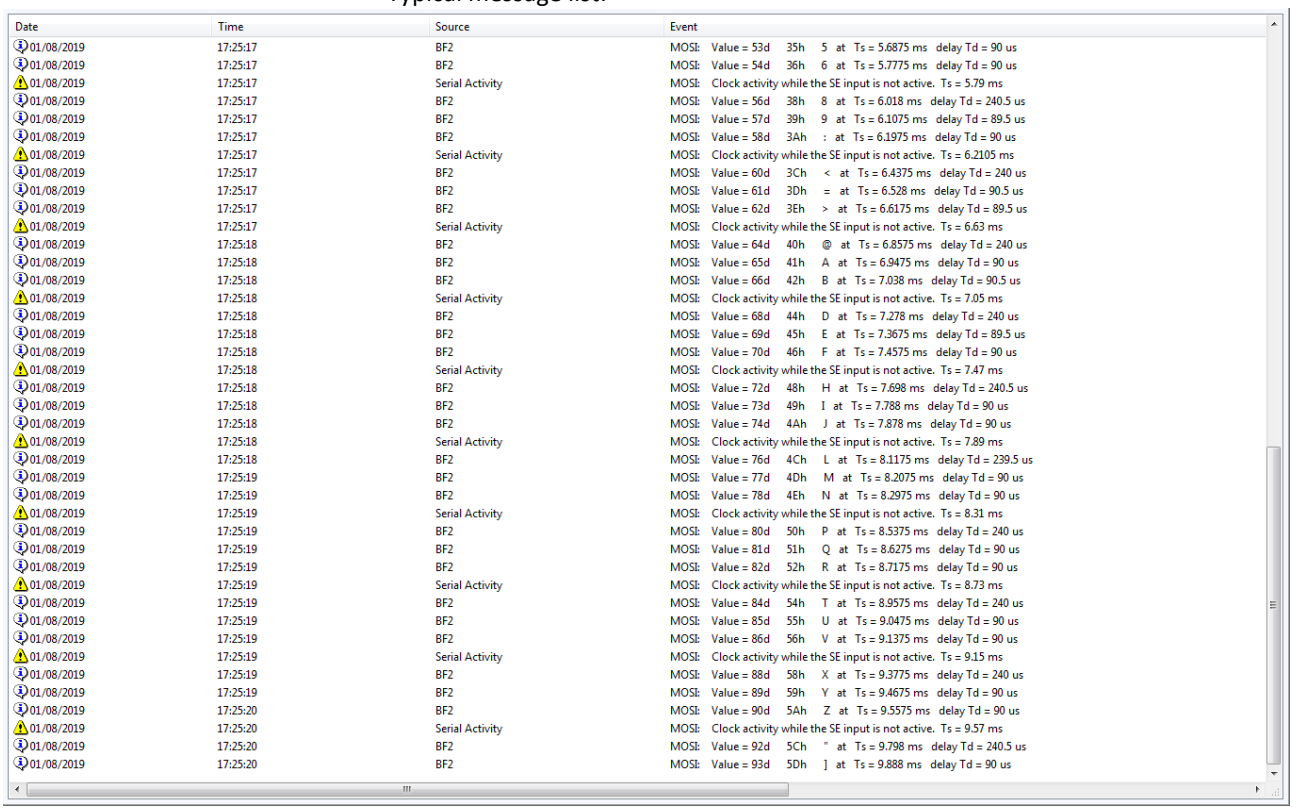
Label:

Enter the desired label.

Disable all functional errors:

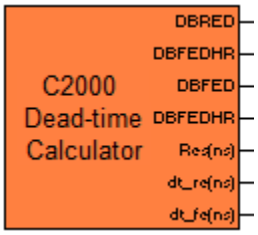
Select this to disable any error messages which can be due to errors in the interpretation or warnings of unexpected data.

Typical message list:



Date	Time	Source	Event
01/08/2019	17:25:17	BF2	MOSI: Value = 53d 35h 5 at Ts = 5.6875 ms delay Td = 90 us
01/08/2019	17:25:17	BF2	MOSI: Value = 54d 36h 6 at Ts = 5.7775 ms delay Td = 90 us
01/08/2019	17:25:17	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 5.79 ms
01/08/2019	17:25:17	BF2	MOSI: Value = 56d 38h 8 at Ts = 6.018 ms delay Td = 240.5 us
01/08/2019	17:25:17	BF2	MOSI: Value = 57d 39h 9 at Ts = 6.1075 ms delay Td = 89.5 us
01/08/2019	17:25:17	BF2	MOSI: Value = 58d 3Ah : at Ts = 6.1975 ms delay Td = 90 us
01/08/2019	17:25:17	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 6.2105 ms
01/08/2019	17:25:17	BF2	MOSI: Value = 60d 3Ch < at Ts = 6.4375 ms delay Td = 240 us
01/08/2019	17:25:17	BF2	MOSI: Value = 61d 3Dh = at Ts = 6.528 ms delay Td = 90.5 us
01/08/2019	17:25:17	BF2	MOSI: Value = 62d 3Eh > at Ts = 6.6175 ms delay Td = 89.5 us
01/08/2019	17:25:17	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 6.63 ms
01/08/2019	17:25:18	BF2	MOSI: Value = 64d 40h @ at Ts = 6.8575 ms delay Td = 240 us
01/08/2019	17:25:18	BF2	MOSI: Value = 65d 41h A at Ts = 6.9475 ms delay Td = 90 us
01/08/2019	17:25:18	BF2	MOSI: Value = 66d 42h B at Ts = 7.038 ms delay Td = 90.5 us
01/08/2019	17:25:18	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 7.05 ms
01/08/2019	17:25:18	BF2	MOSI: Value = 68d 44h D at Ts = 7.278 ms delay Td = 240 us
01/08/2019	17:25:18	BF2	MOSI: Value = 69d 45h E at Ts = 7.3675 ms delay Td = 89.5 us
01/08/2019	17:25:18	BF2	MOSI: Value = 70d 46h F at Ts = 7.4575 ms delay Td = 90 us
01/08/2019	17:25:18	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 7.47 ms
01/08/2019	17:25:18	BF2	MOSI: Value = 72d 48h H at Ts = 7.698 ms delay Td = 240.5 us
01/08/2019	17:25:18	BF2	MOSI: Value = 73d 49h I at Ts = 7.788 ms delay Td = 90 us
01/08/2019	17:25:18	BF2	MOSI: Value = 74d 4Ah J at Ts = 7.878 ms delay Td = 90 us
01/08/2019	17:25:18	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 7.89 ms
01/08/2019	17:25:18	BF2	MOSI: Value = 76d 4Ch L at Ts = 8.1175 ms delay Td = 239.5 us
01/08/2019	17:25:19	BF2	MOSI: Value = 77d 4Dh M at Ts = 8.2075 ms delay Td = 90 us
01/08/2019	17:25:19	BF2	MOSI: Value = 78d 4Eh N at Ts = 8.2975 ms delay Td = 90 us
01/08/2019	17:25:19	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 8.31 ms
01/08/2019	17:25:19	BF2	MOSI: Value = 80d 50h P at Ts = 8.5375 ms delay Td = 240 us
01/08/2019	17:25:19	BF2	MOSI: Value = 81d 51h Q at Ts = 8.6275 ms delay Td = 90 us
01/08/2019	17:25:19	BF2	MOSI: Value = 82d 52h R at Ts = 8.7175 ms delay Td = 90 us
01/08/2019	17:25:19	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 8.73 ms
01/08/2019	17:25:19	BF2	MOSI: Value = 84d 54h T at Ts = 8.9575 ms delay Td = 240 us
01/08/2019	17:25:19	BF2	MOSI: Value = 85d 55h U at Ts = 9.0475 ms delay Td = 90 us
01/08/2019	17:25:19	BF2	MOSI: Value = 86d 56h V at Ts = 9.1375 ms delay Td = 90 us
01/08/2019	17:25:19	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 9.15 ms
01/08/2019	17:25:19	BF2	MOSI: Value = 88d 58h X at Ts = 9.3775 ms delay Td = 240 us
01/08/2019	17:25:19	BF2	MOSI: Value = 89d 59h Y at Ts = 9.4675 ms delay Td = 90 us
01/08/2019	17:25:20	BF2	MOSI: Value = 90d 5Ah Z at Ts = 9.5575 ms delay Td = 90 us
01/08/2019	17:25:20	Serial Activity	MOSI: Clock activity while the SE input is not active. Ts = 9.57 ms
01/08/2019	17:25:20	BF2	MOSI: Value = 92d 5Ch " at Ts = 9.798 ms delay Td = 240.5 us
01/08/2019	17:25:20	BF2	MOSI: Value = 93d 5Dh] at Ts = 9.888 ms delay Td = 90 us

Peripherals



Dead-time Calculator (TI C2000)

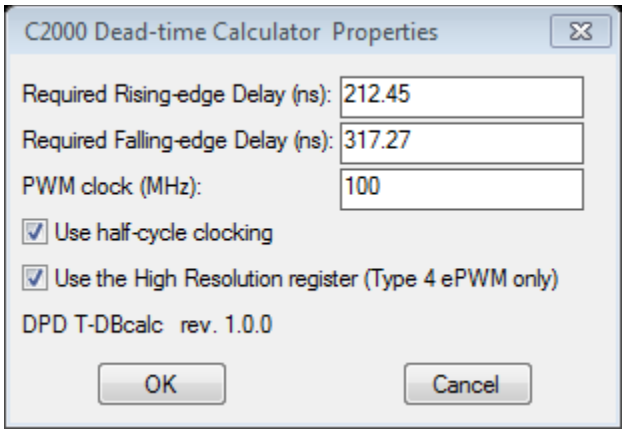
Calculates the actual dead-time and required dead-time register values for a given configuration.

Output pins:

DBRED	Outputs the required value of the DBRED register.
DBREDHR	Outputs the required value of the DBREDHR register.
DBFED	Outputs the required value of the DBFED register.
DBFEDHR	Outputs the required value of the DBFEDHR register.
Res (ns)	Bit field output as configured internally in the block dialog.
Dt_re (ns)	The actual value of the rising-edge dead-band as configured in nano-seconds.
Dt_fe (ns)	The actual value of the falling-edge dead-band as configured in nano-seconds.

Dialog properties:

The Dead-time Calculator block properties menu is shown in the following figure which appears when right-clicking on the block.



Required rising-edge delay (ns):

Enter the required dead-time delay on the rising edge in nano-seconds.

Required falling-edge delay (ns):

Enter the required dead-time delay on the falling edge in nano-seconds.

PWM clock (MHz):

Enter the frequency of the PWM clock in MHz.

Use half-cycle clocking:

Select this if double-resolution half-cycle clocking is required (this is necessary for high-resolution dead-band.

Use the high resolution register:

Select this if high-resolution dead-band is to be implemented.

Frequency Response Analysis

The frequency response analysis section contains tools in order to perform frequency response analyses on any of the converter diagrams and their respective control loops within the digital power designer block set.

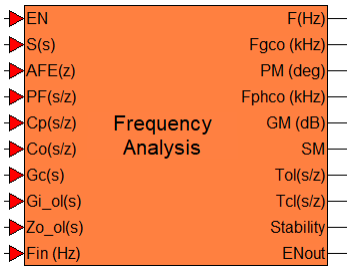
The tools come in two distinct categories:

1. Analytical calculations using given models
2. Frequency (AC-sweep) analysis measuring the frequency response of the switching converter simulation diagrams.

The frequency analysis tool falls into the first category and requires specialised simulation blocks with the built-in analytical models. This section is considered to be in a beta format and the number of analytical models are at the moment rather limited and are intended to be expanded upon in future releases.

The analytical models will perform quite fast analyses over many frequency points in order to analyse control loops. The frequency response analysis can be combined within the simulation environment where the time response can be simulated and checked in the same diagram and simulation run as the frequency response analysis (at separate time instances). With this type of analysis, it is not necessary to maintain a small time-step usually required for the time-domain simulations.

The FRA tool falls into the second category and performs an AC-sweep over many simulation runs. The simulation run management is totally automated and the frequency and amplitude of the injection signal will be incremented according to the selected distribution at each simulation run. With this type of tool, it is necessary to maintain the smaller simulation time step, as required for the simulations in the time domain.



Model-based Frequency Analysis (MBFA)

This block, when inserted in a diagram can calculate the open-loop and closed-loop frequency response of a power converter control loop. The blocks used in the diagram must contain the frequency response models. From the calculated response using the models, the stability margins can be calculated including the gain cross-over frequency (Fgco), phase cross-over frequency (Fphco), phase margin (PM), gain margin (GM) and the stability margin (SM) of the Nyquist diagram. Alternatively to using models, the inputs can also be data files imported using the Frequency Response Import block of AC sweeps performed using either FRA block in Embed or Embed Co-sim with PSIM or AC sweeps performed directly in PSIM and exporting the PSIM FRA file.

The bode plots and Nyquist plot will be generated internally in the block along with an indication of the loop stability.

In general, the conditions for stability used within the block are that the phase margin must be ≥ 45°, the gain margin must be ≥ 8dB and the stability margin ≥ 0.5.

The closed loop response, output impedance and input-to-output attenuation (audio susceptibility) are also calculated and plotted internally in the block.

Input pins:

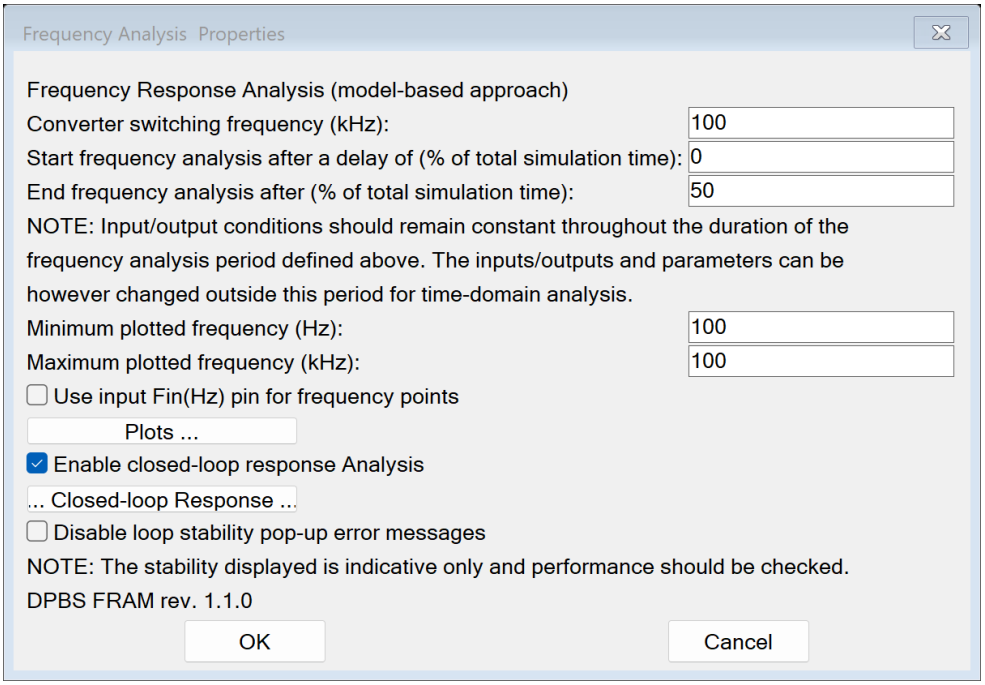
EN Enable input to enable the frequency response analysis.

S(s) The loop feedback sensor transfer function input.

	AFE(z)	The ADC front end transfer function input (digital control loops only).
	PF(s/z)	Pre-filter (or other) transfer function input.
	Cp(s/z)	The compensator transfer function input.
	Co(s/z)	The controller (PWM) transfer function input.
	Gc(s)	The converter control-to-output transfer function input.
	Gi_ol(s)	The converter input-to-output transfer function input.
	Zo_ol(s)	The converter output impedance transfer function input.
	Fin(Hz)	An optional frequency input which can be used when simultaneously analysing multiple loops with the frequency input at this pin from the master MBFA block.
Output pins:	**F(Hz)**	The frequency being used for the analysis in Hz.
	Fgco(kHz)	The calculated gain cross-over frequency in kHz.
	PM (deg)	The phase margin in degrees.
	Fphco (kHz)	The calculated phase cross-over frequency in kHz.
	GM (dB)	The gain margin in dB.
	SM	The stability margin (from the Nyquist plot).
	Tol(s/z)	The open-loop transfer function output.
	Tcl(s/z)	The closed-loop transfer function output.
	Stability	A stability output. This is an indication only, based upon the calculated stability margins.
	ENout	Enable output used to enable other MBFA blocks in multi-loop analyses.

Dialog properties:

The frequency analysis block properties menu is shown in the following figure which appears when right-clicking on the block.



Converter switching frequency:

Enter the converter switching frequency in kHz.

Start frequency analysis after delay:

Enter the value in percent of the total simulation time at which the frequency analysis should commence within the simulation run.

End frequency analysis after:

Enter the value in percent of the total simulation time at which the frequency analysis should end within the simulation run.
During the frequency analysis period, the simulation conditions should remain stable. Outside of this period, variations can be made for time-domain analysis.

Minimum frequency to analyse:

Enter the minimum or start frequency for the frequency analysis.

Maximum frequency to analyse:

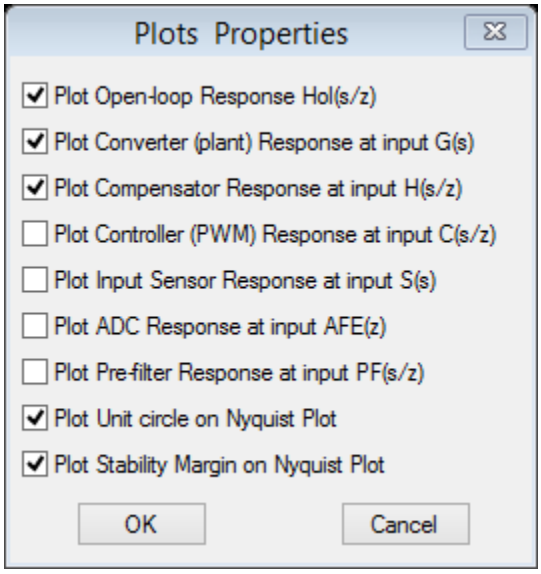
Enter the maximum or end frequency for the frequency analysis.

Use input Fin pin for frequency points:

Select this option if this MBFA block is to be set as a slave in a multi-loop analysis. The frequency should be input from another MBFA block acting as a master in the analysis.

Plots:

The type of plots to view can be selected as below:

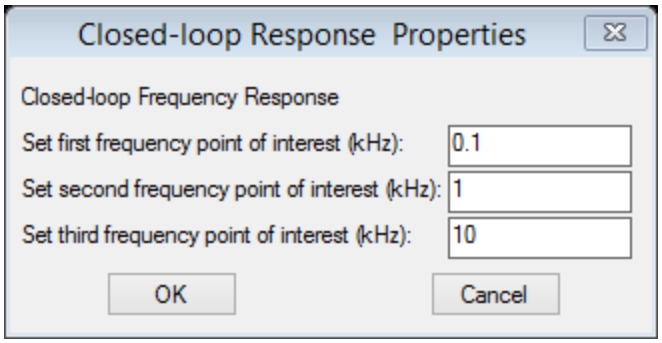


Enable Closed-loop response analysis:

Will enable the closed-loop, output impedance and input-to-output attenuation plots.

Closed-loop response:

The closed-loop response can be enabled and three points of interest selected for the input-to-output attenuation.

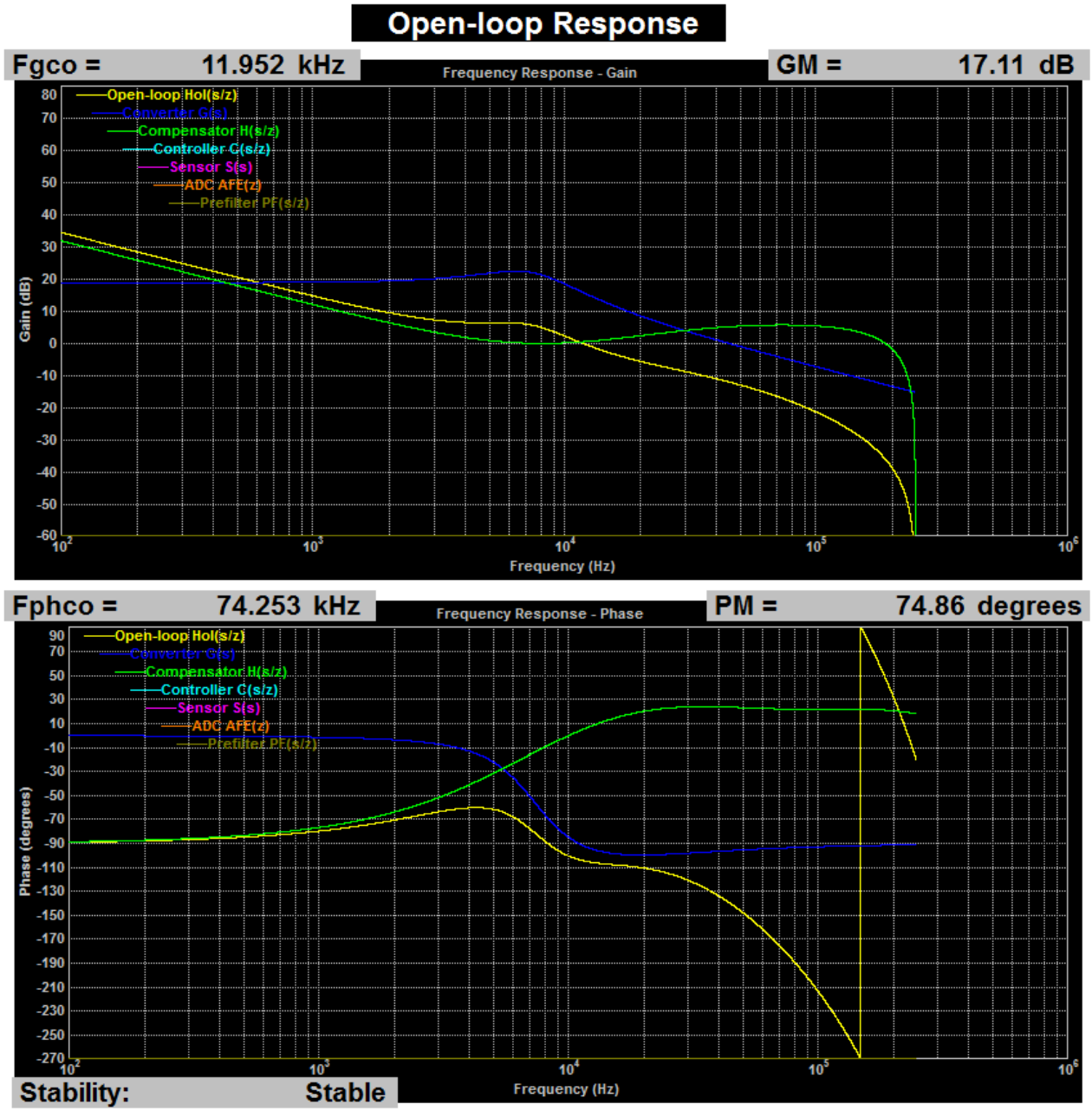


Disable loop stability pop-up messages:

Select this option to disable the pop-ups related to the loop stability. If performing an open-loop analysis or simply plotting the characteristic response, the loop stability messages are not of interest.

Examples of generated plots by this model-based approach for the buck converter with voltage-mode control are given in the following figures.

Bode plot:



The open-loop response (yellow trace) is calculated internally and is given by:

$$T_{ol}(s) = H(s).G(s)$$

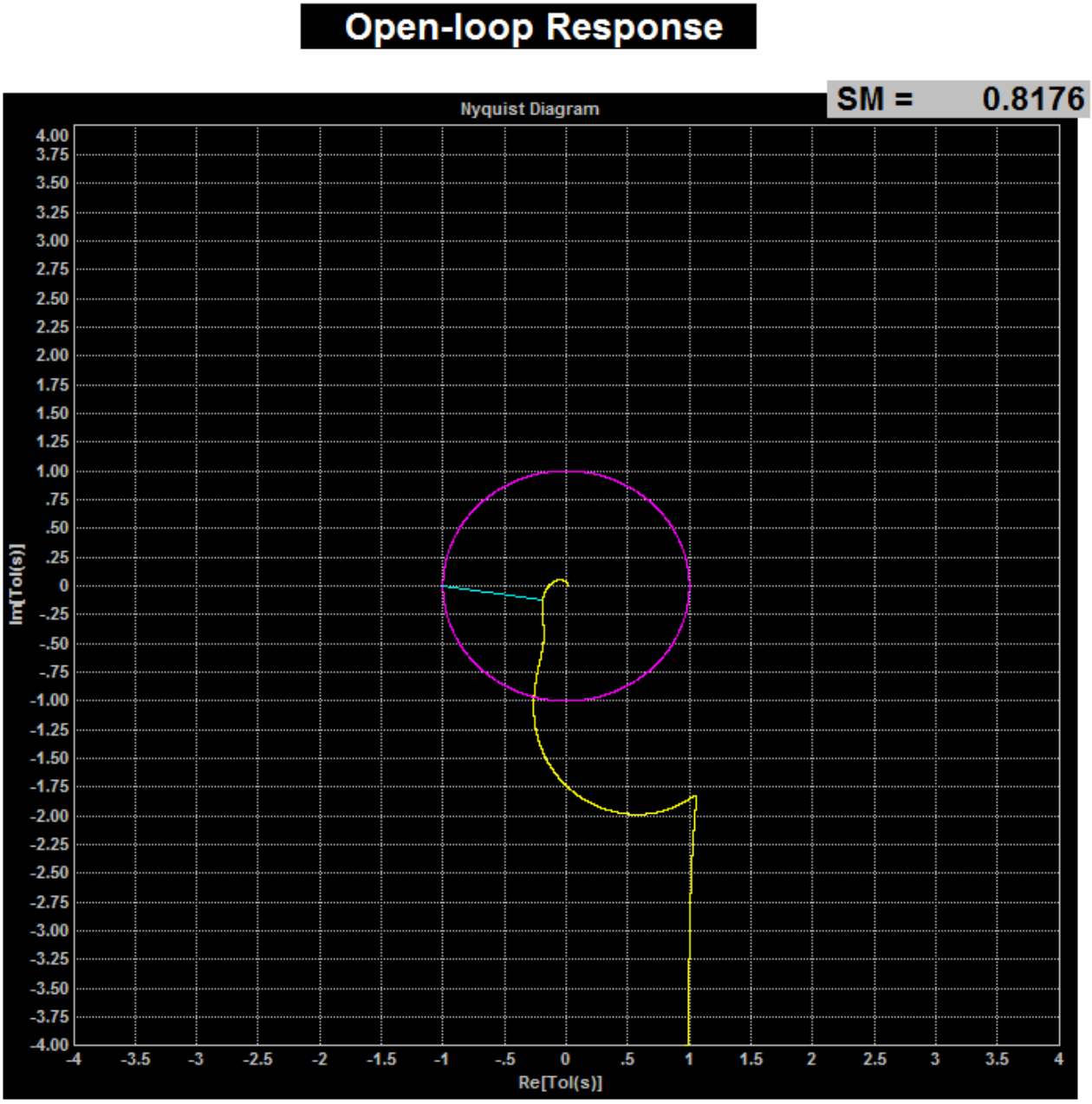
where:

$$G(s) = Gc(s) * Co(s) * Cp(s)$$

and

$$H(s) = S(s) * AFE(s) * PF(s)$$

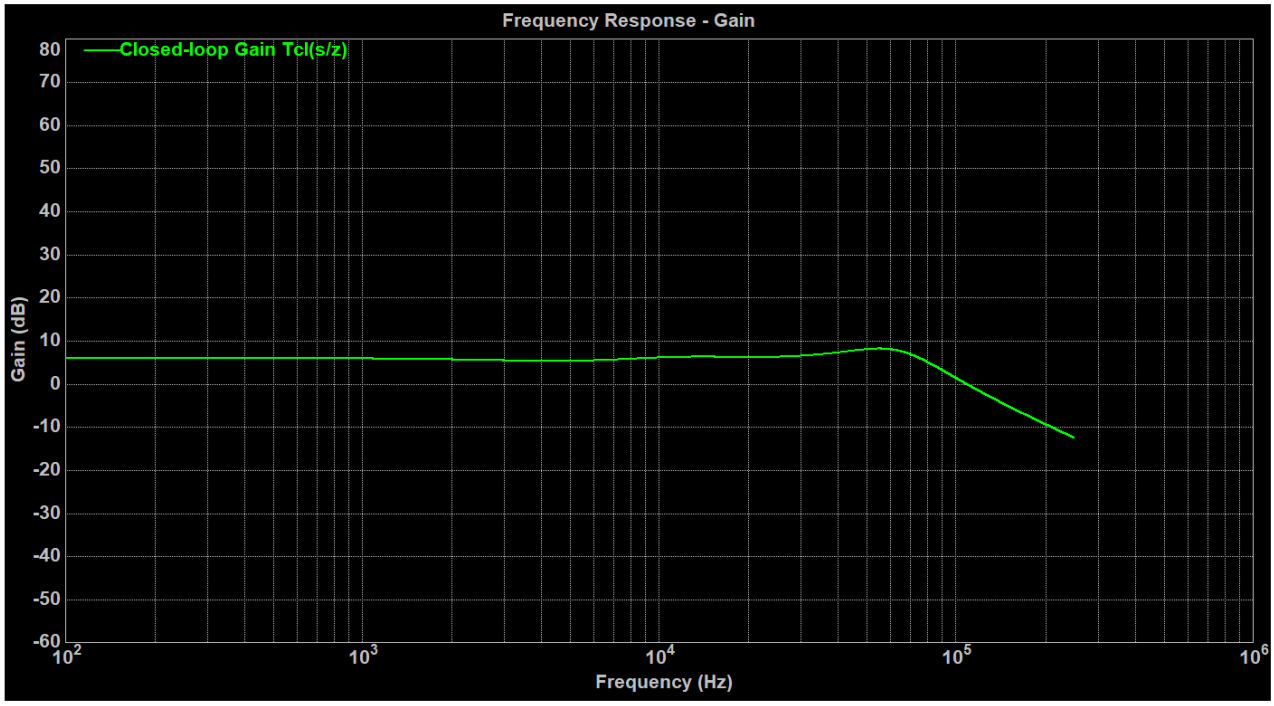
Nyquist plot:

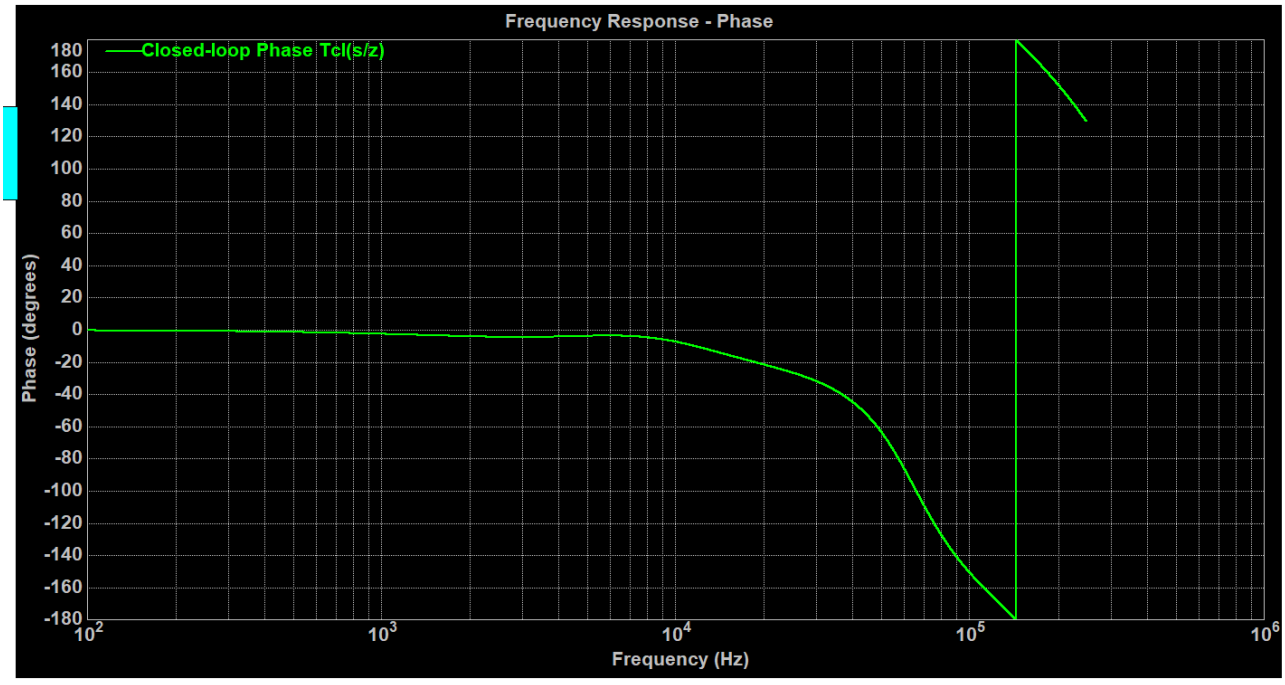


The pink trace is the unit circle which can be disabled if desired. The light blue trace is the stability margin (SM) which is the shortest distance from the yellow Nyquist trace to the instability point at (-1,0).

Closed-loop response:

Closed-loop Response

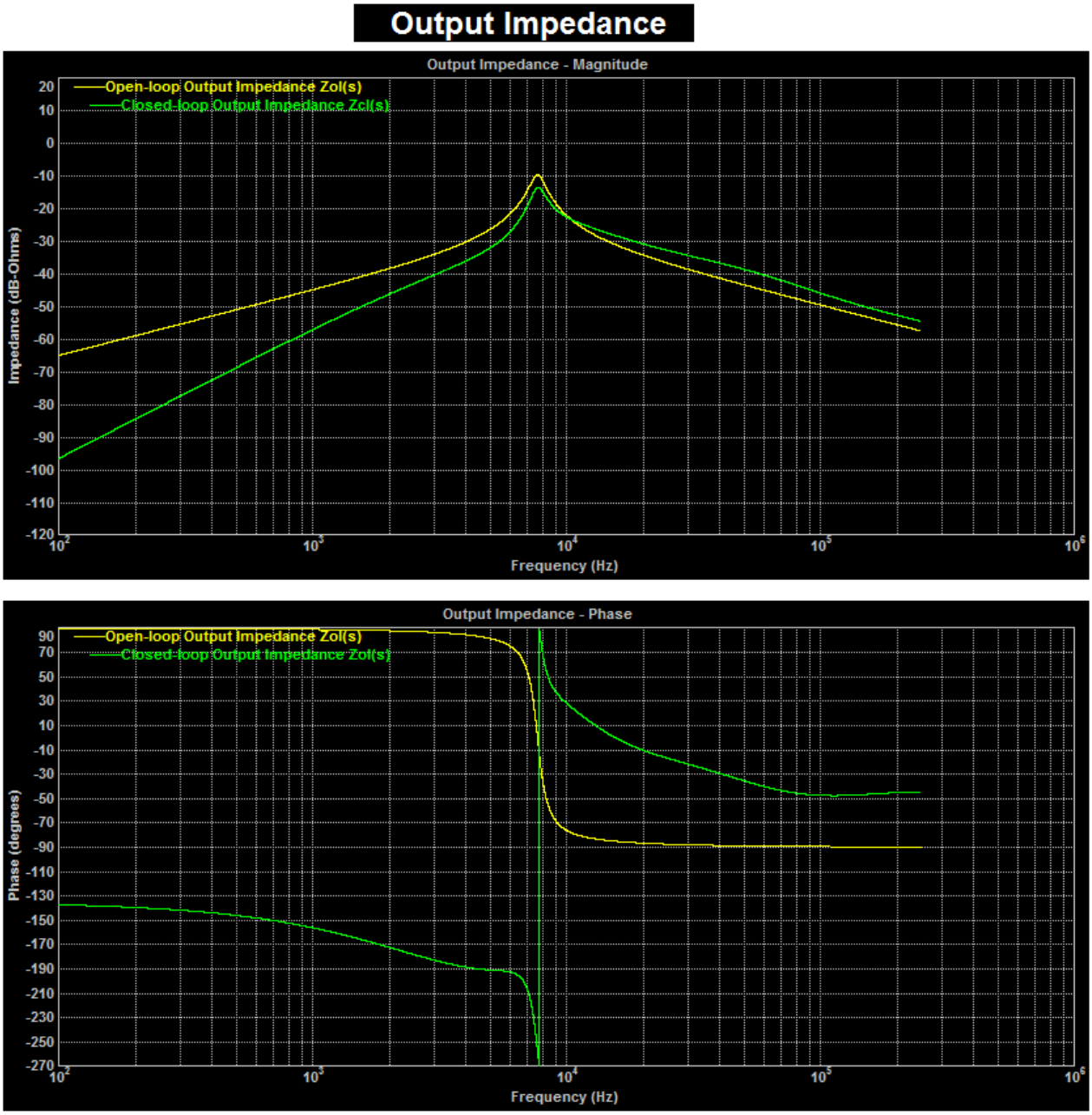




The closed-loop response is calculated internally according to the following:

$$T_{cl}(s) = \frac{G(s)}{1+H(s).G(s)} = \frac{G(s)}{1+T_{ol}(s)}$$

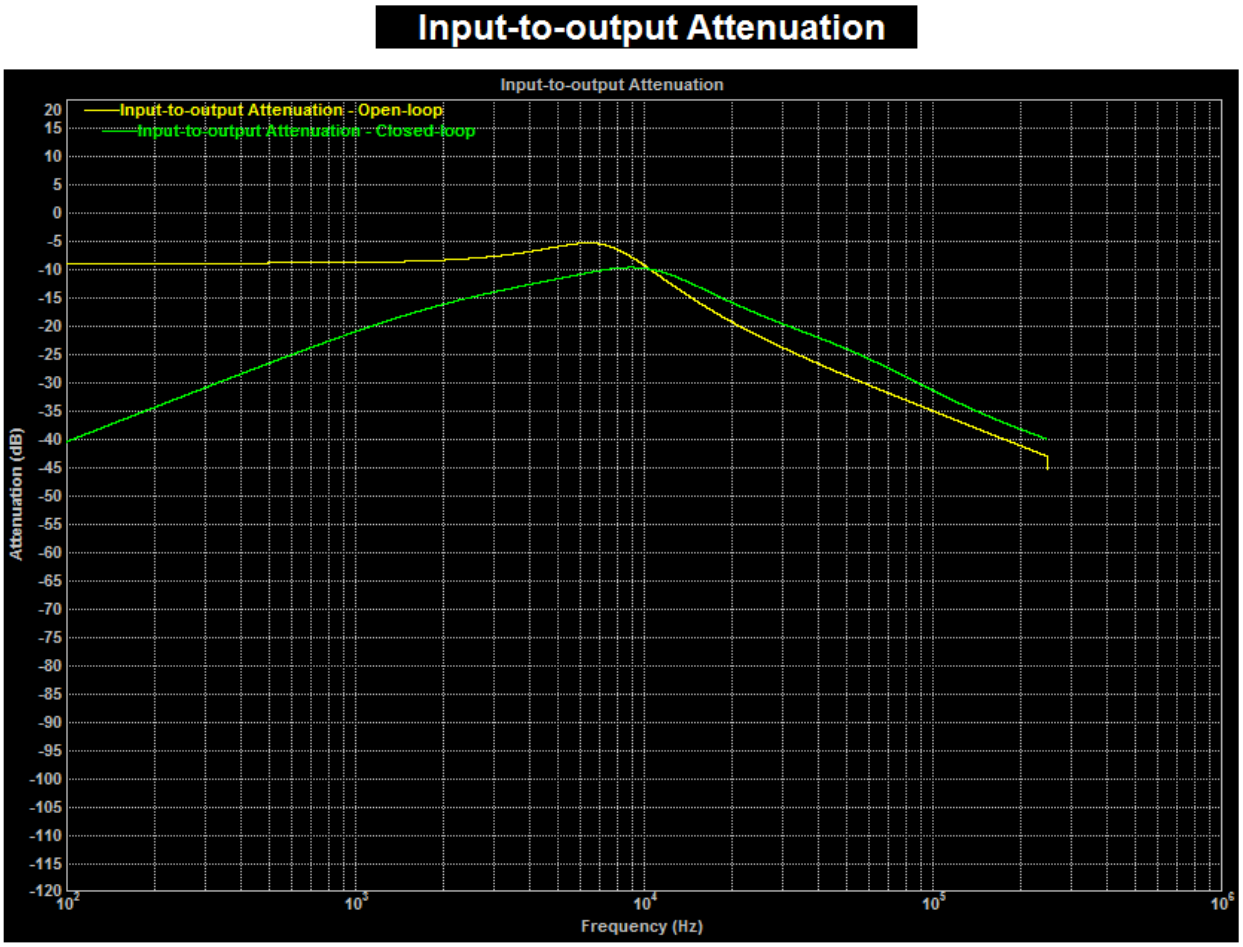
Output impedance:



The open-loop output impedance is input at the Zo_ol(s) pin. The closed-loop output impedance is calculated internally using the open-loop output impedance as follows:

$$Z_{cl}(s) = \frac{Z_{ol}(s)}{1+T_{ol}(s)}$$

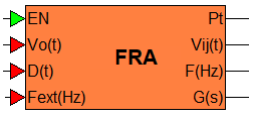
Input-to-output attenuation:



	Closed-loop Input-to-Output Attenuation (dB)
Point 1	-40.3875 at F = 0.1 kHz
Point 2	-20.9188 at F = 1 kHz
Point 3	-9.64292 at F = 10 kHz

The open-loop input-to-output response of the system is input at the Gi_ol(s) pin. This is used to plot the attenuation in this plot. The closed-loop input-to-output response is calculated internally using the open-loop input-to-output response as follows:

$$Gio_{cl}(s) = \frac{Gio_{ol}(s)}{1 + T_{ol}(s)}$$



Frequency Response Analyser (FRA)

The frequency response analyser block performs AC sweeps in order to measure the frequency response of control loops or components.

Input pins:

EN Enable input in order to enable the frequency response AC sweep. If disabled in a diagram, the control loop can be simulated in the time domain as normal with the injected signal disabled.

Vo(t) The output voltage response input of the excited loop.

D(t) The duty cycle or modulation input response to the signal injection.

Fext(Hz) Input pin to use an externally generated frequency if the duty cycle input pin D(t) is enabled.

Output pins:

Pt The programmed point currently in execution (run count).

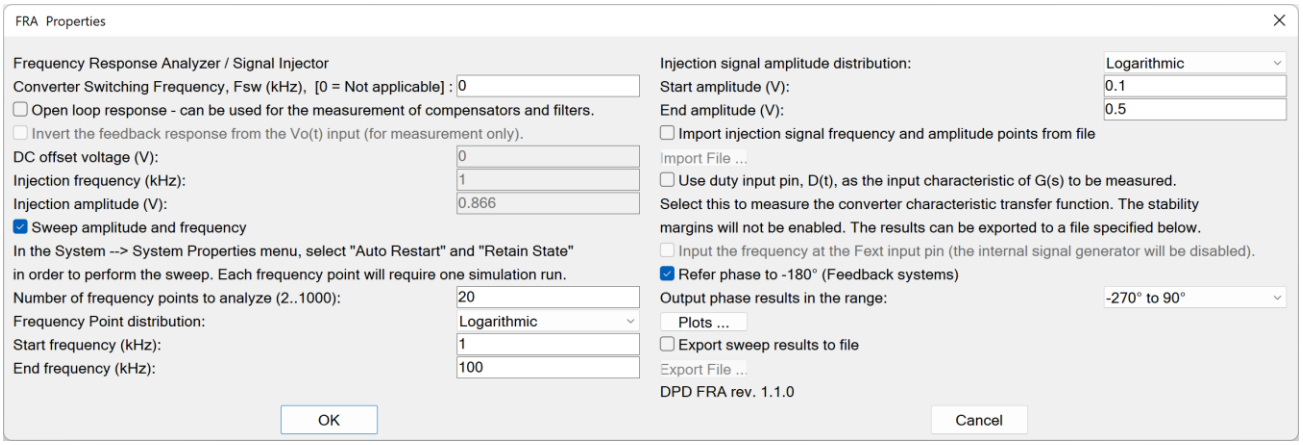
Vij(t) The vector sum of the loop output coming in at the input pin, Vo(t), and internal the injection (excitation) signal to be reconnected into the loop.

F(Hz) The injection signal frequency currently in execution, in Hz.

G (s) The measured transfer function output at the current injection frequency.

Dialog properties:

The FRA block properties menu is shown in the following figure which appears when right-clicking on the block.



Converter switching frequency:

Enter the switching frequency in kHz of the converter being analysed. Entering a value of zero will disable any switching frequency related functions or messages.

Open-loop response:

Select this if an open-loop response is desired to be measured. Note that for power converter loops, a closed-loop response must be used for the analysis and the open-loop response is automatically extracted from this.

Invert response measurement at Vo(t) input pin:

Feedback loops normally have a negative gain. When performing an open-loop sweep, the negative gain can be emulated by selecting this option for comparison with closed-loop systems.

DC offset voltage:

In the case of an open-loop analysis, a DC offset may be added to the injected signal.

Injection frequency (kHz):

This option is enabled only if “sweep amplitude and frequency” is not selected below. Input the desired injection frequency in kHz, only a single simulation run will be performed.

Injection amplitude (V):

Again, this option is enabled only if “sweep amplitude and frequency” is not selected below. Input the desired injection amplitude in V, only a single simulation run will be performed. Note that if the FRA is used to inject current such as for converter closed-loop impedance measurements, then this injection amplitude will be in A.

Sweep amplitude and frequency:

Select this option if the open-loop transfer function (or other) is to be measured over a range of frequencies. The simulation will be performed over multiple runs according to the number of desired points.

Number of frequency points to analyse:

Enter the desired number of frequency points to be analysed and plotted. This will also apply if the import table is used. It is recommended to use around 20 to 30 points. If a more accurate measurement of the gain cross-over frequency is desired and hence the phase margin, a second analysis can be performed using a minimum of two points, either side of the cross-over frequency. Extrapolation is used to approximate the phase margin and the closer the two points are to the cross-over frequency, the more accurate the measurement.

Frequency point distribution:

Enter either a linear or logarithmic distribution. A distribution based upon tabled values can be entered as below.

Start frequency:

Enter the desired start frequency of the frequency sweep analysis in Hz.

End frequency:

Enter the desired end frequency of the frequency sweep analysis in kHz.

Injection signal Amplitude distribution:

Enter either a linear or logarithmic distribution. A distribution based upon tabled values can be entered as below.

Start amplitude:

Enter the start amplitude of the injection signal, applied at the first frequency point.

End amplitude:

Enter the end amplitude of the injection signal, applied at the first frequency point.

Import injection signal amplitude and frequency from file:

Select this option if it is desired to use a tabled format of frequency points and the corresponding injection signal amplitude. The number of rows of data in the import file must be at least equal to the number of frequency points.
The tabled format may be necessary in order to get a good stability of the converter loop over the entire sweep frequency range, since the open-loop gain of the converter will normally vary significantly (several orders of magnitude) over that range.

Use duty cycle input pin:

Select this option if it is desired to measure the response at some other point in the control loop. In this way, the control-to-output transfer function can be measured or the compensator transfer function. This function is equivalent to 3-input commercial frequency response analysers.

Input the frequency at the F_{ext} input pin:

This option becomes available if the “Use duty cycle input pin” option is enabled above. In this case, multiple FRA blocks may be placed in a diagram, simultaneously calculating the frequency response of various sections of the control loop diagram. The internal control of the signal generator will be disabled and controlled using this input pin, the FRA block becomes the slave and a master FRA block, or other frequency controller, is required in the diagram. Only a master FRA block will determine when a simulation run is re-started (moves to the next injection frequency or point to plot).

Refer phase to -180°:

The FRA measures the true phase between the input excitation and output response. In feedback systems it is typical to analyse the open-loop gain, GH. However, the measured response within a feedback loop will in fact be -GH due to the negative feedback of the loop. Select this option to refer the phase to -180° as is traditional for analysing the stability of control-loops.

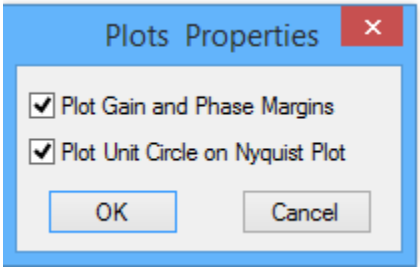
Output phase results in the range:

There are three ranges which can be selected for the phase output to the plots, output pins and the file export:

1. -180° to 180°
2. 90° to -270°
3. 0° to -360°

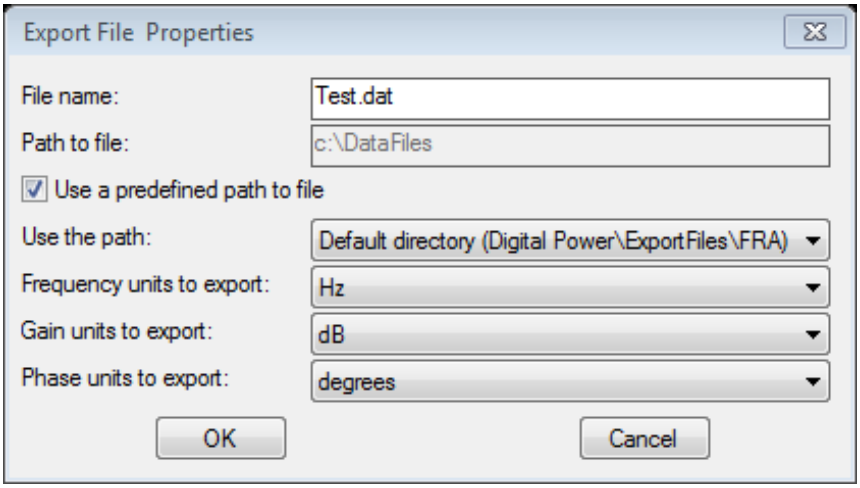
Plots:

Enter the desired plotting options. The plots can also be changed manually within the block by right clicking on them to bring up the plot properties.



Export sweep results to file:

Select this option in order to export the analysis results to a file. The frequency, gain and phase will be exported for each point in the units as selected.



File name and path:

Enter the complete path of the export file. If no path is included, the file must be in the same directory as the main diagram.

Frequency units:

Select either Hz or kHz to be written to the file.

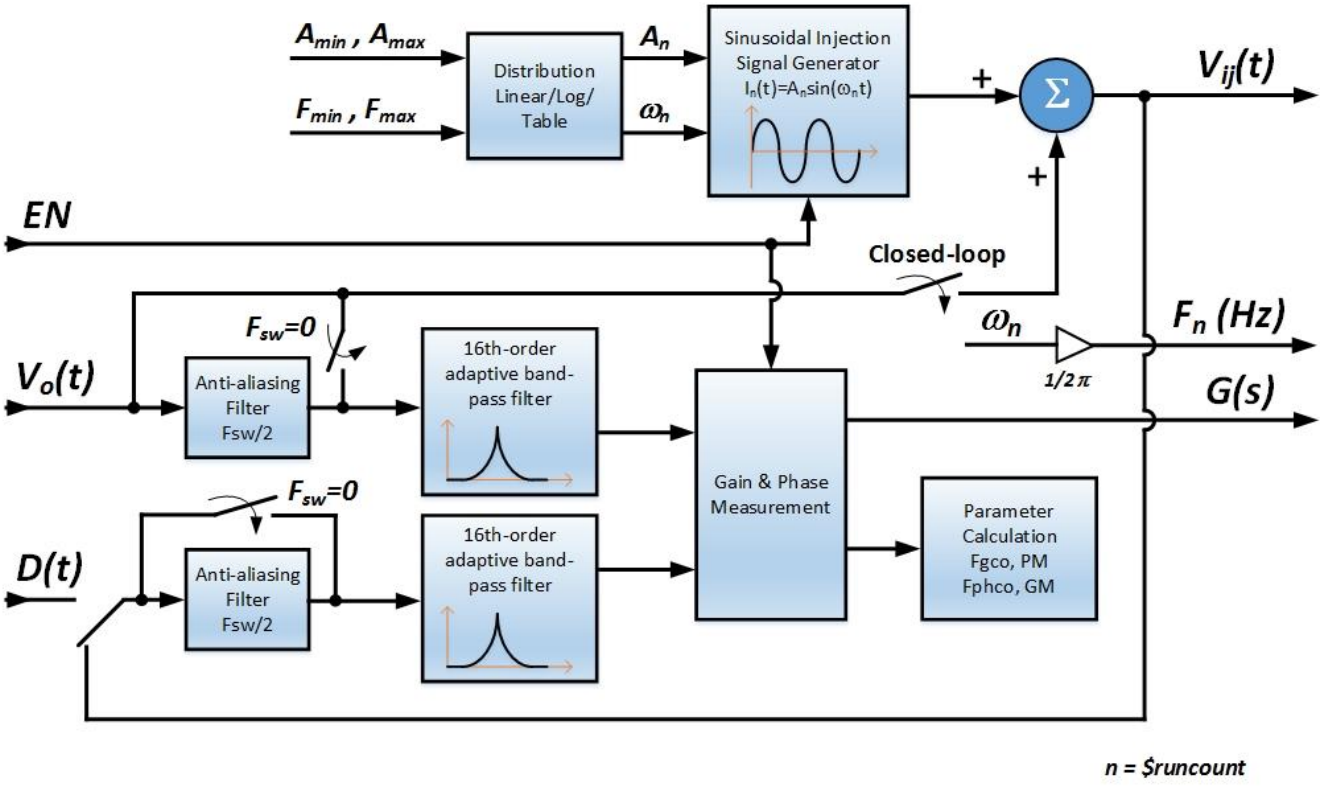
Amplitude units:

Select the desired transfer function gain units to be written to the file, unit-less or in dB.

Phase units:

Select the desired phase unit, rad/s or degrees, to be written to the file.

The operation of the Frequency Response Analyser is outlined in the diagram below.



The analyser injects a single frequency sinewave into the control loop for each simulation run. For every desired frequency point, there will be a simulation run. A simulation run stops and moves on to the next run and injection frequency (and amplitude) as soon as it has been determined that a stable frequency response has been measured. If, after reaching the set simulation end time, a stable frequency response has not been determined, a pop-up message will be shown to this respect, though the next simulation runs will continue. The gain and phase calculation will perform a best-fit even if stability was not determined during the run. To achieve stability at one injection frequency over one simulation run, the amplitude of the input signal and the measured response signal must both be maintained within ±5% over each measured period of the injected signal for a minimum of 5 consecutive periods. This is after a settling-down period of 4 injected frequency periods. The end time of the simulation must be set to at least 15 periods of the minimum frequency to be injected.

The loop can be opened for measuring the frequency response of blocks that do not require closed-loop operation during analysis. Examples are compensators and filters.

With commercial frequency response analysers on the hardware of power converters, the injected signal must normally be applied at a point of low impedance for the measured feedback and high impedance for the injection input. This is usually at the output of the power converter, if the loop signal cannot be buffered to a low impedance in some way. This requirement is not the case within the simulation environment of the digital power designer because the injection

signal is injected in a summing junction which does not affect the impedance at the point of injection within the simulation. Therefore, the injection signal can be applied at other points in the loop if they are more convenient. An example of this is multiple-loop feedback such as the two loops in average current-mode control. A point in the control loop must be found where the entire loop response can be seen and the injection signal applied to the entire loop.

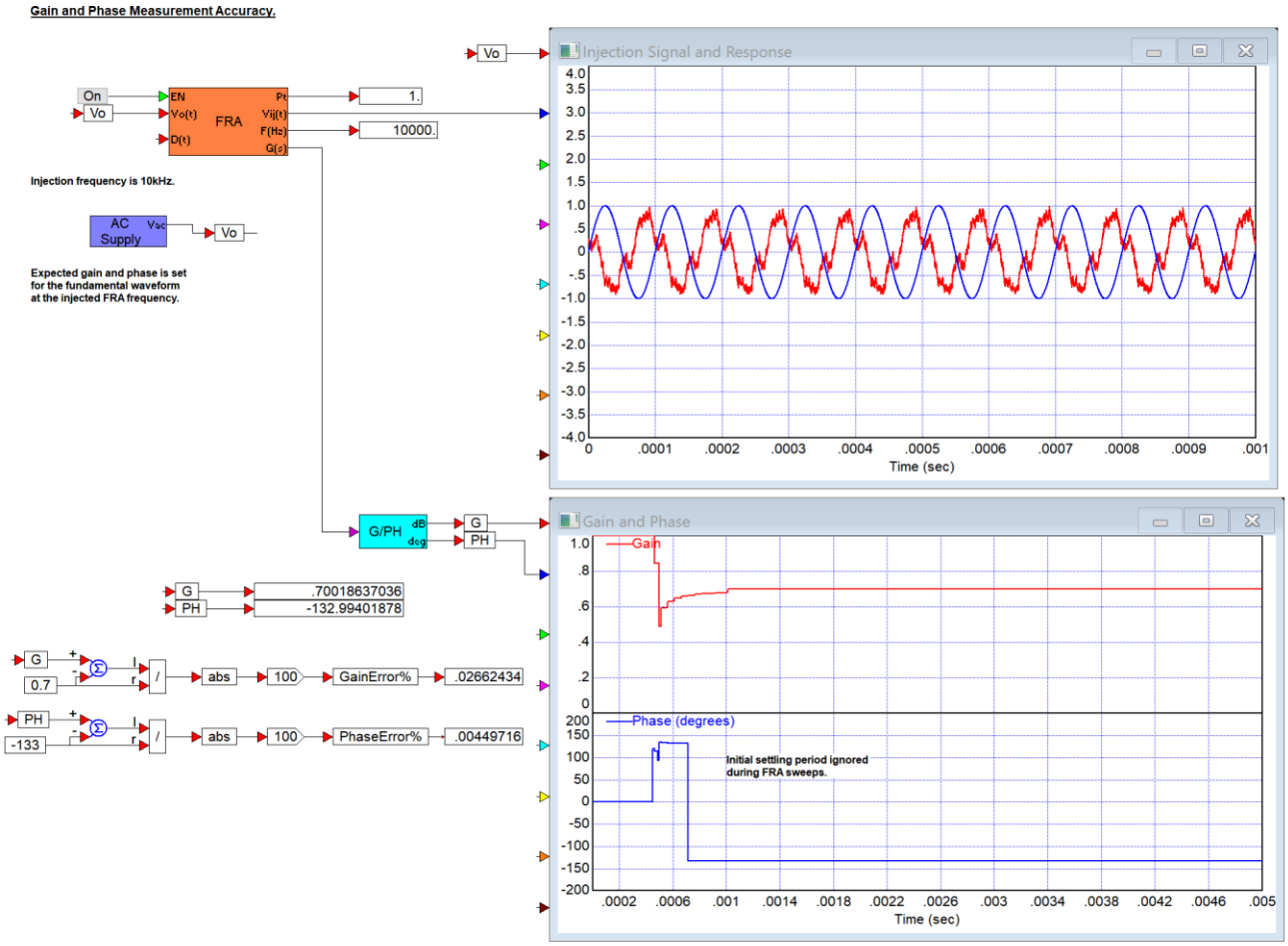
The FRA block must be placed in a series connection in the control loop, with the feedback response of the loop being measured at the input pin Vo(t) and the output of the FRA $V_{ij}(t)$, connected to the broken point of the control loop in order to reclose the loop. As an alternative method, the loop can be completely opened externally to this block and a DC offset added to the FRA $V_{ij}(t)$ injection output in order to keep the loop at its nominal operating point. The FRA should be set for open-loop response in this case. The FRA response should be identical to the case when performed with the loop closed.

It is important that the control loop remains stable during the measurement and this can be guaranteed by the correct selection of the injection amplitude. Also, the loop response must remain linear and this basically means that there must be no saturation of the loop during the analysis. The converter output voltage must remain within limits and the modulation signal must not go too near the zero or the peak value of the ramp amplitude for the PWM. The limits of compensators etc can be increased if necessary. It is therefore recommended to view the relative measurements of the FRA output and input on a plot in the time-domain while performing the frequency analysis.

If the modulation signal (before the PWM stage) is connected to the D(t) input, the converter control-to-output transfer function can be measured.

The FRA block can also be used to inject a current signal in order to measure, for example, input and output impedances or trans-conductance transfer functions.

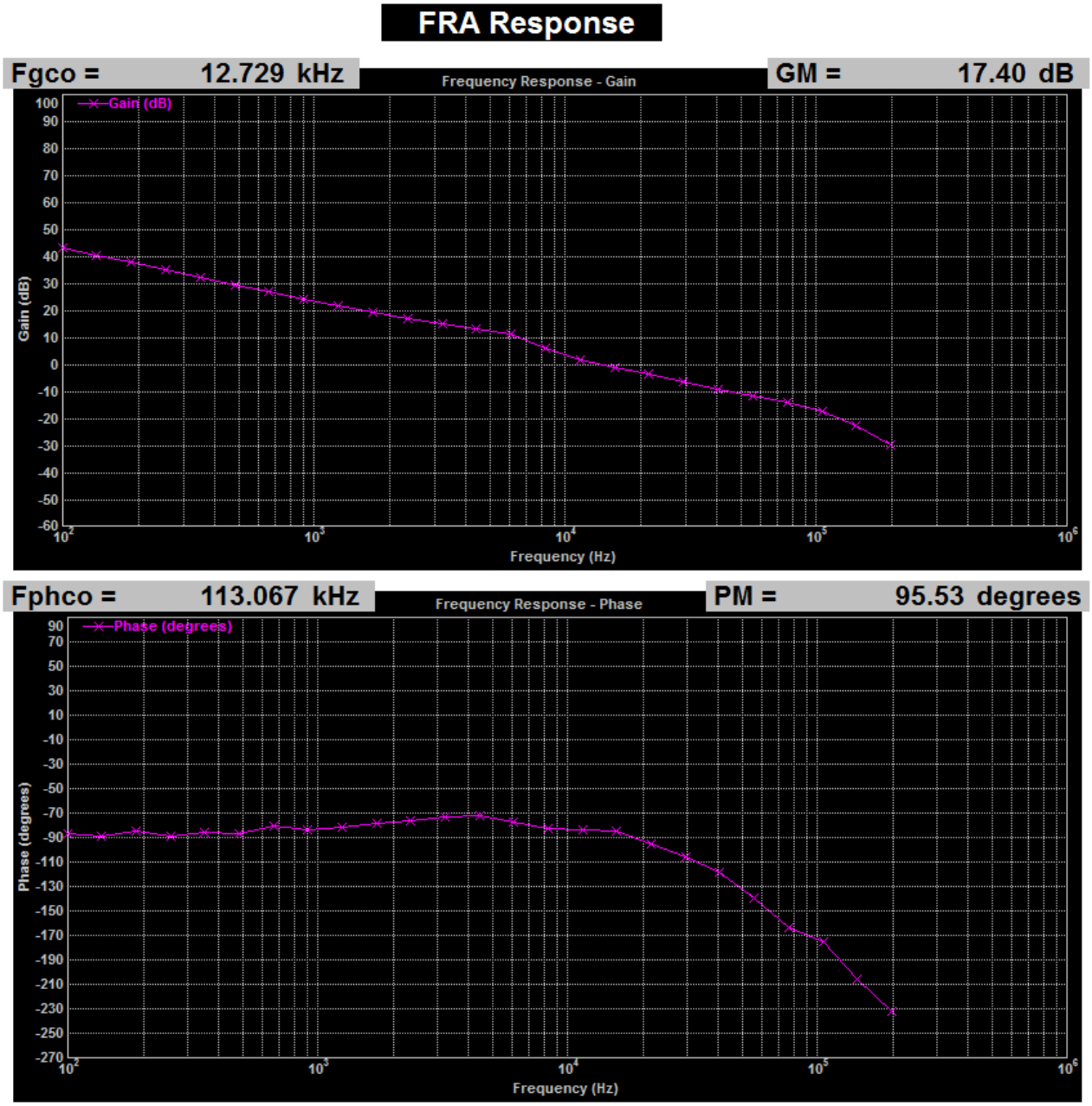
The FRA block accuracy is verified in the example: Examples > Tools > Frequency Response > FRA Calibration.



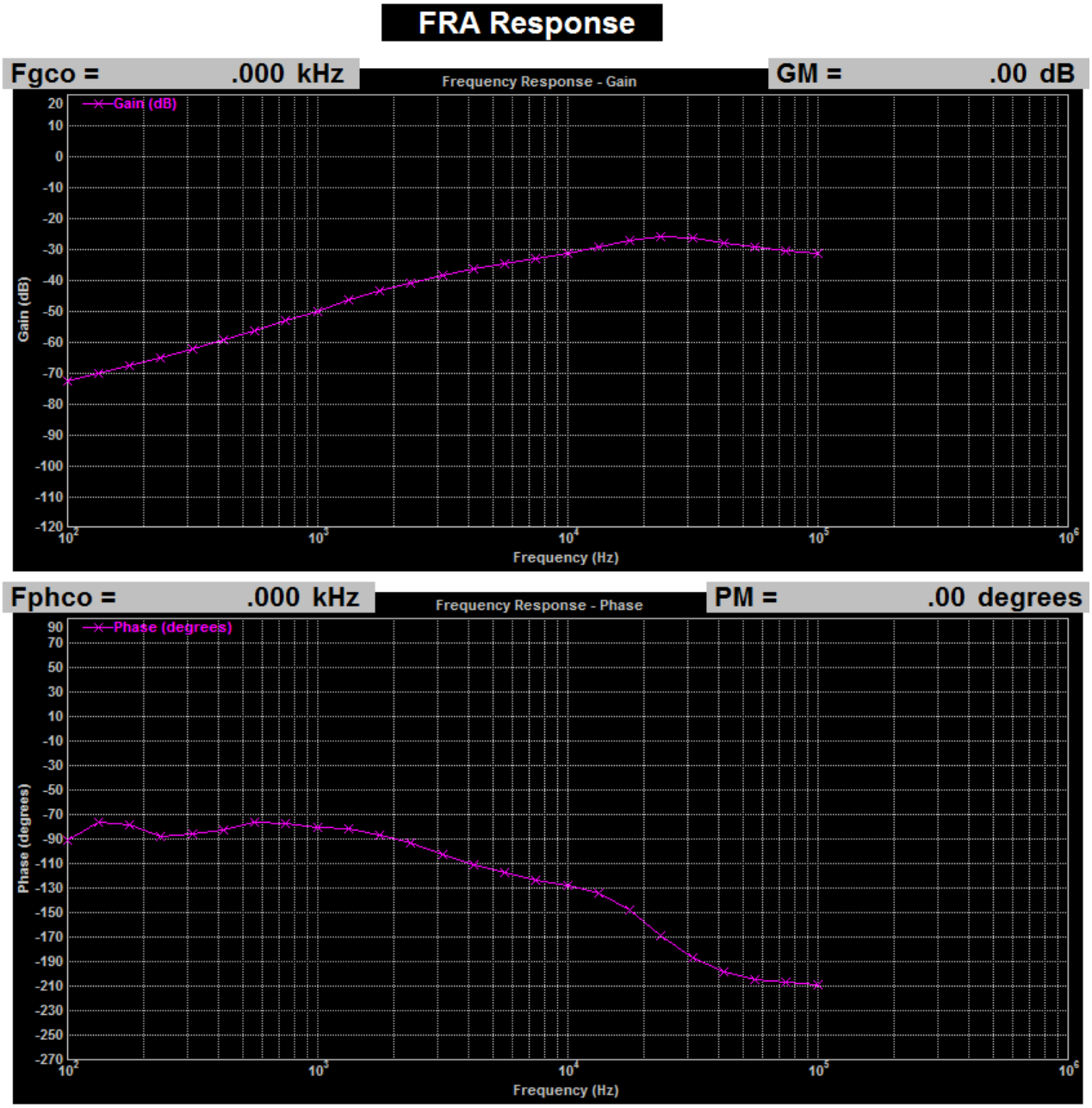
Even in the presence of high harmonics, switching waveforms and noise superimposed on the measured signal, the gain error is typically less than 0.05% while the phase error is typically less than 0.02%. The accuracy is also dependent upon a sufficiently small simulation time step. In the example above the simulation time step was set at 100ns.

Some typical frequency response results using the FRA are given in the following figures.

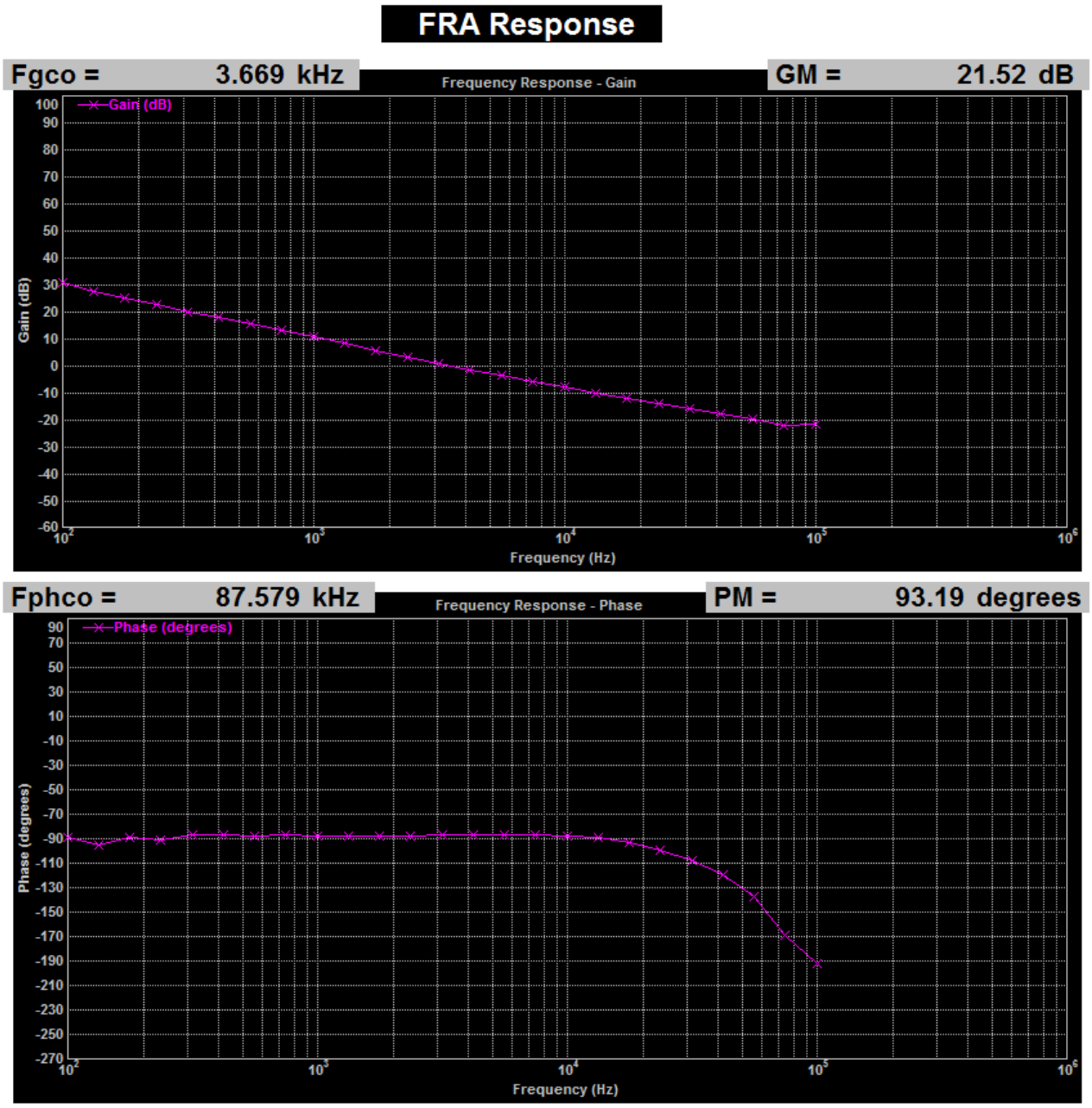
Measured buck converter (VMC) open-loop response:

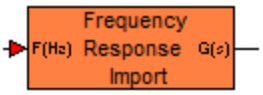


Measured buck converter output impedance:



Measured buck converter open-loop response under peak current mode control:





Frequency Response Import

The frequency import block allows one to use a frequency domain model tabled in a map file or imported into that file from another diagram such as a FRA sweep using the FRA block or from another application such as PSIM.

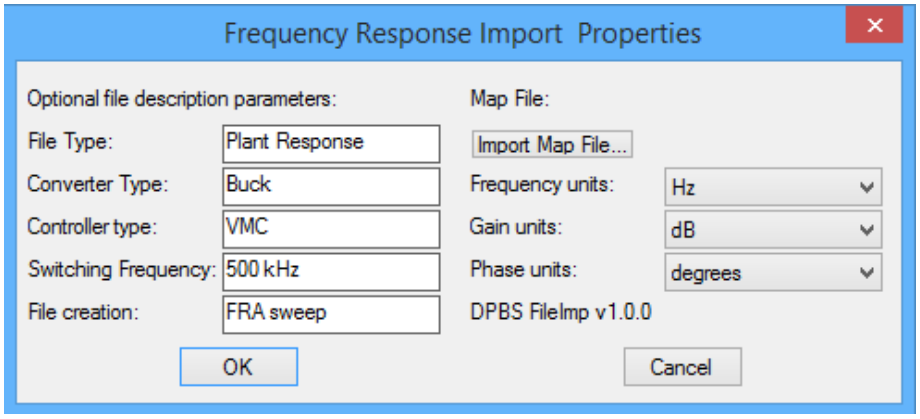
Note that the data file format is also directly compatible with the PSIM FRA data output file from AC sweeps performed in PSIM.

Input pin: **F(Hz)** The frequency for the current system response output.

Output pin: **G(s)** The measured transfer function response output at the current input frequency.

Dialog properties:

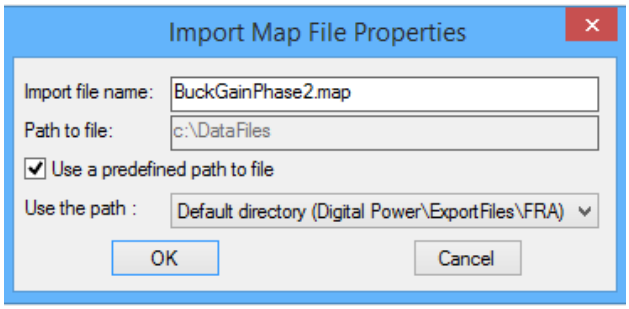
The frequency response import block properties menu is shown in the following figure which appears when right-clicking on the block.



File type, converter type etc:

The first inputs are optional text describing the contents of the data file.

Import Map File:



Import file name:

Select the file name.

Path to file:

Give the path to the file or otherwise select from a predetermined path.

Frequency units:

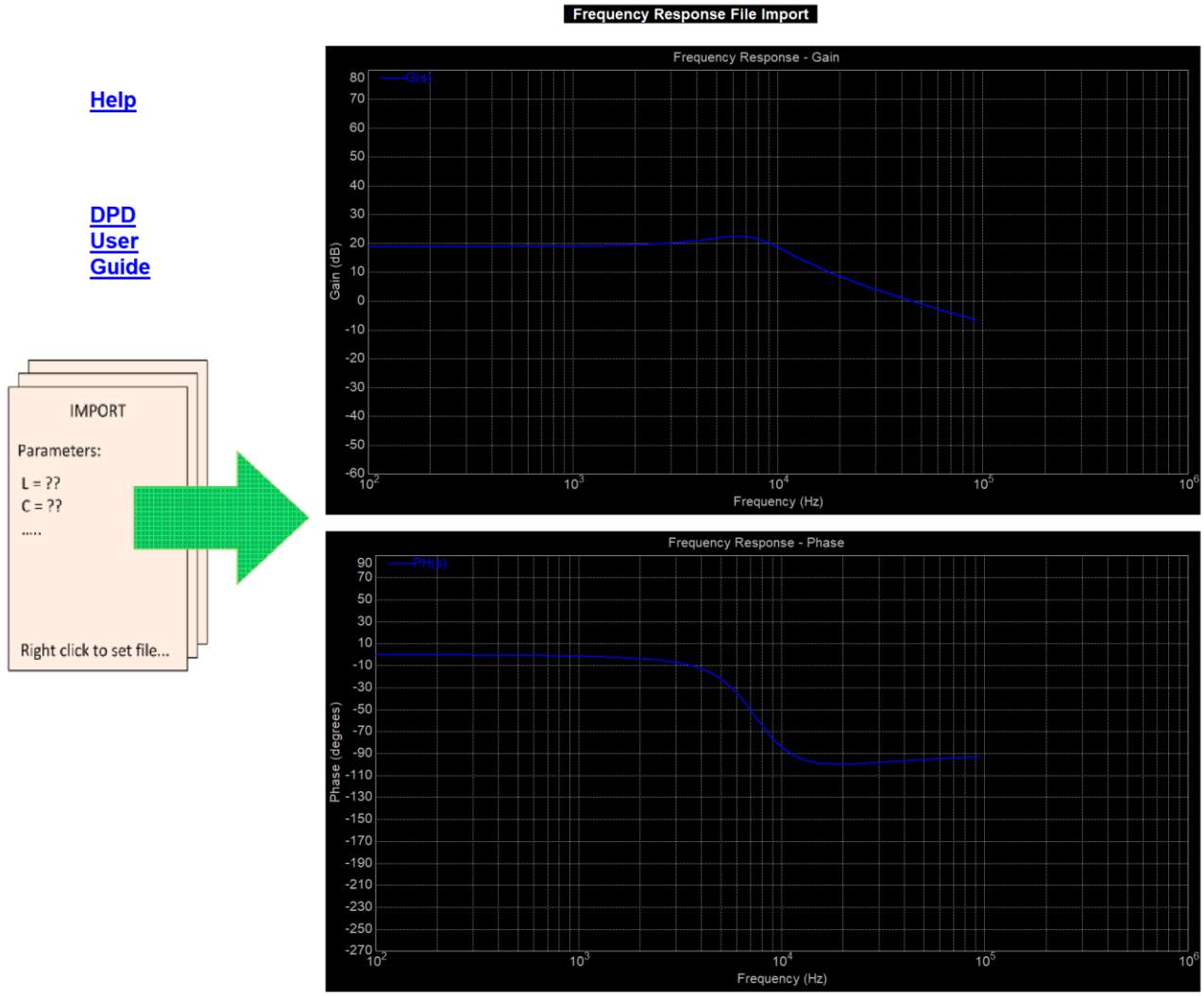
Choose the frequency units in which the imported data file was created (Hz or kHz).

Gain units:

Choose the gain units in which the imported data file was created (normal magnitude or dB).

Phase units:

Choose the phase units in which the imported data file was created (radians or degrees).
The frequency response of the imported file can be verified internally in the blocks as below:



Chapter 6 - Debug

Chapter 6 - Debug 1

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Main Contents

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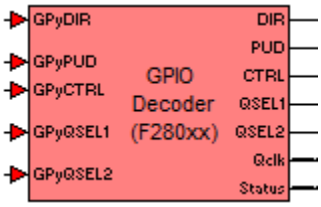
The debug section of the digital power designer block set consists of a series of blocks which can used in debugging peripheral support on TI C2000 MCUs.

Sub-sections within this section contain blocks which are code-generable in order to be included in diagrams to be downloaded to a MCU. Support blocks can then be included in debugging diagrams, usually together with a target-interface diagram, to view the configured properties of peripherals and/or the status of C2000 registers.

Peripheral parameters can also be viewed in real-time in a HIL diagram in an understandable format rather than having to decode registers.

Target Diagram Decoders

The target diagram decoders are blocks intended to be used in HIL debugging diagrams together with a compiled target interface block. The blocks will function in target interface diagrams together with the compiled diagram running on the MCU. In general, the various register values can be outputted from the target interface block at pins and connected to the appropriate target diagram decoder. Alternatively, register values can be fed into monitor buffers and the registers can be then monitored at the full target interface diagram sample rate.



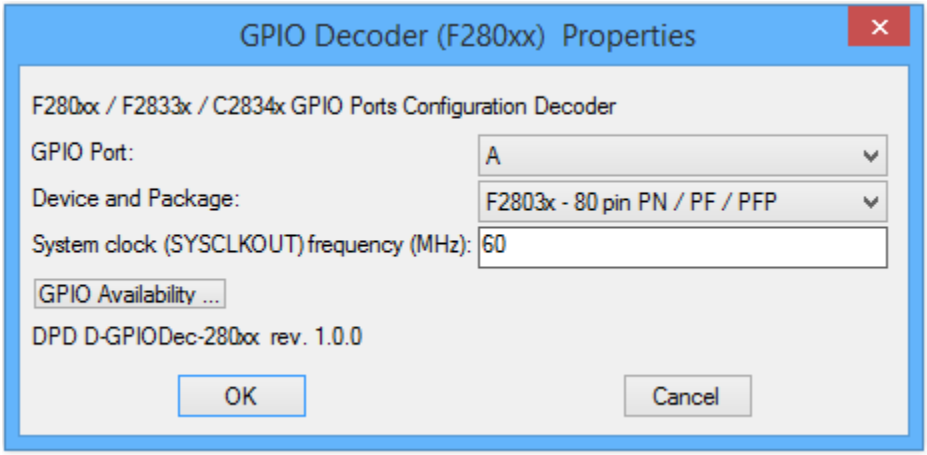
GPIO Decoder

The GPIO decoder block accepts at the input the C2000 GPIO configuration registers. It can be used in target interface diagrams in order to check and debug the GPIO configuration for the selected port.

Input pins:	**GPyDIR**	The input C2000 GPIO direction register from a target interface block.
	GPyPUD	The input C2000 GPIO pull-up disable register from a target interface block
	GPyCTRL	The input C2000 GPIO control register from a target interface block
	GPyQSEL1,2	The input C2000 GPIO Qualification select register from a target interface block.
Output pins:	**DIR**	The GPIO direction register output.
	PUD	The GPIO pull-up disable register output.
	CTRL	The GPIO control register output.
	QSEL1,2	The GPIO qualification select registers outputs.
	Qclk	A struct output displaying the current qualification clock division factors.
	Status	A struct output displaying the current GPIO configuration for the selected port.

Dialog properties:

The GPIO decoder block properties menu is shown in the following box which appears when right-clicking on the block.



GPIO port:

Select the desired GPIO port.

Device and Package:

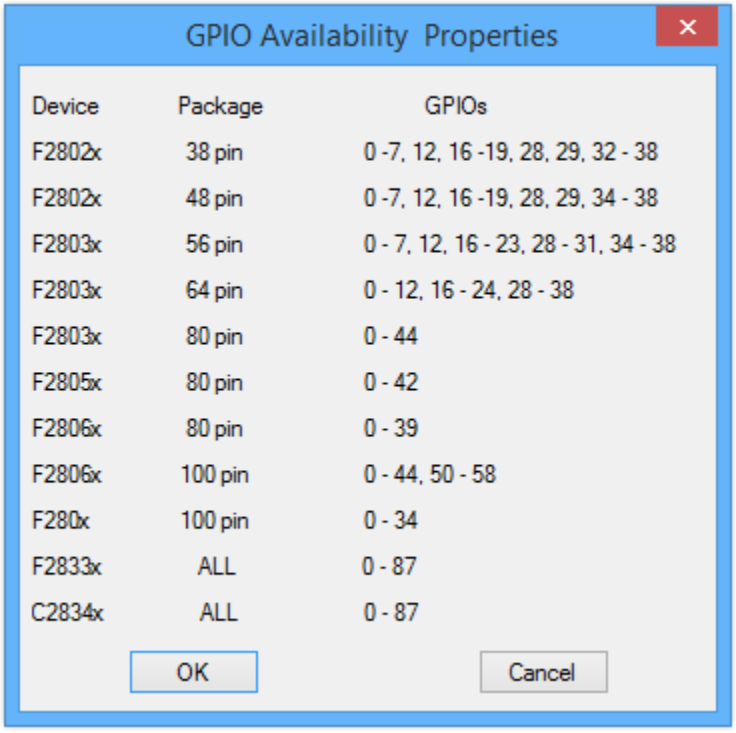
Select the desired C2000 device and package.

System clock frequency (SYSCLKOUT):

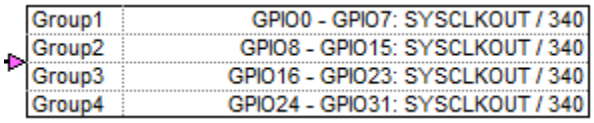
Enter the system clock frequency, SYSCLKOUT in MHz.

GPIO Availability:

The device and package-dependent availability of the various GPIO ports can be inspected in this dialog.



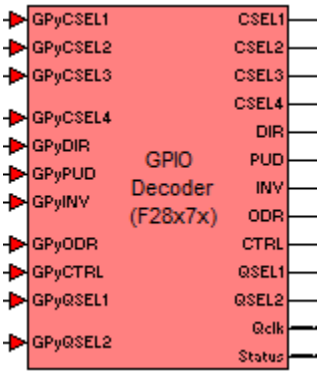
Typical Qclk output:



Typical status output:

Port	Configuration
0	GPIO0: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
1	GPIO1: Output, no Pull-up
2	GPIO2: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
3	GPIO3: Output, no Pull-up
4	GPIO4: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
5	GPIO5: Output, no Pull-up
6	GPIO6: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
7	GPIO7: Output, no Pull-up
8	GPIO8: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
9	GPIO9: Output, no Pull-up
10	GPIO10: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
11	GPIO11: Output, no Pull-up
12	GPIO12: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
13	GPIO13: Output, no Pull-up
14	GPIO14: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
15	GPIO15: Output, no Pull-up
16	GPIO16: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
17	GPIO17: Output, no Pull-up
18	GPIO18: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
19	GPIO19: Output, no Pull-up
20	GPIO20: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
21	GPIO21: Output, no Pull-up
22	GPIO22: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
23	GPIO23: Output, no Pull-up
24	GPIO24: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
25	GPIO25: Output, no Pull-up
26	GPIO26: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
27	GPIO27: Output, no Pull-up
28	GPIO28: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
29	GPIO29: Output, no Pull-up
30	GPIO30: Input, Pull-up, Qual: 3 samples, Delay = 17000 (ns)
31	GPIO31: Output, no Pull-up

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GPIO Decoder (F28x7x)

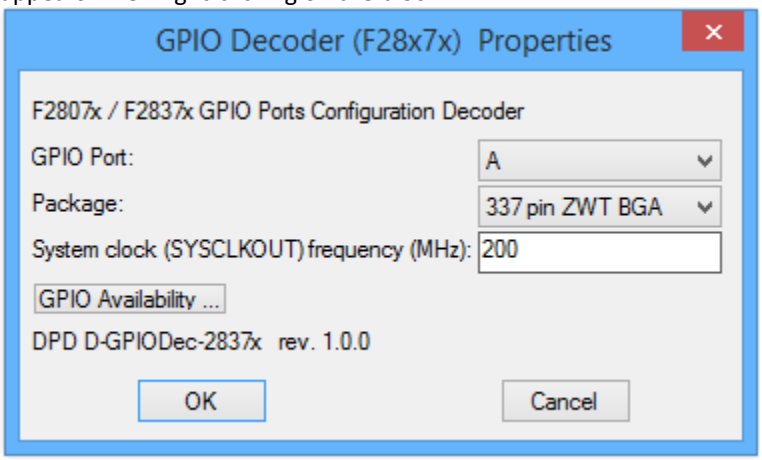
The GPIO decoder for the F2837x and piccolo F2807x is similar to the GPIO decoder above except that it covers the much more expanded configuration possibilities of the GPIO ports in these devices.

Input pins:	**GPyCSEL1..4**	The input C2000 GPIO core select registers inputs from a target interface block.
	GPyDIR	The input C2000 GPIO direction register from a target interface block.
	GPyPUD	The input C2000 GPIO pull-up disable register from a target interface block

	GPyINV	The input C2000 GPIO input invert register input.
	GPyODR	The input C2000 GPIO core open drain enable register input.
	GPyCTRL	The input C2000 GPIO control register from a target interface block.
	GPyQSEL1,2	The input C2000 GPIO qualification select register input.
Output pins:	**CSEL1..4**	The core select register output.
	DIR	The direction register output.
	PUD	The pull-up disable register output.
	INV	The input invert register output.
	ODR	The open drain enable register output.
	CTRL	The GPIO control register output.
	QSEL1,2	The qualification select register outputs.
	Qclk	A struct output displaying the current qualification clock division factors.
	Status	A struct output displaying the current GPIO configuration for the selected port.

Dialog properties:

The GPIO decoder block properties menu is shown in the following box which appears when right-clicking on the block.



GPIO port:

Select the desired GPIO port from A to F.

Package:

Enter the package type used.

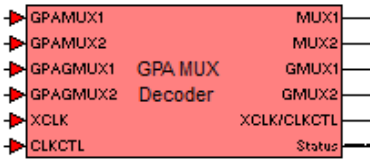
System clock frequency (SYSCLKOUT):

Enter the system clock frequency, SYSCLKOUT (MHz).

GPIO Availability:

The device and package-dependent availability of the various GPIO ports can be inspected in this this dialog.

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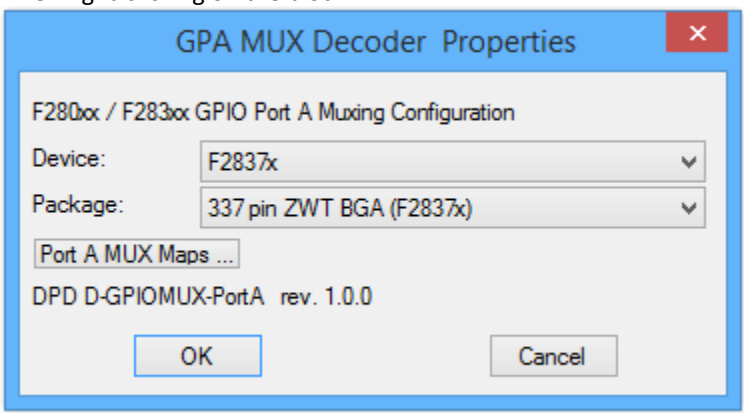
GPA Mux

The GPA Mux target interface decoder decodes the MUX configuration as currently set-up on the MCU and as reported by a target interface block.

Input pins:	**GPAMUX1**	The GPAMUX1 register input.
	GPAMUX2	The GPAMUX2 register input.
	GPAGMUX1	The GPAGMUX1 group register input (only F28x7x)
	GPAGMUX2	The GPAGMUX2 group register input (only F28x7x).
	XCLK	XCLK register input.
	CLKCTL	CLKCTL register input.
Output pins:	**MUX1,2**	GPAMUX1 and 2 registers outputs.
	GMUX1,2	GPAGMUX1 and 2 registers outputs (F28x7x only).
	XCLK/CLKCTL	The XCLK and CLKCTL registers combined at the output.
	Status	A struct output displaying the current GPIO MUX configuration for the selected port.

Dialog properties:

The GPA MUX block properties menu is shown in the following box which appears when right-clicking on the block.



Device:

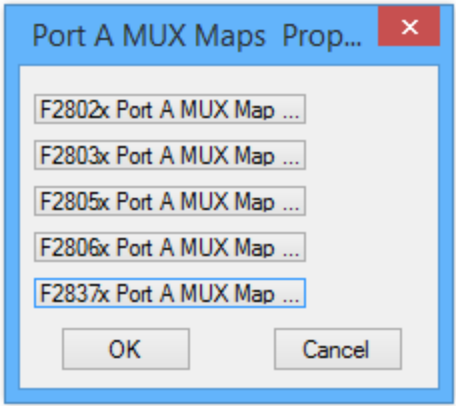
Select the C2000 device.

Package:

Select the package type.

Port A MUX Maps:

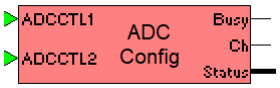
The device and package-dependent available MUXing of the various GPIO ports can be inspected in this this dialog.



Typical status output:

GPIO0	Reserved, pin C8
GPIO1	Reserved, pin D8
GPIO2	OUTPUTXBAR1, (O), pin A7
GPIO3	OUTPUTXBAR2, (O), pin B7
GPIO4	OUTPUTXBAR3, (O), pin C7
GPIO5	Reserved, pin D7
GPIO6	EQEP3A, (I), pin A6
GPIO7	EQEP3B, (I), pin B6
GPIO8	EQEP3S, (I/O), pin G2
GPIO9	EQEP3I, (I/O), pin G3
GPIO10	EQEP1A, (I), pin B2
GPIO11	EQEP1B, (I), pin C1
GPIO12	EQEP1S, (I/O), pin C2
GPIO13	EQEP1I, (I/O), pin D1
GPIO14	Reserved, pin D2
GPIO15	Reserved, pin D3
GPIO16	ePWM9A, (O), pin E1
GPIO17	ePWM9B, (O), pin E2
GPIO18	ePWM10A, (O), pin E3
GPIO19	ePWM10B, (O), pin E4
GPIO20	ePWM11A, (O), pin F2
GPIO21	ePWM11B, (O), pin F3
GPIO22	ePWM12A, (O), pin J4
GPIO23	ePWM12B, (O), pin K4
GPIO24	Reserved, pin K3
GPIO25	Reserved, pin K2
GPIO26	OUTPUTXBAR3, (O), pin K1
GPIO27	OUTPUTXBAR4, (O), pin L1
GPIO28	OUTPUTXBAR5, (O), pin V11
GPIO29	OUTPUTXBAR6, (O), pin W11
GPIO30	OUTPUTXBAR7, (O), pin T11
GPIO31	OUTPUTXBAR8, (O), pin U11

Contents - Debug



ADC Config

The ADC Config decoder decodes the registers for the ADC (Type 3) configuration.

Input pins: **ADCCTL1** The ADC configuration 1 register input.

ADCCTL2 The ADC configuration 2 register input.

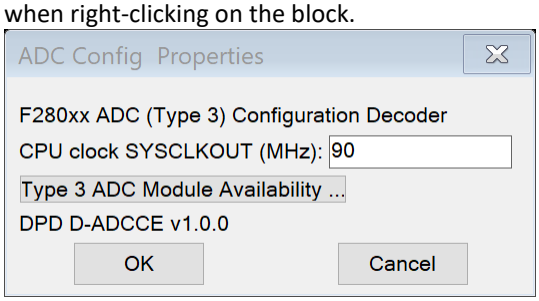
Output pins: **Busy** Indicates when the ADC is busy converting.

Ch Indicates the current channel converting or the last channel converted.

Status A struct output giving the current status of the ADC configuration when running together with a target-interface diagram.

Dialog properties:

The ADC Config block properties menu is shown in the following box which appears when right-clicking on the block.



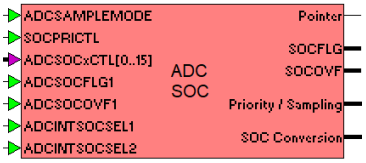
CPU clock SYSCLKOUT:

Enter the CPU clock frequency in MHz.

Typical status output:

ADC	ADC module enabled
ADC Power	ADC powered on
Bandgap Circuit	Bandgap circuitry enabled
Reference buffers	Reference buffers enabled
ADC Clock	45 MHz
Temperature sensor	Temp. sensor conversion (ADCINA5 not connected).
VREFLO conversion	ADCINB5 input is connected
Interrupt Pulse	Interrupt pulse at Result latched (EOC).
ADC Reference	Internal Bandgap reference used
Overlap	Sample and Conversion Overlap Enabled

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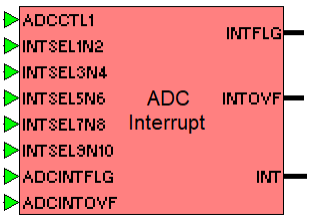


ADC SOC

The ADC SOC decoder decodes the registers for the ADC (Type 3) start-of -conversion or SOC.

Input pins: **ADCSAMPLEMODE** The ADC sample mode register input.

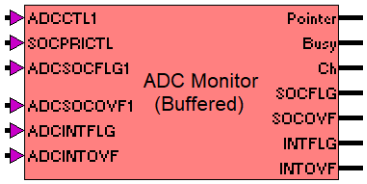
	SOCPRICTL	The ADC SOC priority control register input.
	ADCSOCx[0..15]	The ADC SOC registers input vector up to 16 elements.
	ADCSOCFLG1	The ADC SOC Flag register input.
	ADCSOCOVF1	The ADC SOC Overflow register input.
	ADCINTSOCSEL1	The ADC SOC Interrupt Select 1 register input.
	ADCINTSOCSEL2	The ADC SOC Interrupt Select 2 register input.
Output pins:	**Pointer**	Indicates the current SOC pointer position.
	SOCFLG	Indicates which SOC is currently being serviced.
	SOCOVF	Indicates if a SOC could not be serviced.
	Priority/Sampling	Indicates the SOC priority and type of sampling.
	SOC Conversion	A struct output with the current SOC conversion configuration.



ADC Interrupt

The ADC Interrupt decoder decodes the registers for the ADC (Type 3) interrupt configuration.

Input pins:	**ADCCTL1**	The ADC configuration 1 register input.
	INTSEL1N2	The ADC interrupt select register input for interrupts 1 and 2.
	INTSEL3N4	The ADC interrupt select register input for interrupts 3 and 4.
	INTSEL5N6	The ADC interrupt select register input for interrupts 5 and 6.
	INTSEL7N8	The ADC interrupt select register input for interrupts 7 and 8.
	INTSEL9N10	The ADC interrupt select register input for interrupt 9.
	ADCINTFLG	The ADC interrupt flag register input.
	ADCINTOVF	The ADC interrupt overflow flag register.
Output pins:	**INTFLG**	Indicates which interrupt is currently active.
	INTOVF	Indicates if an overflow has occurred and an interrupt is not serviced.
	INT	A struct output with the full ADC interrupt configuration.



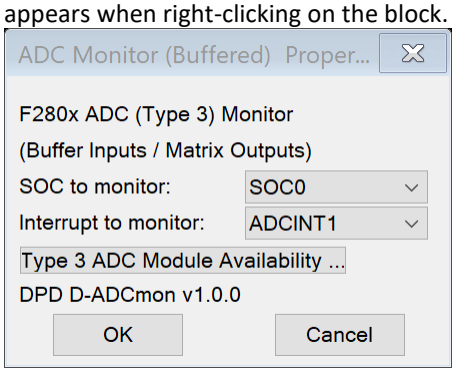
ADC Monitor (Buffered)

The ADC Config decoder decodes the registers for the ADC (Type 3) configuration. This decoder has buffered inputs to view the data in real-time using monitor buffers in the target interface diagram.

Input pins:	**ADCCTL1**	The ADC configuration 1 register input.
	SOCPRICTL	The ADC SOC priority control register input.
	ADCSOCFLG1	The ADC SOC flag register input
	ADCSOCOVF1	The ADC SOC overflow register input
	ADCINTFLG	The ADC interrupt flag register input
	ADCINTOVF	The ADC interrupt overflow register input
Output pins:	**Pointer**	Indicates the current SOC pointer position.
	Busy	Indicates when the ADC is busy converting.
	Ch	Indicates the current channel converting or the last channel converted.
	SOCFLG	Indicates when the SOC is currently being serviced.
	SOCOVF	Indicates if the SOC could not be serviced.
	INTFLG	Indicates when the specified interrupt is currently active.
	INTOVF	Indicates if an overflow has occurred and the interrupt is not serviced.

Dialog properties:

The ADC monitor block properties menu is shown in the following box which appears when right-clicking on the block.



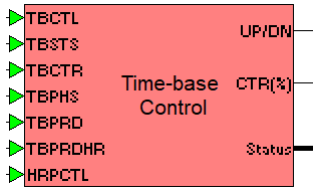
SOC to monitor:

Select the desired SOC to be monitored.

Interrupt to monitor:

Select the desired ADC interrupt to be monitored.

Contents - Debug



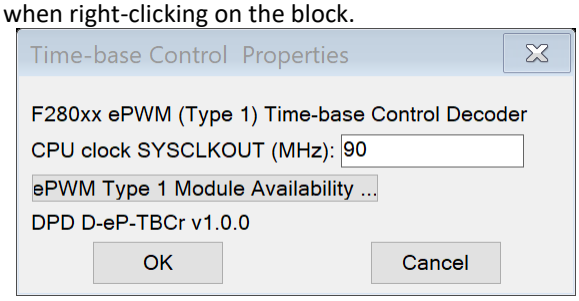
ePWM Time-base Control Decoder

The ePWM time-base submodule decoder decodes the registers allocated to the PWM time base configuration.

Input pins:	**TBCTL**	The time-base submodule control register input.
	TBSTS	The time-base submodule status register input.
	TBCTR	The time-base submodule counter register input.
	TBPHS	The time-base submodule phase value register input.
	TBPRD	The time-base submodule period value register input.
	HRPCTL	The high-resolution control register input.
Output pins:	**UP/DN**	Gives the current direction of the counter (UP = 1; DN = 0).
	CTR(%)	The current counter value in % of the period (can only be captured using slow counter rates or on an interrupt or emulation freeze).
	Status	A struct output giving the current status of the time-base submodule when running together with a target-interface diagram.

Dialog properties:

The Time-base Submodule block properties menu is shown in the following box which appears when right-clicking on the block.

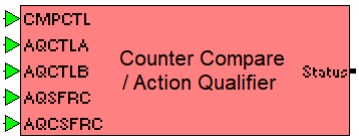


PWM clock frequency:

Enter the CPU frequency or SYSCLKOUT frequency.

Typical status output:

	ePWM Time-base Counter Configuration
PWM frequency	45 kHz
Phase	119.88 degrees
Phase direction	Always DOWN count.
Counter direction	Currently counting UP
Sync Event	No Sync event has occurred.
Counter overflow	Counter has reached Max. value
Counter mode	DOWN count mode.
Phase Sync	Load the phase value TBPHS on a sync signal.
Sync Out Source	EPWMxSYNC
High Resolution	High resolution NOT enabled.
HR Sync	High resolution synchronisation NOT enabled.
HR period	0 kHz
PWM resolution	0.05 %, 10.9658 bits
Emulation	Free run.



ePWM Counter-compare Action-qualifier Decoder

The counter-compare / action qualifier submodules decoder decodes the registers allocated to these sub-modules.

Input pins:	**CMPCTL**	The counter compare control register input.
	AQCTLA	Action qualifier control A register input
	AQCTLB	Action qualifier control B register input
	AQSFRC	Action qualifier software force register input
	AQCSFRC	Action qualifier software force register input
Output pins:	**Status**	A struct output giving the current status of the counter-compare / action-qualifier submodules when running together with a target-interface diagram.

Typical status output:

	ePWM Counter Compare / Action Qualifier Configuration
Load mode	Freeze CMPA loads, Load CMPB on CTR = 0 OR PRD.
Shadow mode	Shadow mode on CMPA, Immediate mode on CMPB.
Shadow Buffer	Shadow FIFO on CMPA not Full, Shadow FIFO on CMPB Full.
CTR = 0 Action	Toggle: EPWMxA = not[z^-1(EPWMxA)], Clear: EPWMxB = 0.
CTR = PRD Action	Set: EPWMxA = 1, No action on EPWMxB.
CTR = CMPA, CTR dec. Action	No action on EPWMxA, No action on EPWMxB.
CTR = CMPA, CTR inc. Action	Toggle: EPWMxA = not[z^-1(EPWMxA)], Set: EPWMxB = 1.
CTR = CMPB, CTR dec. Action	Set: EPWMxA = 1, Toggle: EPWMxB = not[z^-1(EPWMxB)].
CTR = CMPB, CTR inc. Action	No action on EPWMxA, Set: EPWMxB = 1.
One-time Software Forcing	No action on EPWMxA, No action on EPWMxB.
Continuous Software Forcing	Disabled on EPWMxA, Disabled on EPWMxB, Load on CTR = 0.



ePWM Event Trigger Decoder

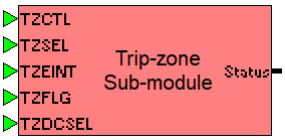
The event trigger submodule decoder decodes the registers allocated to the this sub-module configuration.

Input pins:	**ETSEL**	The event-trigger submodule select register input.
	ETPS	The event-trigger submodule select register input.
	ETFLG	The event-trigger submodule flag register input.
Output pins:	**SOCA**	Indicates that an SOCA event was generated.
	SOCB	Indicates that an SOCB event was generated.
	INT	Indicates that an interrupt event was generated.
	SOCACNT	Number of SOCA triggers that have occurred.
	SOCBCNT	Number of SOCB triggers that have occurred.
	INTCNT	Number of interrupts that have occurred.

Status A struct output giving the current status of the event trigger submodule when running together with a target-interface diagram.

Typical status output:

	ePWM Event Trigger Configuration
SOCA Config	SOCA Pulse Disabled.
SOCB Config	SOCB Pulse Disabled.
INT Config	EPWM Interrupt Enabled, on TBCTR = PRD, on the first event.



ePWM Trip-zone Decoder

The trip zone submodule decoder decodes the register allocated to this sub-module configuration.

Input pins:

TZCTL The trip-zone submodule control register input.

TZSEL The trip-zone submodule select register input.

TZEINT The trip-zone submodule interrupt enable register input.

TZFLG The trip-zone submodule flag register input.

TZDCSEL The trip-zone / digital compare submodule digital compare select register input.

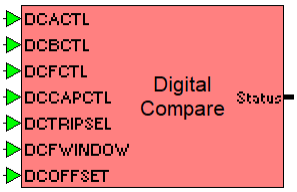
Output pins:

Status A struct output giving the current status of the trip-zone submodule when running together with a target-interface diagram.

Typical status output:

	ePWM Trip-zone Configuration
Trip-zone Action	EPWMxA = No action, EPWMxB = 1.
DCAEVT1 Action	EPWMxA = 0.
DCAEVT2 Action	EPWMxA = 0.
DCBEVT1 Action	EPWMxB = 0.
DCBEVT2 Action	EPWMxB = HZ.
Enabled CBC Trip-zones	TZ1/, TZ2/, TZ3/, TZ6/, DCBEVT2.
Enabled One-shot Trip-zones	TZ2/, DCBEVT1.
Digital Compare DCAEVT1 Action	DCAH = Don't Care, DCAL = 1.
Digital Compare DCAEVT2 Action	Reserved - no action.
Digital Compare DCBEVT1 Action	Event disabled.
Digital Compare DCBEVT2 Action	DCBH = 0, DCBL = Don't Care.
Enabled Events on TZ Interrupt	DCBEVT1,
TZ Flag Events Generated.	DCBEVT1,
TZ Interrupt	TZINT has been generated.

Contents - Debug



ePWM Digital Compare Decoder

The ePWM digital compare submodule decoder decodes the register allocated to the chopper sub-module configuration.

Input pins:

DCACTL The digital compare submodule control A register input.

DCBCTL The digital compare submodule control B register input.

DCFCTL The digital compare submodule filter control register input.

DCCAPCTL The digital compare submodule capture register input.

DCTRIPSEL The digital compare submodule trip select register input.

DCFWINDOW The digital compare submodule filter (blanking) window configuration register input.

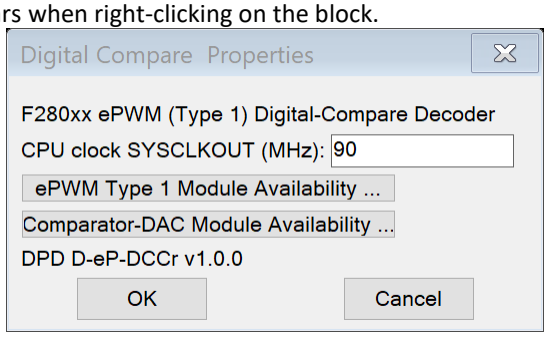
DCOFFSET The digital compare submodule blanking window offset register input.

Output pins:

Status A struct output giving the current status of the digital compare submodule when running together with a target-interface diagram.

Dialog properties:

The digital compare submodule block properties menu is shown in the following box which appears when right-clicking on the block.



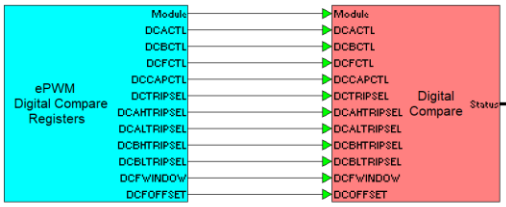
PWM clock frequency:

Enter the CPU clock frequency in MHz or SYSCLKOUT frequency.

Typical status output:

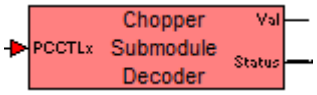
	ePWM (Type 1) Digital Compare Configuration
DCAEVT1 Source	Source is DCEVTFILT, Source is Asynchronous.
DCAEVT2 Source	Source is DCAEVT2, Source is Asynchronous.
DCBEVT1 Source	Source is DCEVTFILT, Source is Asynchronous.
DCBEVT2 Source	Source is DCBEVT2, Source is Asynchronous.
DCAEVT1 SOC/SYNC	SOC generation Enabled, Sync generation Disabled.
DCBEVT1 SOC/SYNC	SOC generation Enabled, Sync generation Disabled.
DCAH input source	TZ2/ input.
DCAL input source	TZ3/ input.
DCBH input source	TZ1/ input.
DCBL input source	TZ1/ input.
Filter Source	Source is DCAEVT2, Pulse-select Reserved position.
Blanking Window	Blanking window Disabled, Blanking window NOT Inverted.
Counter Capture	TBCTR capture Enabled, Shadow mode Enabled.
Blanking Window Length	0.366667 us.
Blanking window Offset	6.26667 us.

Typical application (Type 4/5 submodule):



	ePWM1. (Type 4) Digital Compare Submodule Configuration
DCAEVT1 Source	Source is DCAEVT1, Source is Synchronous.
DCAEVT2 Source	Source is DCAEVT2, Source is Synchronous.
DCBEVT1 Source	Source is DCBEVT1, Source is Synchronous.
DCBEVT2 Source	Source is DCBEVT2, Source is Synchronous.
DCAEVT1 SOC/SYNC	SOC generation Disabled, Sync generation Disabled.
DCBEVT1 SOC/SYNC	SOC generation Disabled, Sync generation Disabled.
DCAH input source	TZ1/ and TRIPIN1 input.
DCAL input source	TZ1/ and TRIPIN1 input.
DCBH input source	TZ1/ and TRIPIN1 input.
DCBL input source	TZ1/ and TRIPIN1 input.
Filter Source	Source is DCAEVT1, TBCTR = PRD.
Counter Capture	TBCTR capture Disabled, Shadow mode Enabled.
Blanking Window	Blanking window Disabled, Blanking window NOT Inverted.
Blanking Window Length	0. us.
Blanking window Offset	0. us.

In code-gen diagram **In target-interface diagram**



ePWM Chopper Submodule Decoder

The chopper submodule decoder decodes the register allocated to the chopper sub-module configuration.

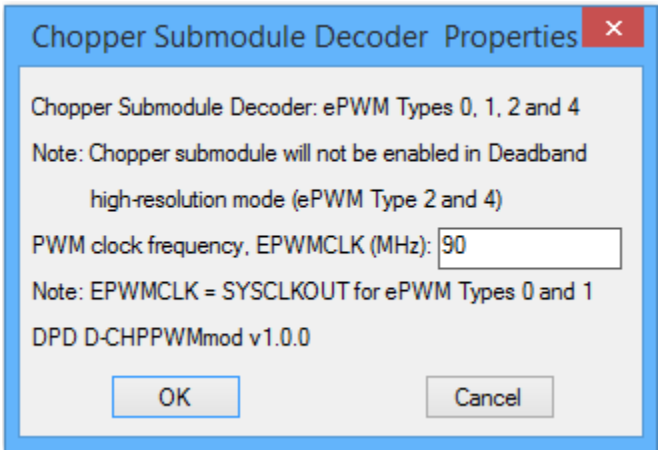
Input pins: **PCCTLx** The chopper submodule control register input.

Output pins: **Val** The current value output.

Status A struct output giving the current status of the chopper submodule when running together with a target-interface diagram.

Dialog properties:

The Chopper Submodule block properties menu is shown in the following box which appears when right-clicking on the block.



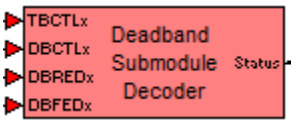
PWM clock frequency:

Enter the EPWMCLK frequency in MHz, which is usually the SYSCLKOUT frequency.

Typical status output:

Parameter	Configuration
CHPEN	Chopper submodule function enabled
OSHTWTH	First pulse = 533.333 (ns)
CHPFREQ	Chopper Frequency = 3.75 (MHz)
CHPDUTY	Duty cycle = 37.5 (%)

[Contents - Debug]



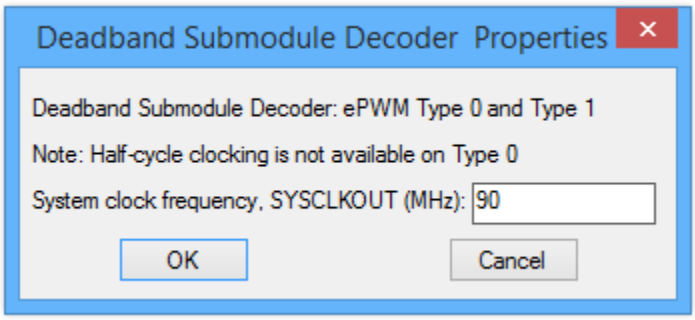
ePWM Deadband Submodule Decoder

The dead-band submodule target interface block is compatible with PWM types 0 and 1.

Input pins:	**TBCTLx**	The timer base control register input of the dead-band submodule.
	DBCTLx	The dead-band control register input of the dead-band submodule.
	DBEDx	The dead-band rising edge delay register input of the dead-band submodule.
	DBFEDx	The dead-band falling edge delay register input of the dead-band submodule.
Output pins:	**Status**	A struct output giving the current status of the dead-band submodule when running together with a target-interface diagram.

Dialog properties:

The Dead-band submodule properties menu is shown in the following box which appears when right-clicking on the block.

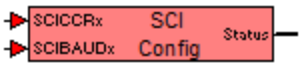


System clock frequency: Enter the system clock frequency (SYSCLKOUT) in MHz.

Typical status output:

Parameter	Configuration
OUT_MODE	Both RED and FED are enabled
POLSEL	Active High Complementary Mode - EPWMA is not inverted and EPWMB is inverted
IN_MODE	EPWMA is the source for RED, EPWMB is the source for FED
Clocking	Half-cycle clocking enabled
RED	1.42222 (us)
FED	622.222 (ns)
Resolution	11.1111 (ns)

Contents - Debug



SCI Config

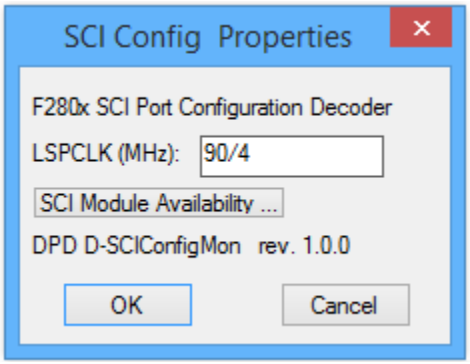
Input pins: **SCICCRx** The SCI configuration control register input.

SCIBAUDx The SCI Baud rate input register.

Output pins: **Status** A struct output giving the current status of the SCI submodule configuration when running together with a target-interface diagram.

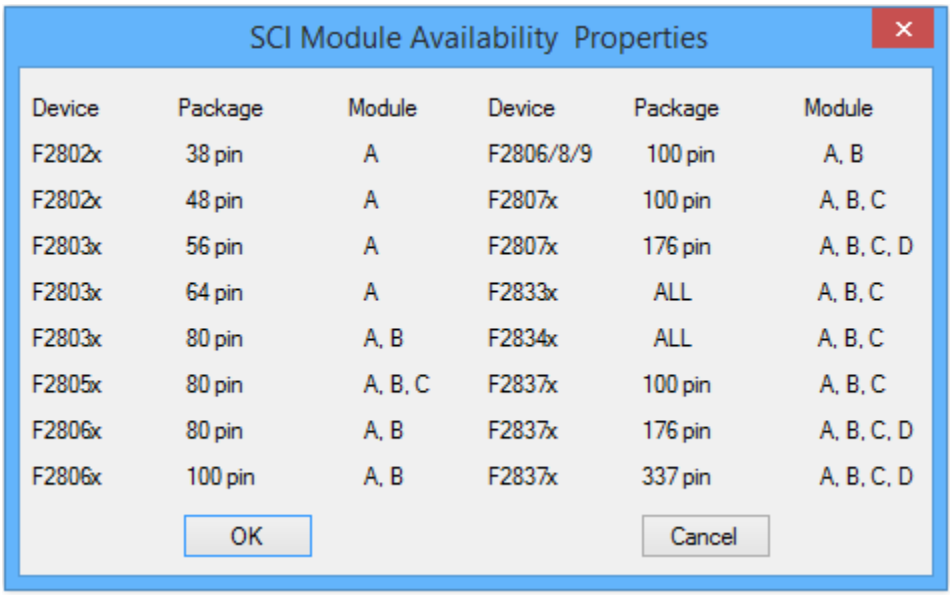
Dialog properties:

The SCI Config submodule properties menu is shown in the following box which appears when right-clicking on the block.



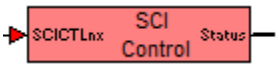
LSPCLK: Enter the low-speed clock frequency (LSPCLK) in MHz.

SCI Module Availability:



Typical status output:

Bit Length	1.0000
Mode	Idle mode
Loopback	Disabled
Parity Enabled	NO
Parity	Not Enabled
Stop bits	1
Baud Rate (kHz)	1406.2500



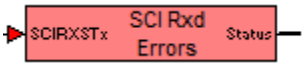
SCI Control

Input pins: **SCICTLx** The SCI control register input.

Output pins: **Status** A struct output giving the current status of the SCI submodule control when running together with a target-interface diagram.

Typical status output:

Receiver	Disabled
Transmitter	Disabled
Sleep Mode	Disabled
Tx Wakeup Method	Manual
SCI function	In Reset
Rx Error Interrupt	Disabled
Tx RDY Interrupt	Disabled
Rx RDY Interrupt	Disabled
TX Empty	Buffer not empty
TX Ready	Buffer Full



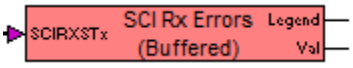
SCI Receive Errors

Input pins: **SCIRXSTx** The Receive status register input..

Output pins: **Status** A struct output giving the current status of the SCI submodule configuration when running together with a target-interface diagram.

Typical status output:

Wake	Sleep (if enabled)
Parity	OK
Overrun	No
Frame	No
Break Detect	No
Rx Ready	No char in buffer
Rx Error	No

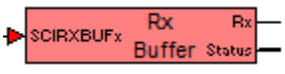


SCI Receive Errors (Buffered)

Input pins: **SCIRXSTx** The Receive status register input.

Output pins: **Legend** Descriptive output describing the buffered Val output columns

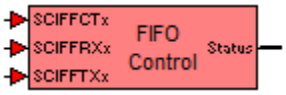
Val A buffer output giving the current status of the SCI submodule configuration when running together in a target-interface diagram.



SCI Rxd Buffer

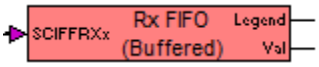
Input pins: **SCICCRx** The configuration control input register.

Output pins: **Status** A struct output giving the current status of the SCI submodule configuration when running together in a target-interface diagram.



SCI FIFO Control

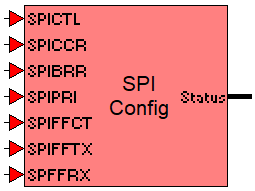
Input pins:	**SCIFFCTx**	The SCI FIFO control input register.
	SCIFFRXx	The SCI Rx FIFO register input.
	SCIFFTXx	The SCI Tx FIFO register input.
Output pins:	**Status**	A struct output giving the current status of the SCI submodule FIFO control when running together in a target-interface diagram.



SCI Receive FIFO (Buffered)

Input pins:	**SCIFFRXx**	The configuration control register input register.
Output pins:	**Legend**	Descriptive output describing the buffered Val output columns
	Val	A buffer output giving the current status of the SCI submodule configuration when running together in a target-interface diagram.

Contents - Debug



SPI Config

The SPI configuration decoder decodes the configuration and operation settings of the SPI communication peripheral.

Input pins:

SPICTL The SPI operation control register input.

SPICCR The SPI configuration control register input.

SPIBRR The SPI baud rate register input.

SPIPRI The SPI Priority Control register input.

SPIFFCT The SPI FIFO control register input.

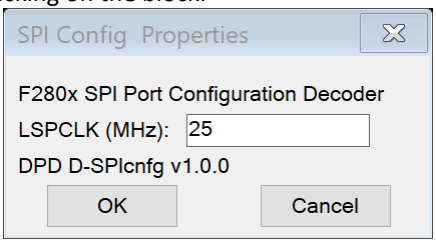
SPIFFTX The SPI Transmit FIFO configuration register input.

SPIFFRX The SPI Receive FIFO configuration register input.

Output pins: **Status** A struct output giving the current status of the SPI submodule configuration when running together with a target-interface diagram.

Dialog properties:

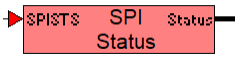
The SPI Config submodule properties menu is shown in the following box which appears when right-clicking on the block.



LSPCLK: Enter the low-speed clock frequency (LSPCLK) in MHz.

Typical status output:

Reset	In Software Reset.
Master/Slave	Master
SPI Interrupt	Disabled
Overrun Interrupt	Disabled
Talk	Enabled
Clock Polarity	Output on RE, input latched on FE
Clock Phase	Normal
High-speed mode (Type 2)	Disabled
Loopback Mode	Disabled
Word Length	16 bits.
Baud Rate	250 kHz
STE Invert	Not inverted (active low).
Wiring mode	Normal 4-wire mode.
FIFO	Disabled.
Transmit FIFO Interrupt	Not applicable.
Receive FIFO Interrupt	Not applicable.
Emulation mode	Free run mode.



SPI Status

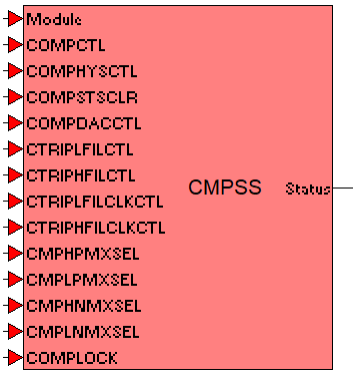
This decoder uses a buffered input of the SPI status register. The register should be buffered within a target interface diagram using a monitor buffer.

Input pins: **SPISTS** The SPI status register input (buffered).

Output pins: **Status** A struct output giving the current status of the SPI submodule when running together with a target-interface diagram.

Typical status output:

Overrun	No overrun
INT Flag	Active
Buffer Full	Not full

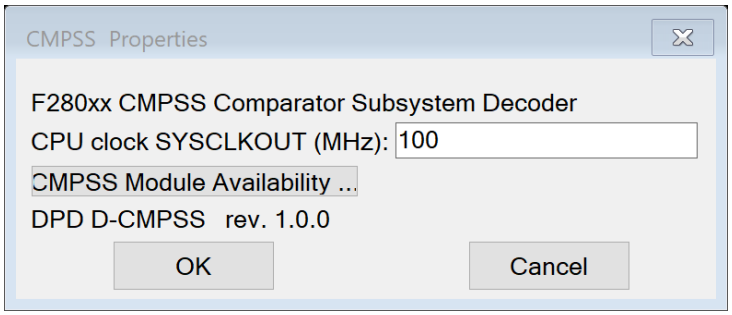


CMPSS module

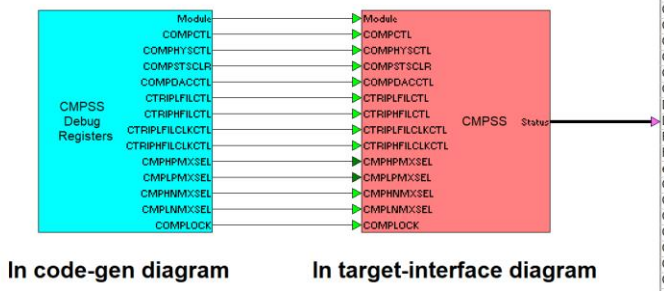
This block decodes the registers of the CMPSS module.

Input pins: **Registers** The CMPSS registers.

Output pin: **Status** A struct output giving the current status of the CMPSS submodule when running together with a target-interface diagram.



Typical application:



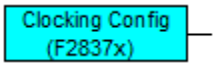
In code-gen diagram **In target-interface diagram**

	Comparator Subsystem Configuration for CMPSS1.
Enable	Comparator/DAC is DISABLED.
Comparators Hysteresis	No hysteresis on comparators.
CompH Negative Input Source	Inverting input driven by DACH and DACH source is DACHVALS.
CompH Positive Input Source	Non-inverting input external pin: A2/B6/PGA1_OF
CompH output invert	High comparator output is NOT inverted.
CompH Output OR	Asynchronous output NOT ORed with Filter output.
CTRIPH	Asynchronous comparator output.
CTRIPHOUT	Asynchronous comparator output.
CompH Filter Window	Filter sample window width = 1. samples = 1.e-002 us.
CompH Filter threshold	Min. number of required samples in sample window = 1..
CompH Latch Reset	EPWMSYNCO will NOT reset the High comparator Latch.
DAC Voltage Reference	VDDA is the voltage reference for the DACs.
DAC value Load	DAC value is updated on SYSCLK.
Ramp Load	Ramp value is loaded from RAMPMAXREFA.
Ramp generator sync source	Ramp generator sync source is EPWM1.SYNCO.
ePWM Blanking	EPWM blanking is DISABLED.
CompL Negative Input Source	Inverting input driven by DACL
CompL Positive Input Source	Non-inverting input external pin: A2/B6/PGA1_OF
CompL output invert	Low comparator output is NOT inverted.
CompL output OR	Asynchronous output NOT ORed with Filter output.
CTRIPL	Asynchronous comparator output.
CTRIPLOUT	Asynchronous comparator output.
CompL Filter Window	Filter sample window width = 1. samples = 1.e-002 us.
CompL Filter threshold	Min. number of required samples in sample window = 1..
CompL Latch Reset	EPWMSYNCO will NOT reset the Low comparator Latch.
Lock	No CMPSS registers are locked.

MCU (Codegen)

This section contains various blocks to be used in diagrams to be compiled and downloaded to the MCU. In general, the blocks are C2000 register lists which can be easily selected using the dialogs and those parameters outputted from target interface diagrams when compiling with the “Use selected compound edge pins for data exchange”.

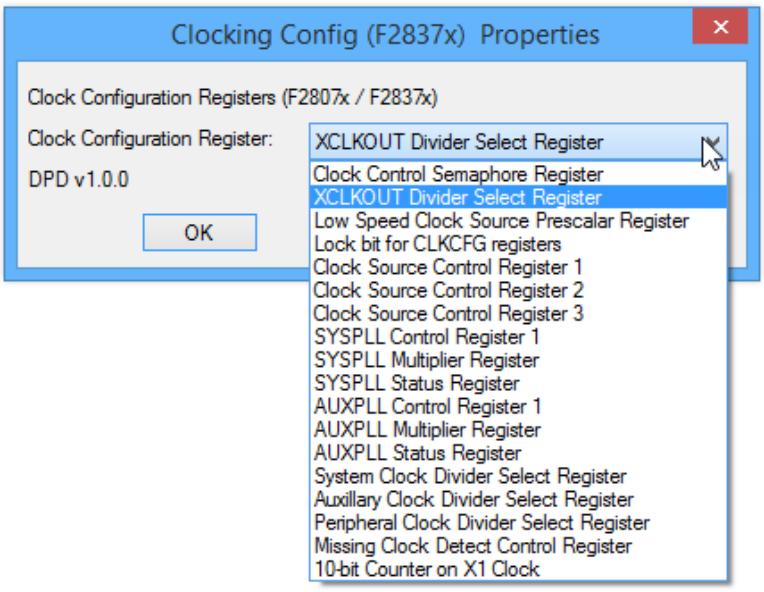
For further description on the C2000 registers, refer to the appropriate TI documentation.

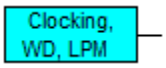


Clocking Config (F28x7x)

Clocking config register selection.

Output pin: Selected Register.

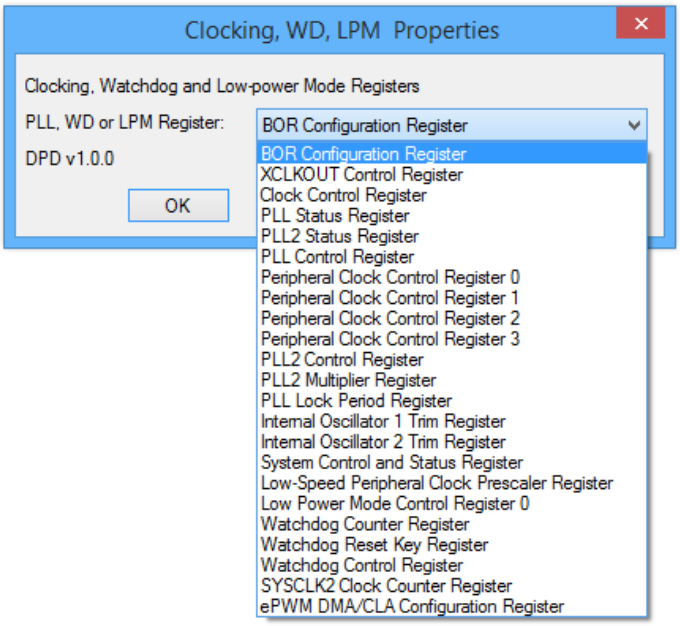


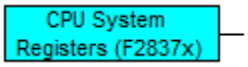


Clocking, WD, LPM

Clocking register selection.

Output pin: Selected Register.

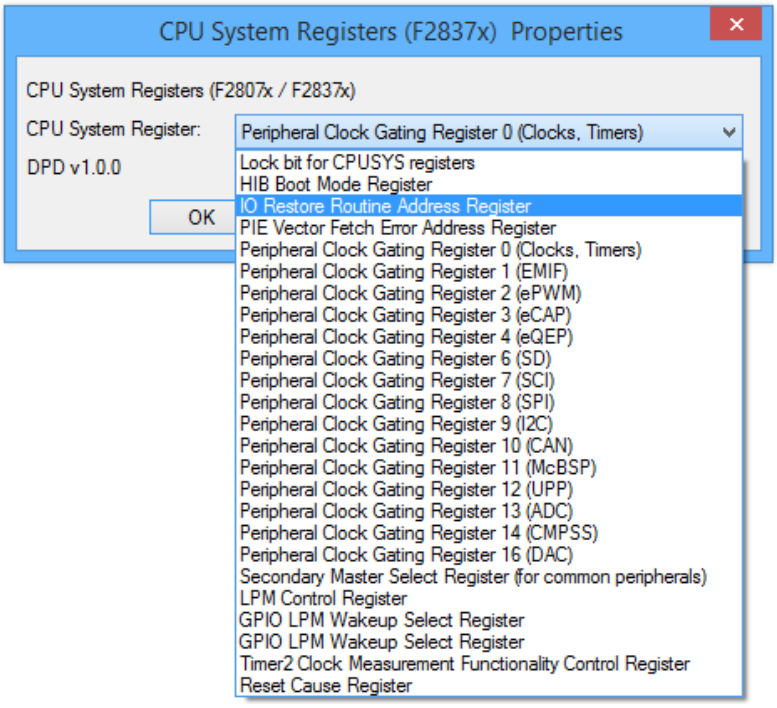


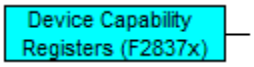


CPU System Registers

CPU system register selection.

Output pin: Selected Register.

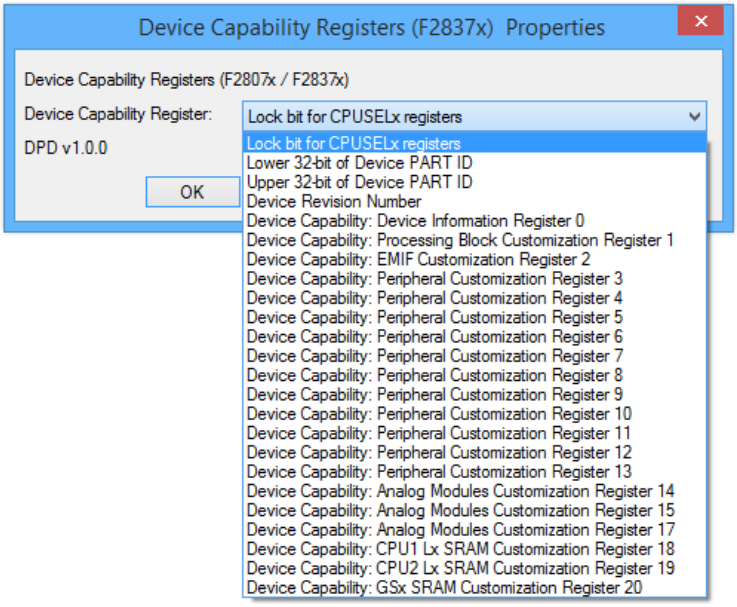


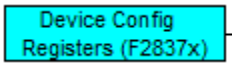


Device Capability Registers

Device capability register selection.

Output pin: Selected Register.

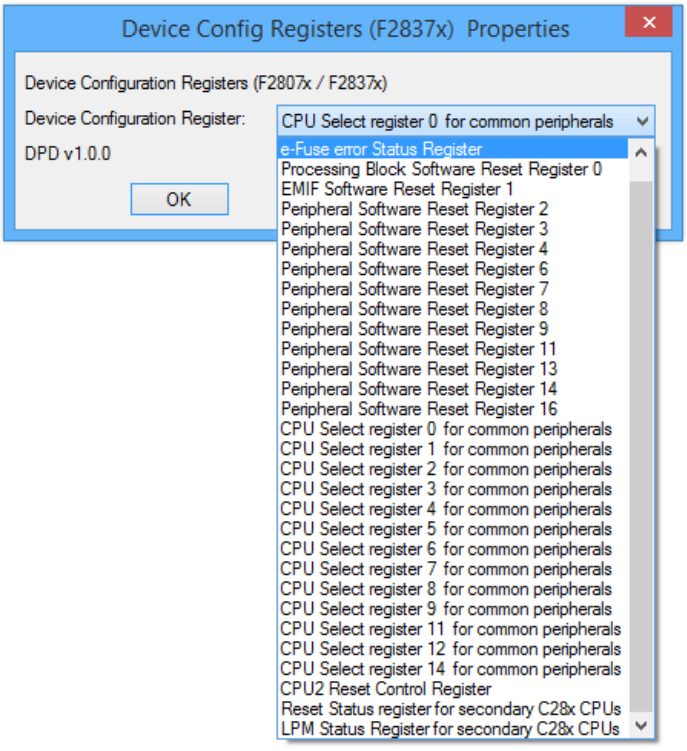




Device Config Registers

Device config register selection.

Output pin: Selected Register.

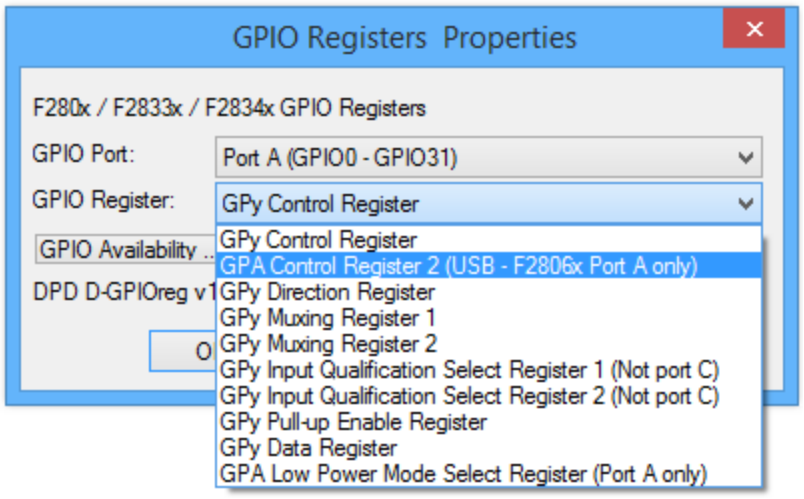


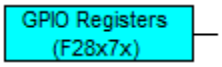


GPIO Registers

GPIO register selection.

Output pin: Selected Register.

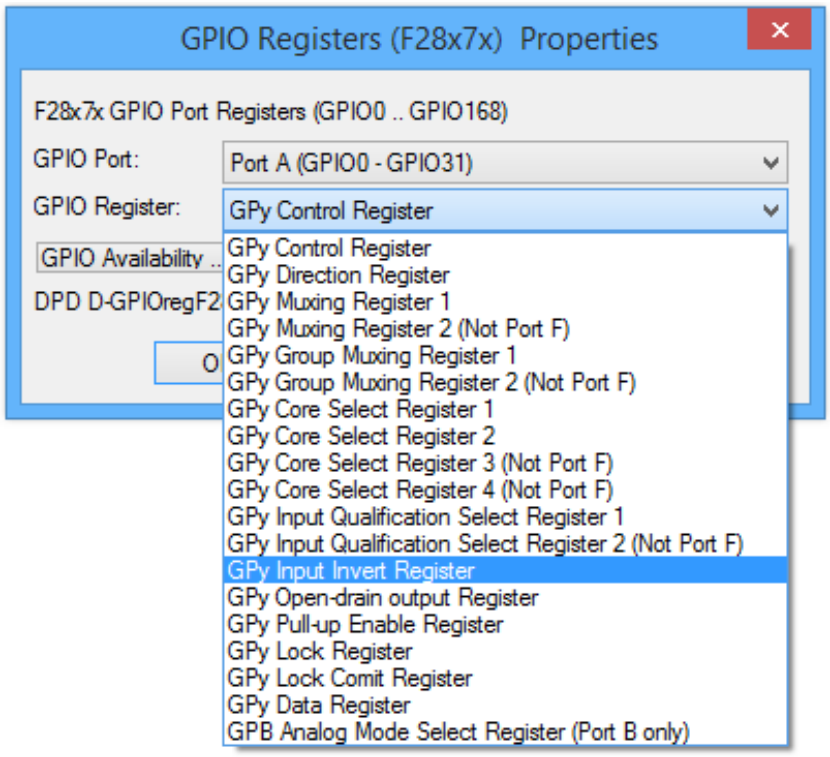


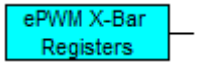


GPIO Registers (F28x7x)

GPIO register selection for F28x7x.

Output pin: Selected Register.

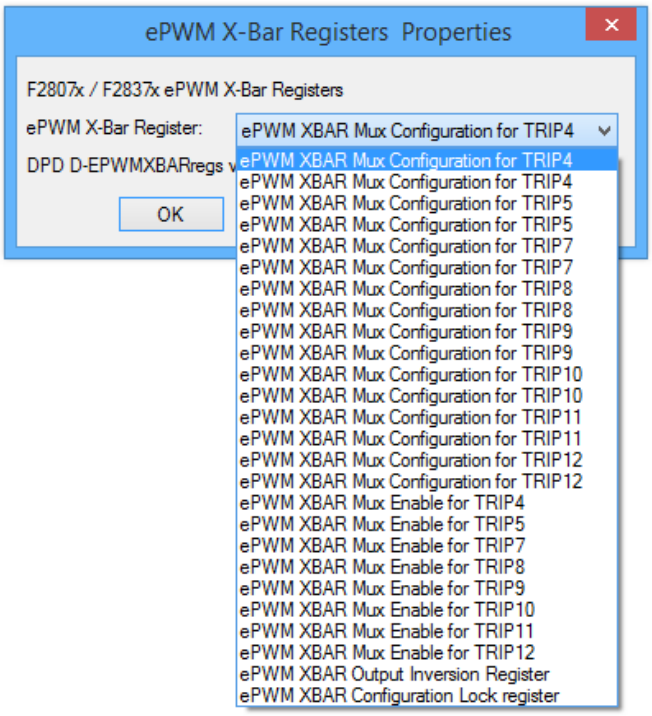


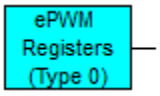


ePWM X-Bar Registers

EPWM X-bar register selection.

Output pin: Selected Register.

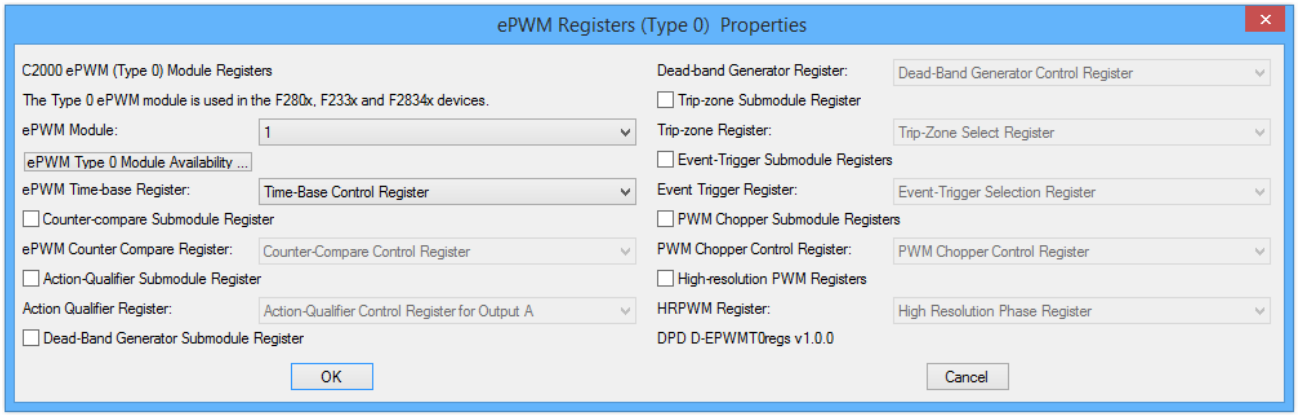


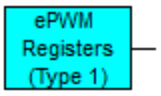


ePWM Registers (Type 0)

EPWM type 0 register selection.

Output pin: Selected Register.

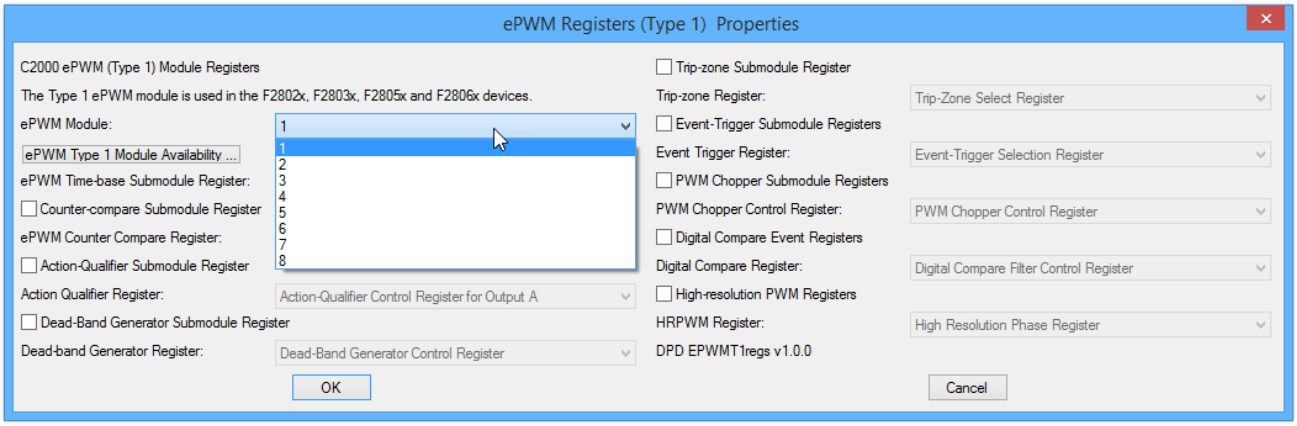


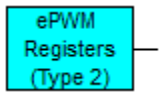


ePWM Registers (Type 1)

EPWM type 1 register selection.

Output pin: Selected Register.

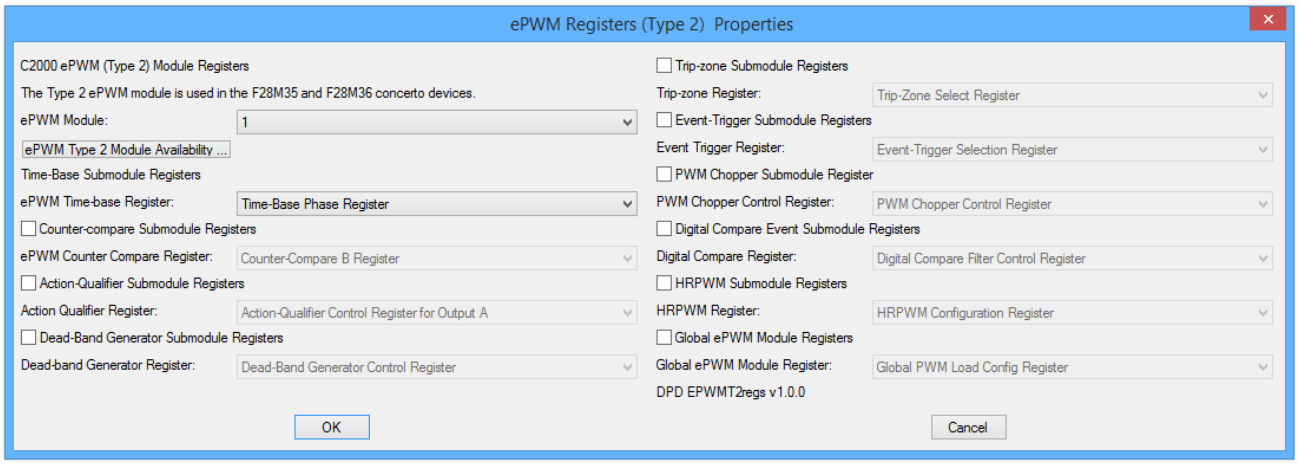


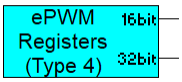


ePWM Registers (Type 2)

EPWM type 2 register selection.

Output pin: Selected Register.





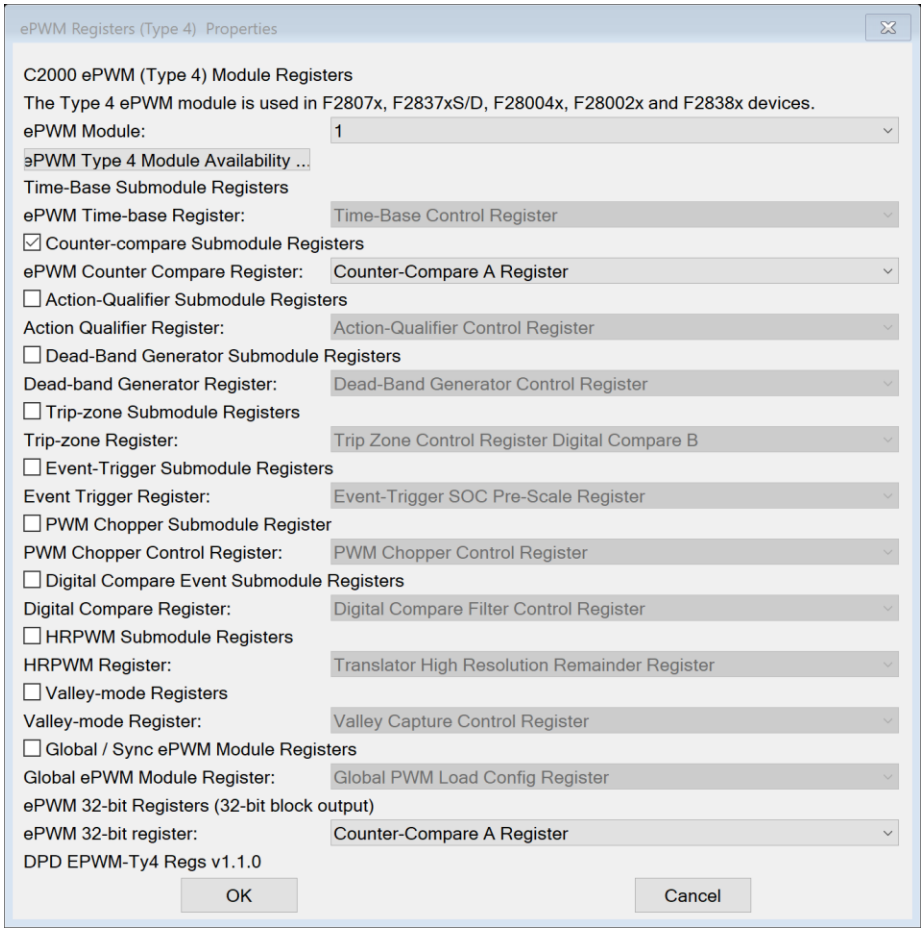
ePWM Registers (Type 4)

EPWM type 4/5 register selection.

Output pin:

Selected Register (16bit).

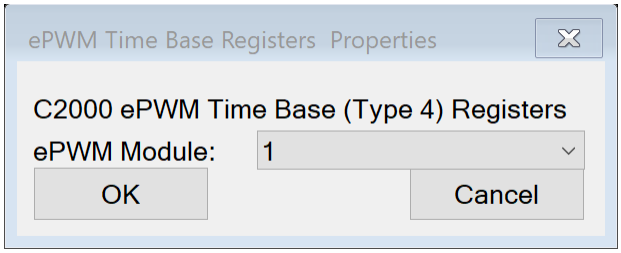
Selected Register (32bit).

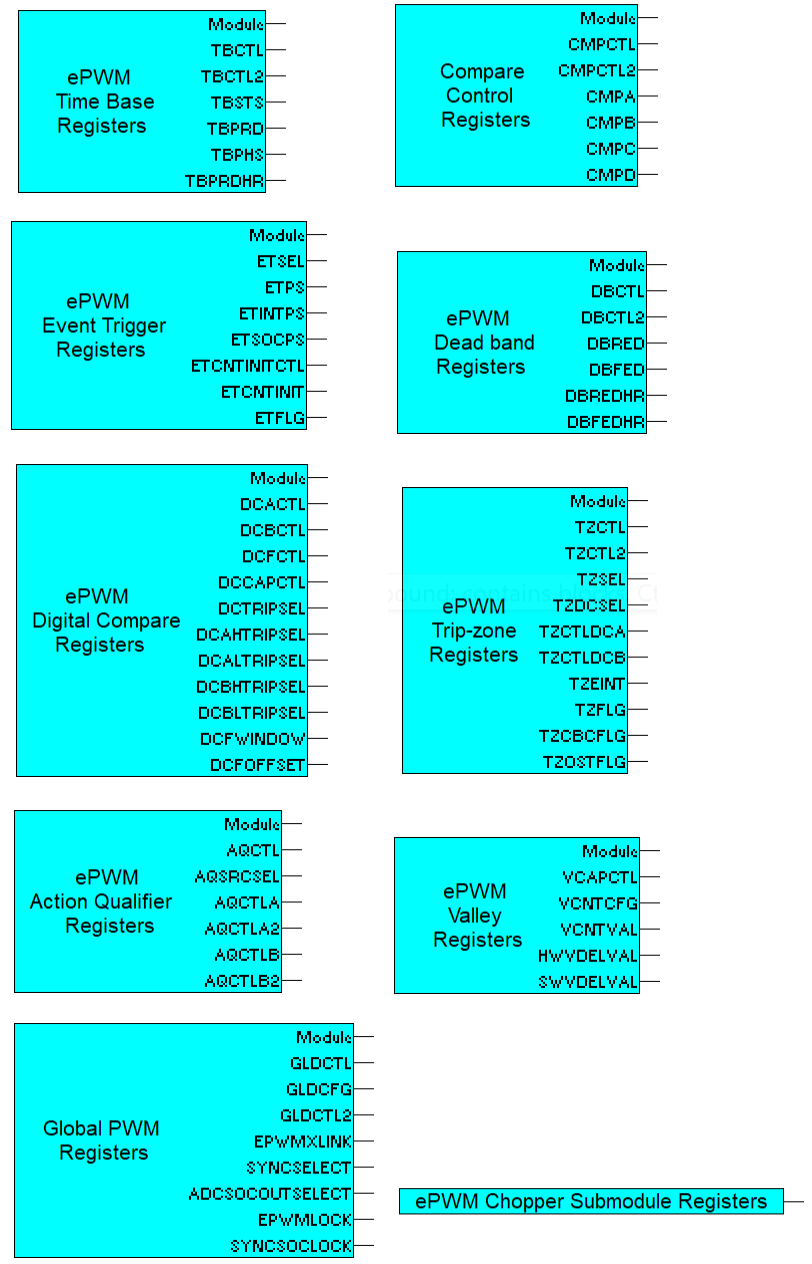


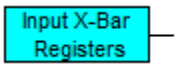
ePWM submodule Registers

EPWM registers grouped into the submodules.

Output pins: All of the submodule registers.



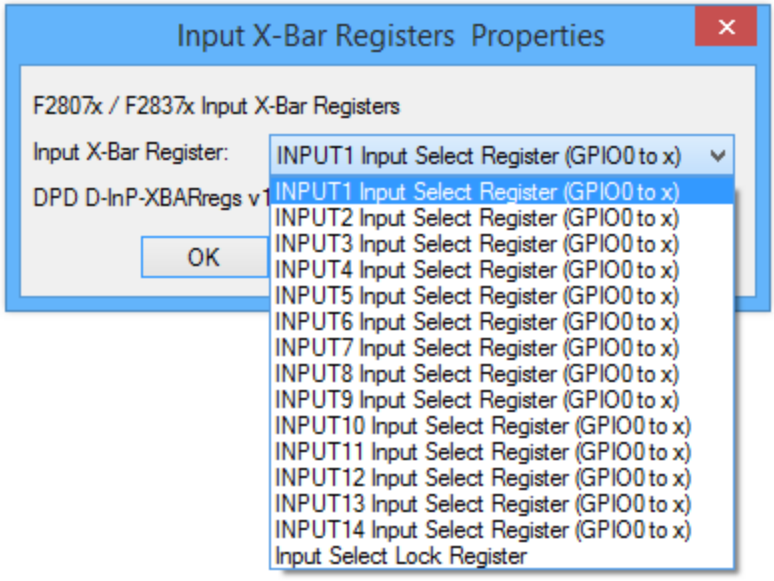




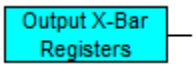
Input X-Bar Registers

Input X-bar register selection.

Output pin: Selected Register.



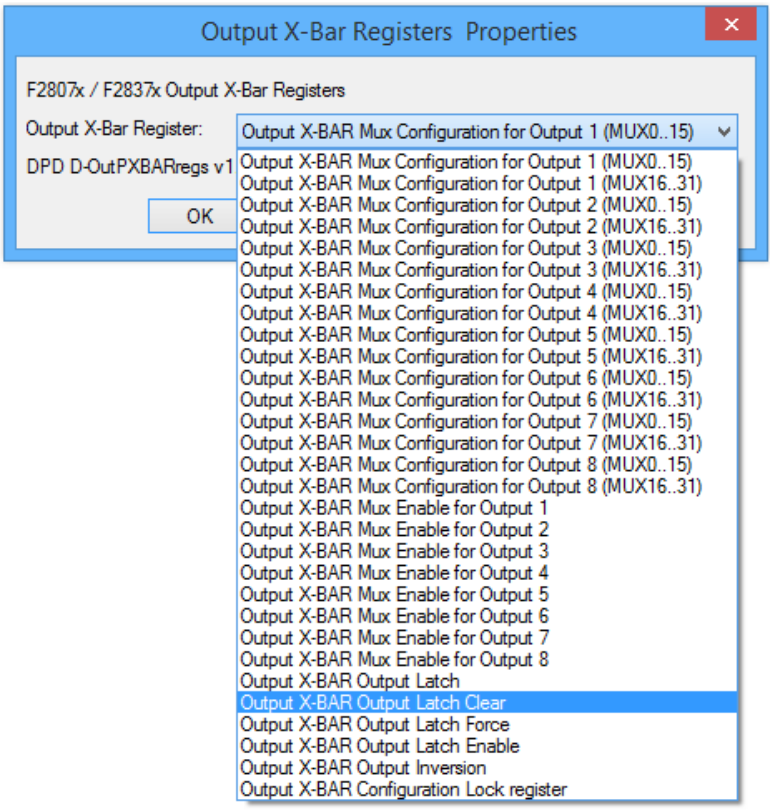
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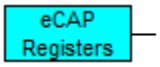


Output X-Bar Registers

Output X-bar register selection.

Output pin: Selected Register.

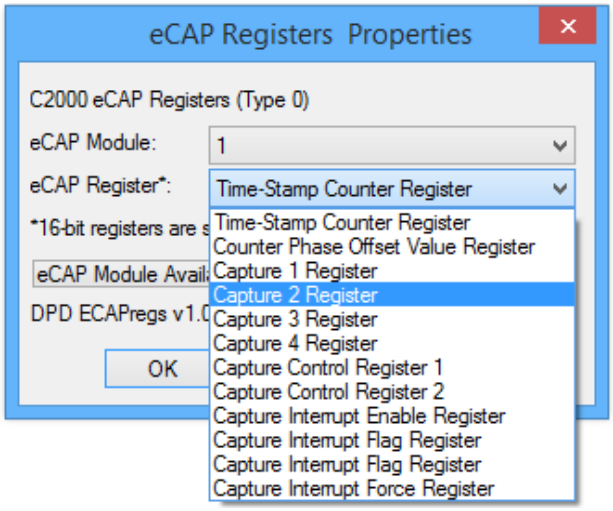


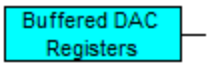


eCAP Registers

eCAP register selection.

Output pin: Selected Register.

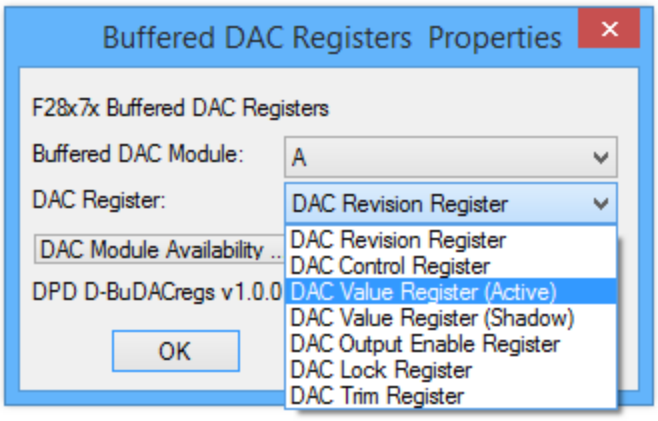




Buffered-DAC Registers

Buffered DAC register selection.

Output pin: Selected Register.

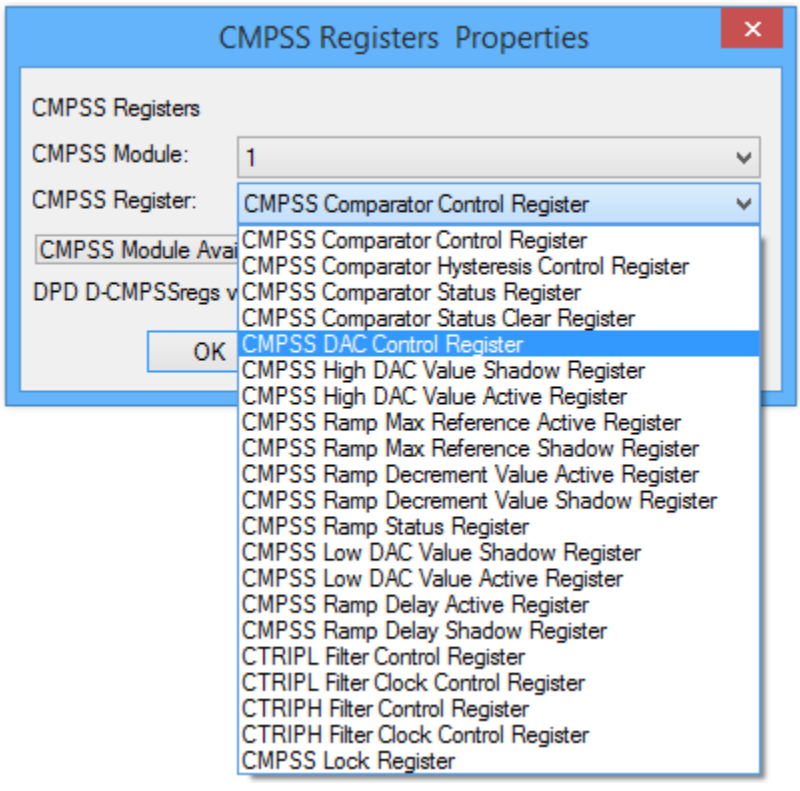




CMPSS Registers

CMPSS register selection.

Output pin: Selected Register.

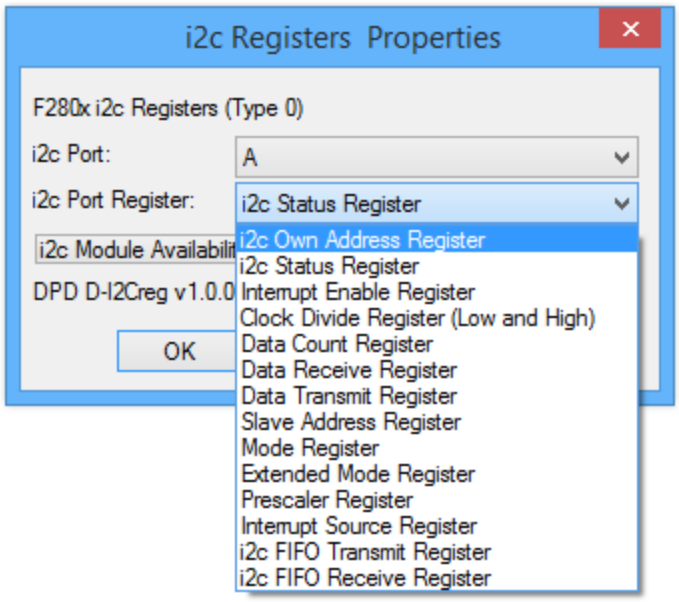




i2c Registers

i2c peripheral register selection.

Output pin: Selected Register.

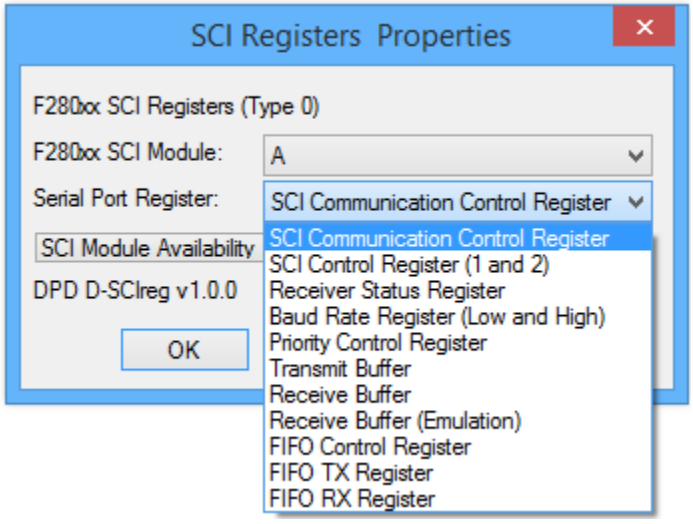


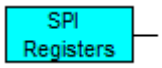


SCI Registers

Serial communication interface (SCI) peripheral register selection.

Output pin: Selected Register.

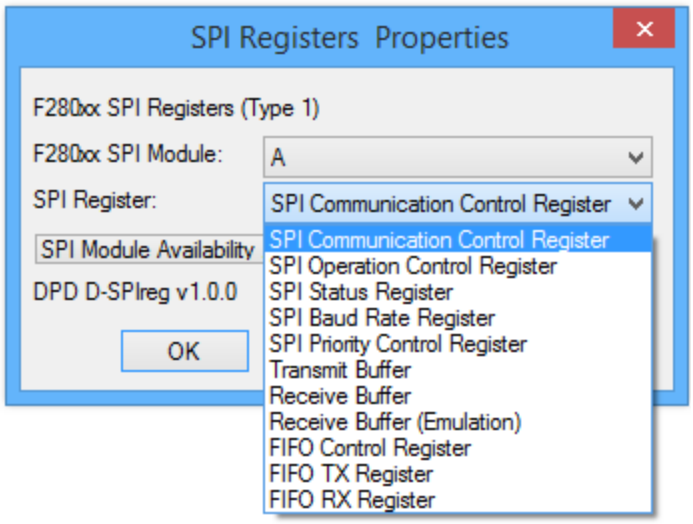




SPI Registers

Serial peripheral Interface (SPI) peripheral register selection.

Output pin: Selected Register.

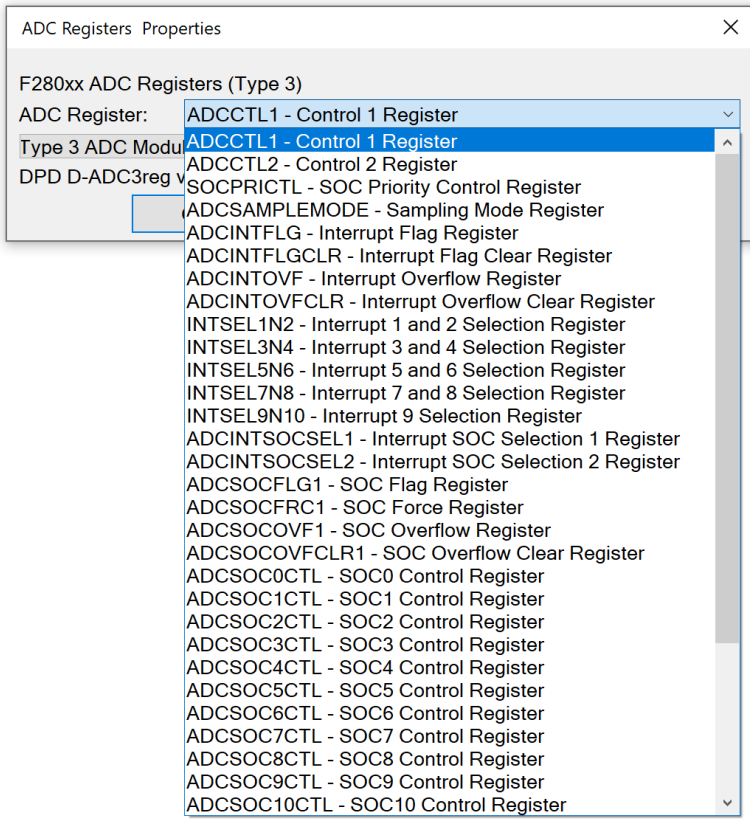




ADC Registers (Type 3)

ADC control register selection for the type 3 ADC (piccolo F280x, Concerto).

Output pin: Selected Register.

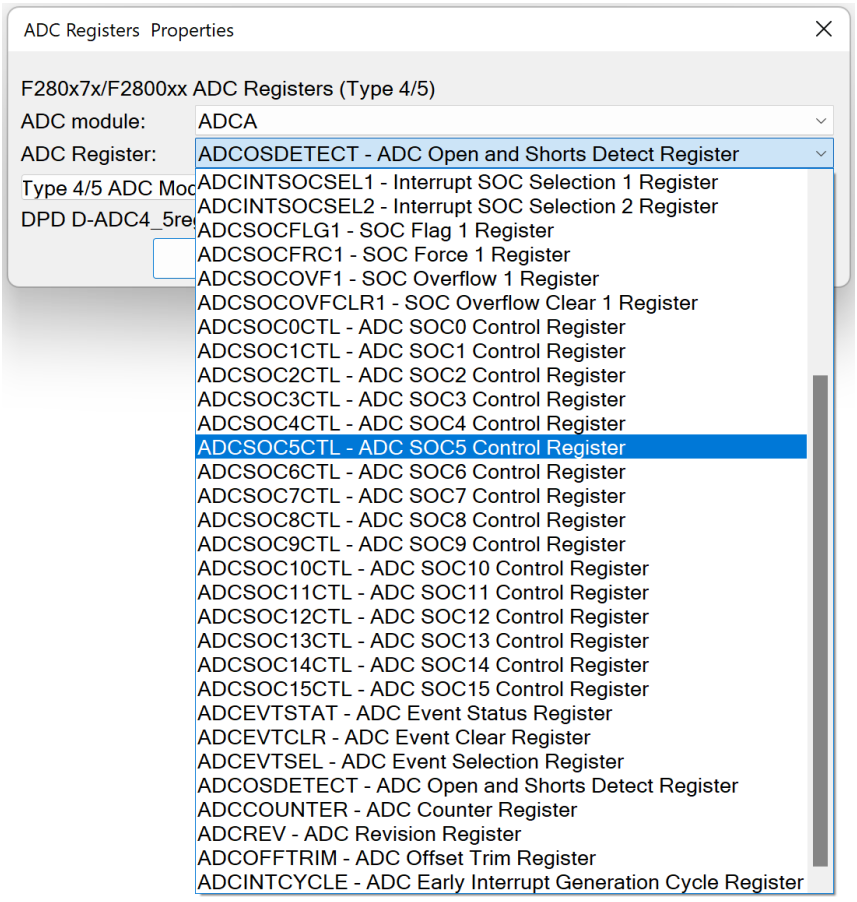


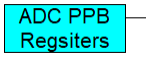


ADC Registers (Type 4/5)

ADC control register selection for the ADC types 4 and 5 (F2807x, F2837x, F2804x, F2802x).

Output pin: Selected Register.

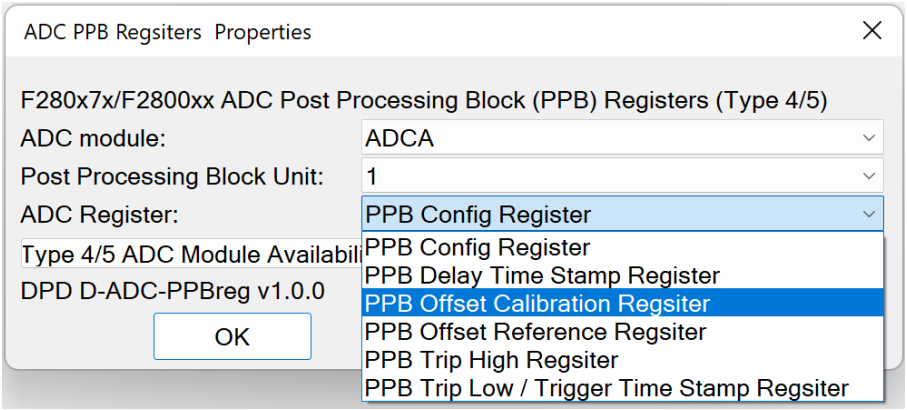


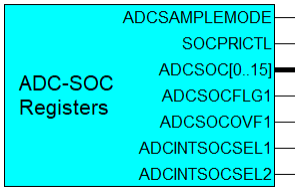


ADC PPB Registers (Types 4/5)

ADC post processing block (PPB) registers selection.

Output pin: Selected Register.





ADC SOC Registers (Type 3)

ADC Start of Conversion (SOC) registers compatible with the debug block.

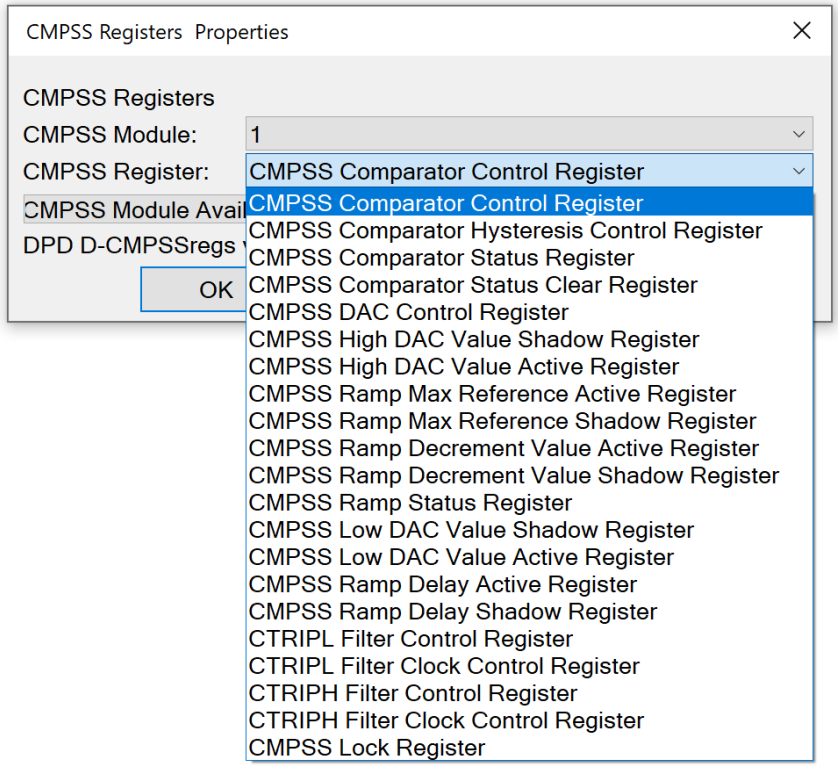
Output pins: Selected Registers.



CMPSS Registers

Comparator sub-system CMPSS control register selection.

Output pin: Selected Register.

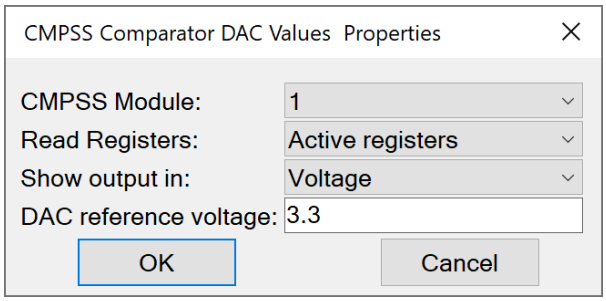




CMPSS comparator DAC values

Comparator sub-system CMPSS DAC value visualization.

Output pin: Current DACH and DACL values.



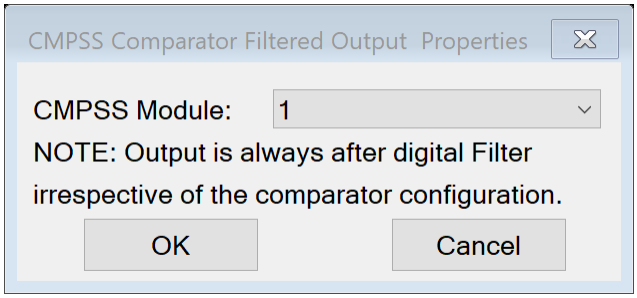
Contents - Debug

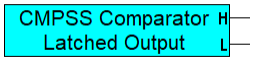


CMPSS comparator Filtered output

Comparator sub-system CMPSS filtered comparator output visualization.

Output pins: Current filtered outputs.

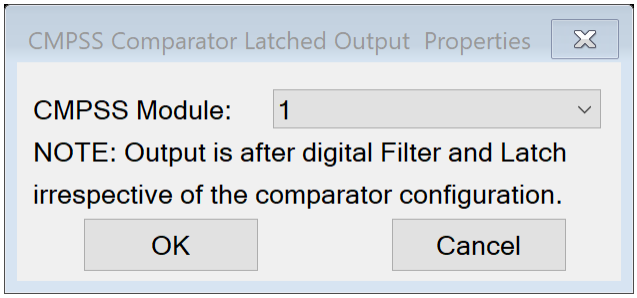


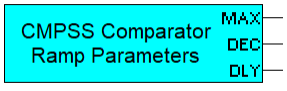


CMPSS comparator Latched output

Comparator sub-system CMPSS latched comparator output visualization.

Output pins: Current latched outputs.

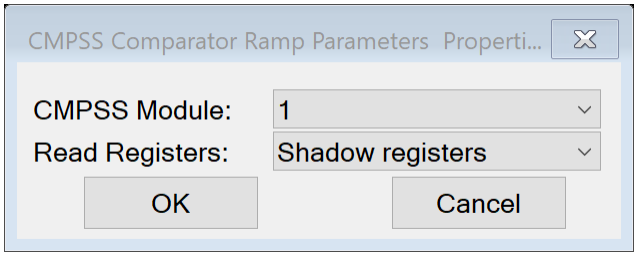




CMPSS comparator Ramp Parameters

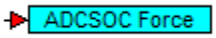
Comparator sub-system CMPSS ramp parameters visualization.

Output pins: Ramp parameters.



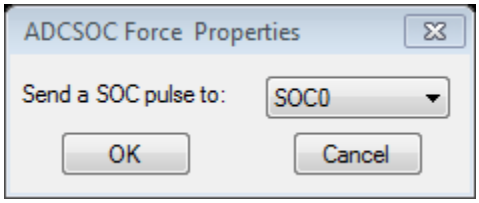
Control (Codegen)

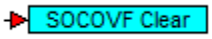
This section contains blocks for performing debugging and / or control actions for various peripherals on the MCU.



ADCSOC Force

Use to force an ADC start of conversion (SOC) via software.





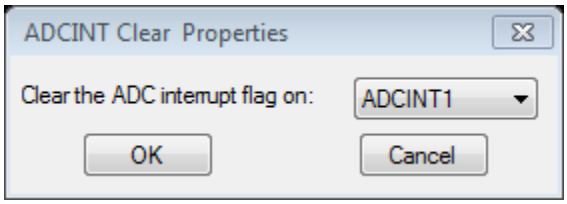
SOCOVF Clear

Use to clear the ADC SOC overflow flag.



ADCINT Force

Use to reset the ADC interrupt.





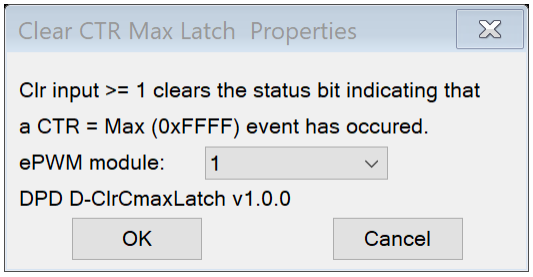
ADCINTOVF Clear

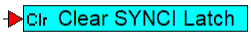
Use to reset the ADC interrupt overflow flag.



EPWM Clear CTR=Max Latch

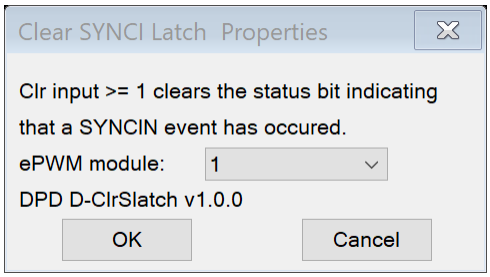
Use to reset the PWM counter = max flag.





EPWM Sync Event Clear Latch

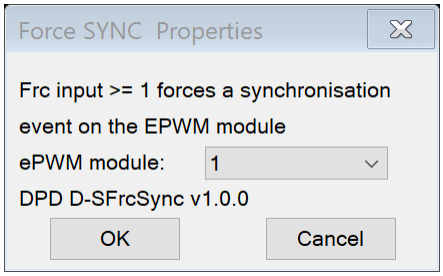
Use to reset the PWM sync event flag.





EPWM Force Sync

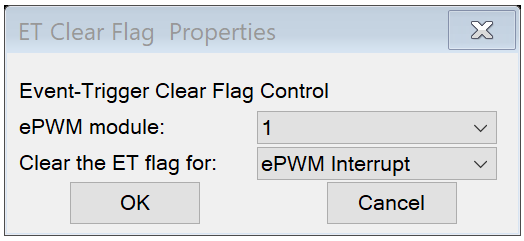
Use to force a PWM sync event via software.

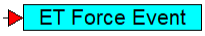




EPWM ET Clear Flag

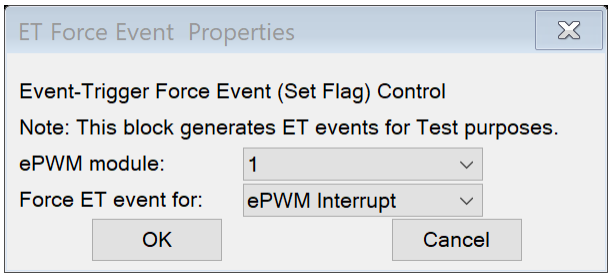
Use to clear a PWM event trigger flag (a PWM interrupt flag or a SOCA or SOC flag).





EPWM ET Force Event

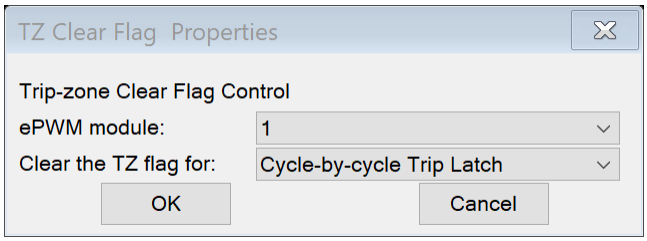
Use to software force a PWM event trigger (a PWM interrupt flag or a SOCA or SOC flag).



TZ Clear Flag

EPWM TZ Clear Flag

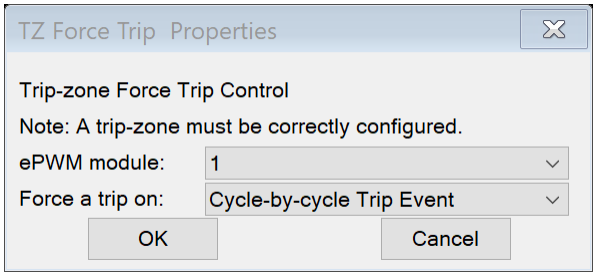
Use to reset the trip-zone flag event.



TZ Force Trip

EPWM TZ Force Trip

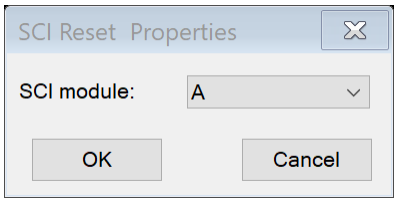
Use to force a trip on the selected EPWM module (if configured).



SCI Reset

SCI Reset

Use to reset the internally set SCI module.



SCI Reset Rx Pointer

SCI Reset Rx Pointer

Use to reset the Rx FIFO pointer of the internally set SCI module.

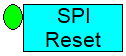
Note: This is a reset of the hardware FIFO pointer and does not reset the queue if an interrupt queue is used. The software queue must be read completely out in order to reset it to zero.

SCI Reset Tx Pointer

SCI Reset Tx Pointer

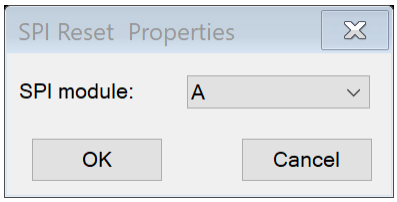
Use to reset the Tx FIFO pointer of the internally set SCI module.

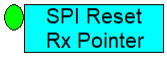
Note: This is a reset of the hardware FIFO pointer and does not reset the queue if an interrupt queue is used. The software queue must be written completely out in order to reset it to zero.



SPI Reset

Use to reset the internally set SPI module.

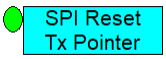




SPI Reset Rx Pointer

Use to reset the Rx FIFO pointer of the internally set SPI module.

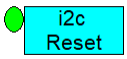
Note: This is a reset of the hardware FIFO pointer and does not reset the queue if an interrupt queue is used. The software queue must be read completely out in order to reset it to zero.



SPI Reset Tx Pointer

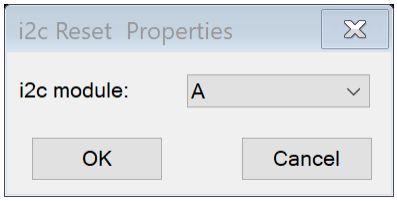
Use to reset the Tx FIFO pointer of the internally set SPI module.

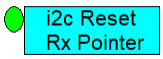
Note: This is a reset of the hardware FIFO pointer and does not reset the queue if an interrupt queue is used. The software queue must be written completely out in order to reset it to zero.



i2c Reset

Use to reset the internally set i2c module.

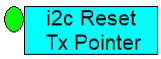




i2c Reset Rx Pointer

Use to reset the Rx FIFO pointer of the internally set i2c module.

Note: This is a reset of the hardware FIFO pointer and does not reset the queue if an interrupt queue is used. The software queue must be read completely out in order to reset it to zero.



i2c Reset Tx Pointer

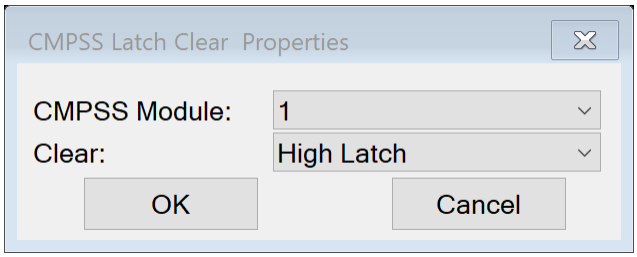
Use to reset the Tx FIFO pointer of the internally set i2c module.

Note: This is a reset of the hardware FIFO pointer and does not reset the queue if an interrupt queue is used. The software queue must be written completely out in order to reset it to zero.



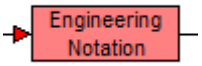
CMPSS Latch Clear

Use to clear the comparator output latch (if enabled).



Contents - Debug

Displays



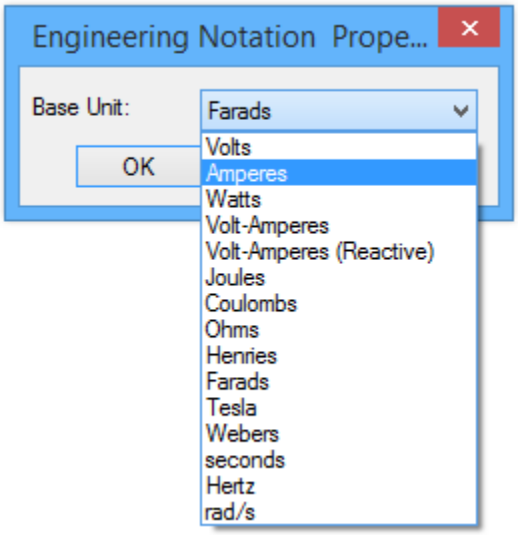
Engineering Notation

The Engineering Notation block converts any electrical input value into a more readable notation by adding SI prefixes at each magnitude of one thousand.

Input Pin: Input signal.

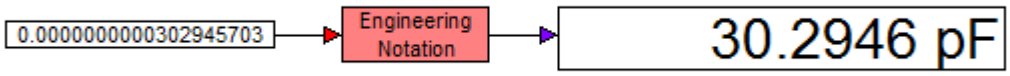
Output Pin: Output value expressed in SI units with the appropriate engineering prefix

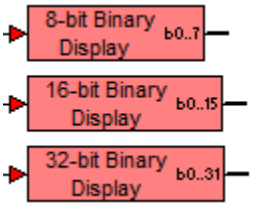
Dialog properties:



Base Unit:

An electrical unit can be selected in order for it to be displayed with the appropriate SI prefix at the output of the block.





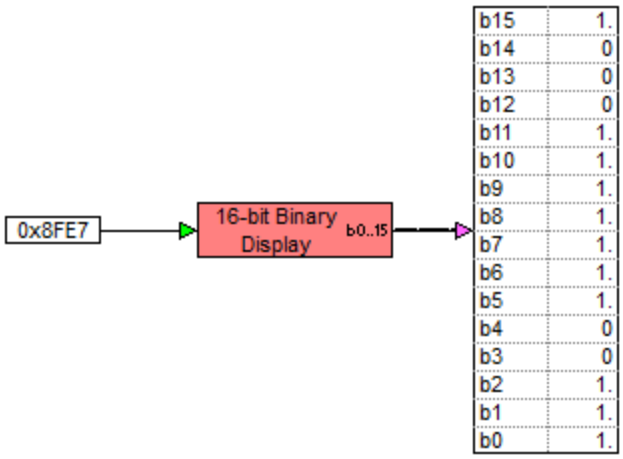
Binary Displays

These blocks can be connected to a display block in order to view the input value in binary format.

Input Pins: Input signal.

Output Pins: Output in binary format (struct).

An example is given below for the 16-bit display.

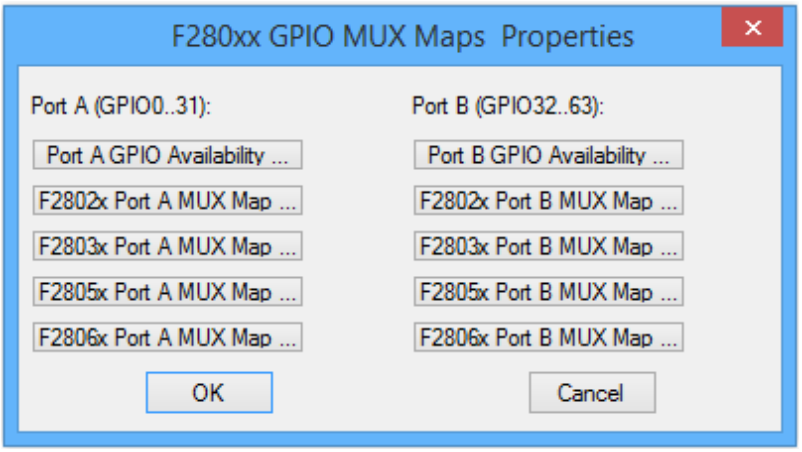


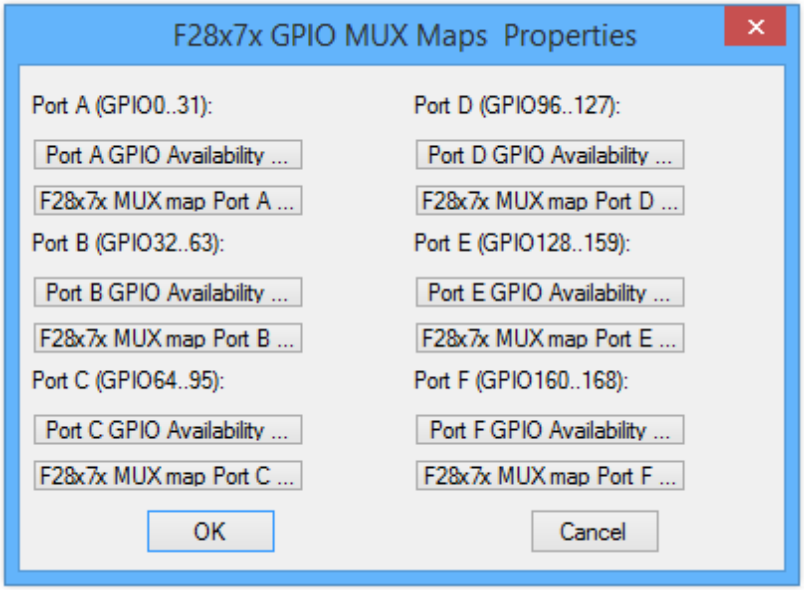
F280xx GPIO MUX Maps

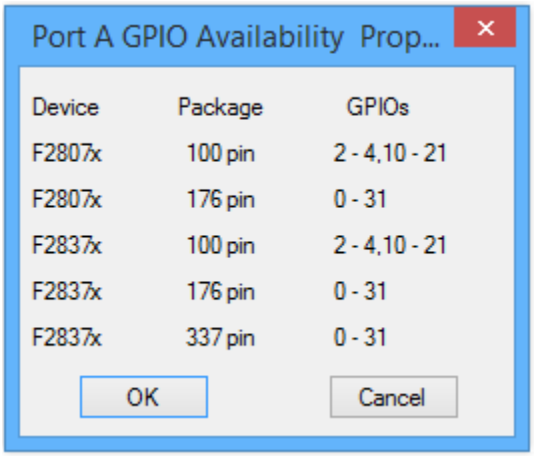
F28x7x GPIO MUX Maps

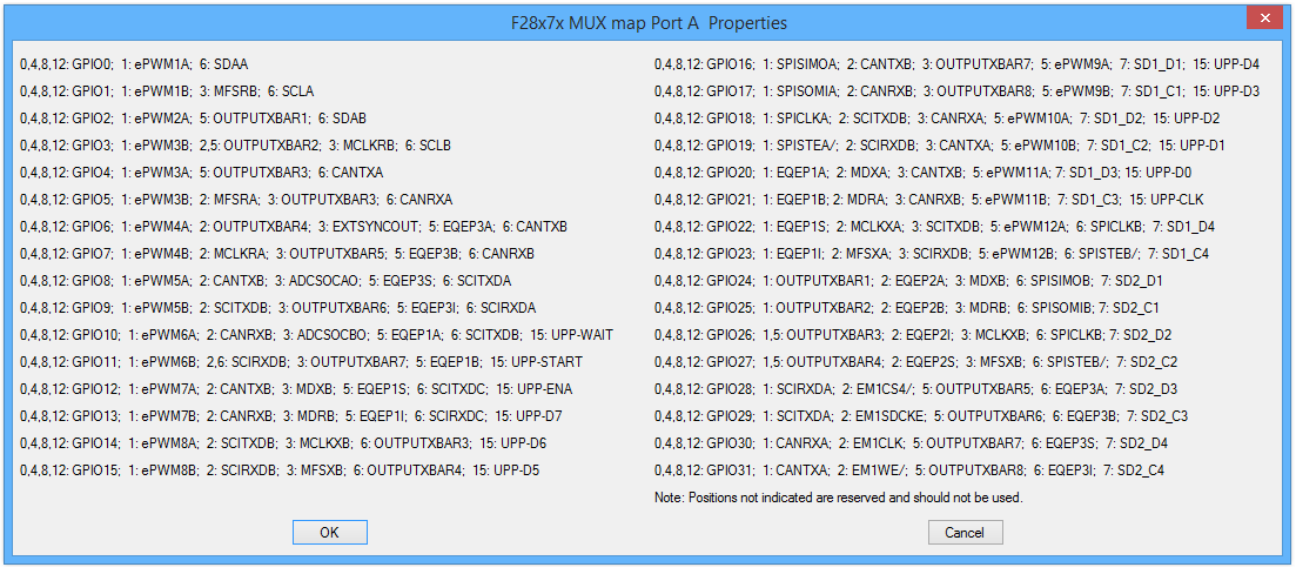
GPIO MUX Maps

These blocks allows one to view the TI C2000 GPIO availability and Muxing for each device as shown in the example dialog properties below.

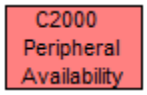






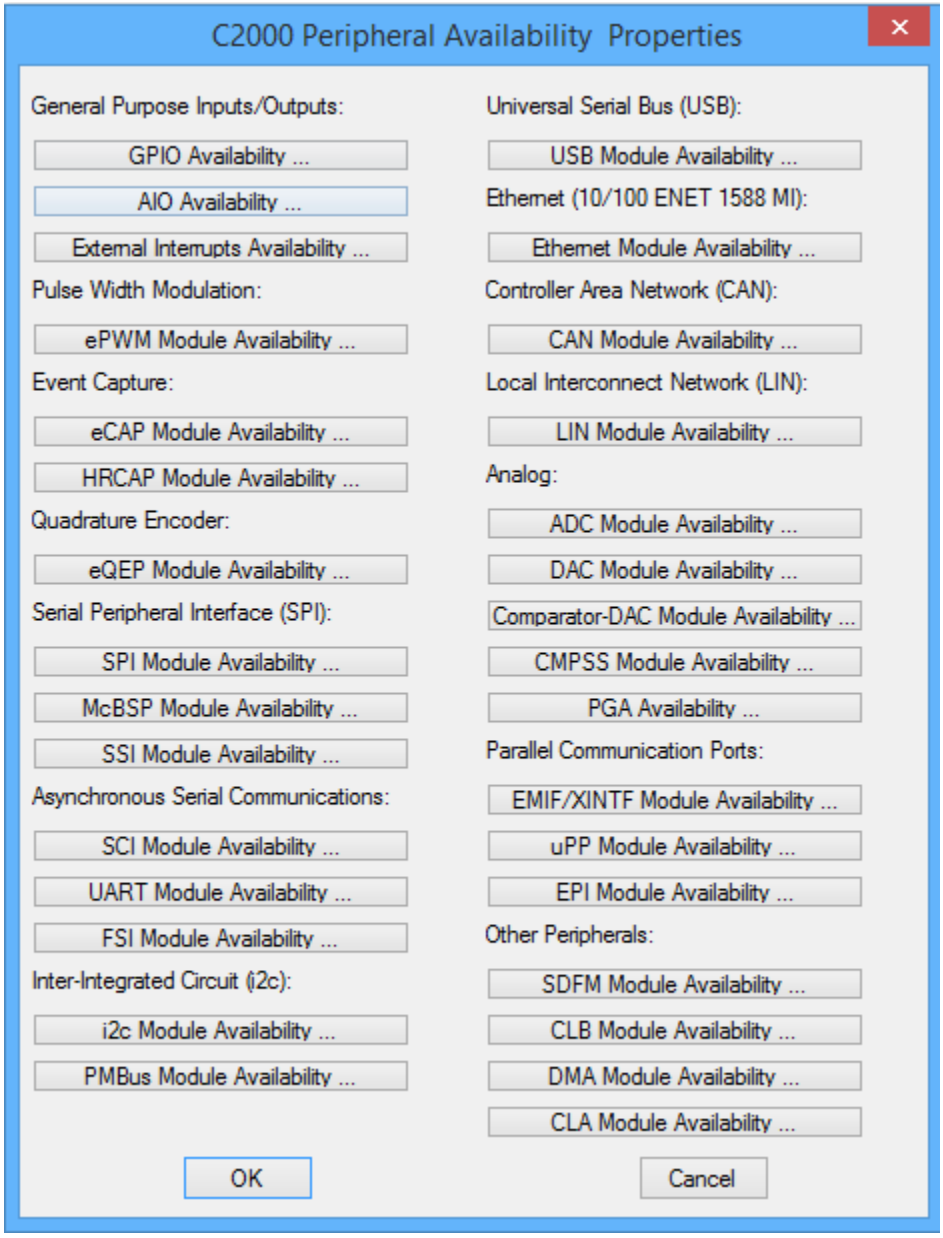


Contents - Debug

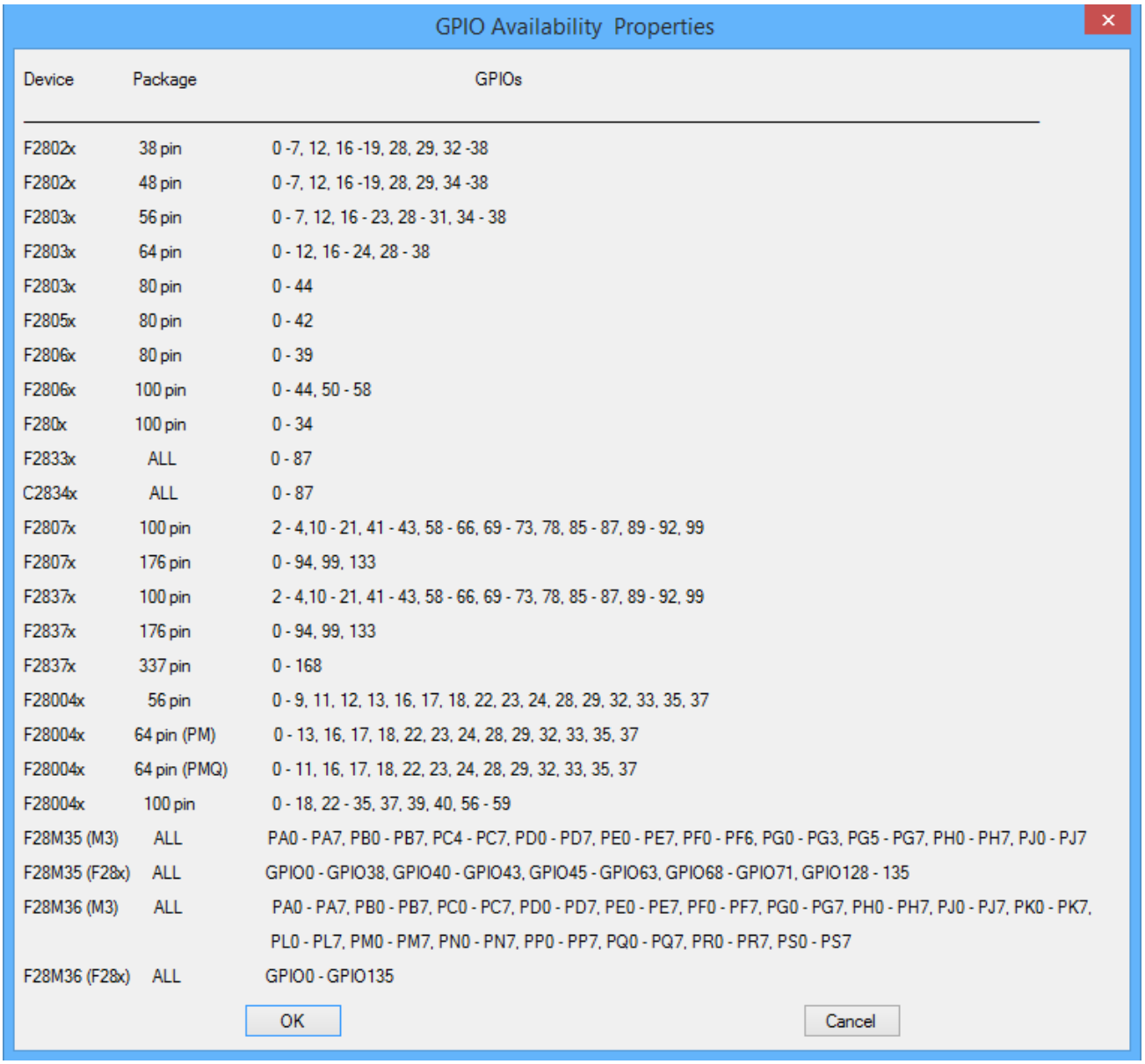


Peripheral Availability

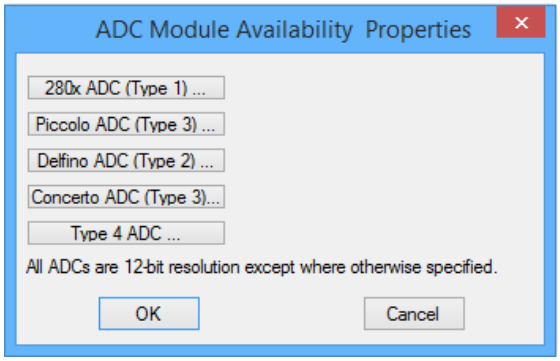
This block allows one to view the availability on each TI C2000 device, many of the peripherals used in digital power and other applications.



GPIO availability in C2000 devices:



ADC peripheral availability in C2000 devices:



Piccolo ADC (Type 3) Properties

Device	Package	ADC No.	Input No.	Channels	S/H	Min. S/H Width (clks)	Conversion Time (ns)
F28020/1	38 pin	1	7	A0***, A2, A4, A6, B2, B4, B6	Dual	14	500
F28020/1	48 pin	1	13	A0***-A4, A6, A7, B1-B4, B6, B7	Dual	14	500
F28022/3	38 pin	1	7	A0***, A2, A4, A6, B2, B4, B6	Dual	7	260
F28022/3	48 pin	1	13	A0***-A4, A6, A7, B1-B4, B6, B7	Dual	7	260
F28026/7	38 pin	1	7	A0***, A2, A4, A6, B2, B4, B6	Dual	7	216.67
F28026/7	48 pin	1	13	A0***-A4, A6, A7, B1-B4, B6, B7	Dual	7	216.67
F28030/1	56 pin	1	13	A0-A4, A6, A7, B1-B4, B6, B7	Dual	24	500
F28030/1	64 pin	1	14	A0-A4, A6, A7, B0-B4, B6, B7	Dual	24	500
F28030/1	80 pin	1	16	A0-A7*, B0-B7**	Dual	24	500
F28032-5	56 pin	1	13	A0-A4, A6, A7, B1-B4, B6, B7	Dual	7	216.67
F28032-5	64 pin	1	14	A0-A4, A6, A7, B0-B4, B6, B7	Dual	7	216.67
F28032-5	80 pin	1	16	A0-A7*, B0-B7**	Dual	7	216.67
F28050/1	80 pin	1	16	A0-A7*, B0-B7**	Dual	24	500
F28052-4	80 pin	1	16	A0-A7*, B0-B7**	Dual	10*****	267
F2806x	80 pin	1	12	A0-A2, A4-A6, B0-B2, B4-B6	Dual	7	289
F2806x	100 pin	1	16	A0-A7*, B0-B7**	Dual	7	289

*A5 shared with internal temp. sensor, **B5 shared internally with VREFLO, ***A0 shared with VREFHI *****Varies with PGA use and overlap mode.

OK Cancel

AIO port availability in C2000 devices:

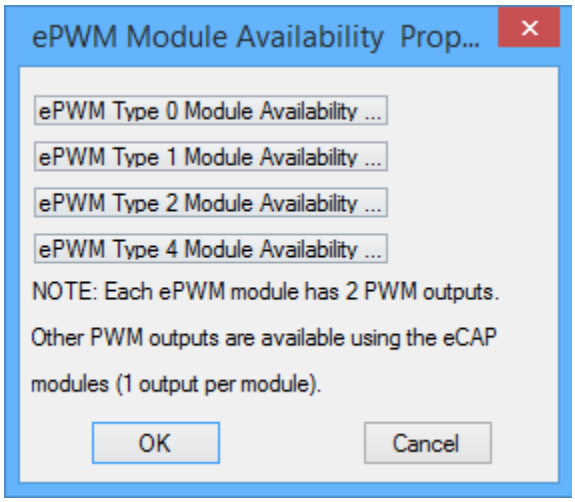
AIO Availability Properties

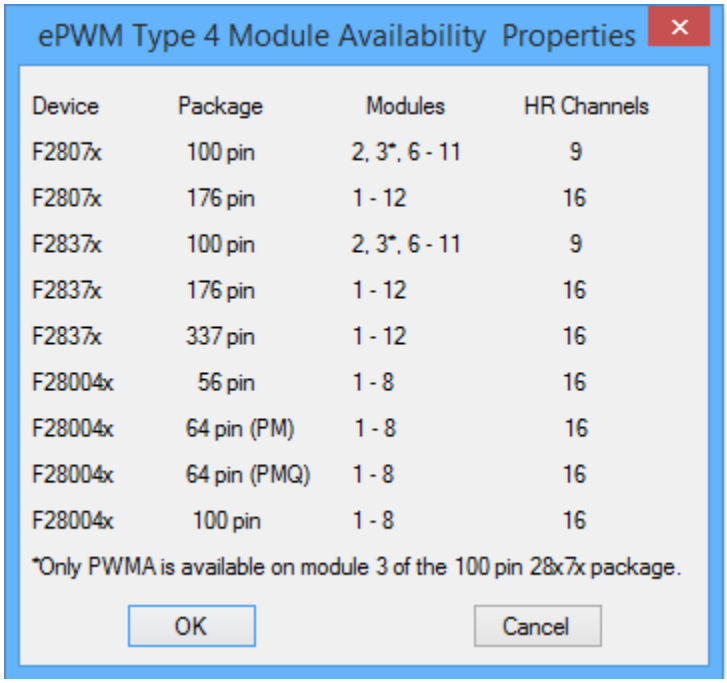
Device	Package	AIO
F2802x	38 pin	2(A2), 4(A4), 6(A6), 10(B2), 12(B4), 14(B6)
F2802x	48 pin	2(A2), 4(A4), 6(A6), 10(B2), 12(B4), 14(B6)
F2803x	56 pin	2(A2), 4(A4), 6(A6), 10(B2), 12(B4), 14(B6)
F2803x	64 pin	2(A2), 4(A4), 6(A6), 10(B2), 12(B4), 14(B6)
F2803x	80 pin	2(A2), 4(A4), 6(A6), 10(B2), 12(B4), 14(B6)
F2806x	80 pin	2(A2), 4(A4), 6(A6), 10(B2), 12(B4), 14(B6)
F2806x	100 pin	2(A2), 4(A4), 6(A6), 10(B2), 12(B4), 14(B6)
F28004x*	56 pin	224 - 227, 230 - 232, 237, 238, 242, 244, 245
F28004x*	64 pin	224 - 228, 230 - 232, 237 - 239, 242, 244, 245
F28004x*	100 pin	224 - 234, 236 - 242, 244 - 246
F28M35	ALL	2, 4, 6, 12, 18, 20, 22, 28
F28M36	ALL	2, 4, 6, 10, 12, 14, 18, 20, 22, 26, 28, 30

*F28004x are digital inputs only

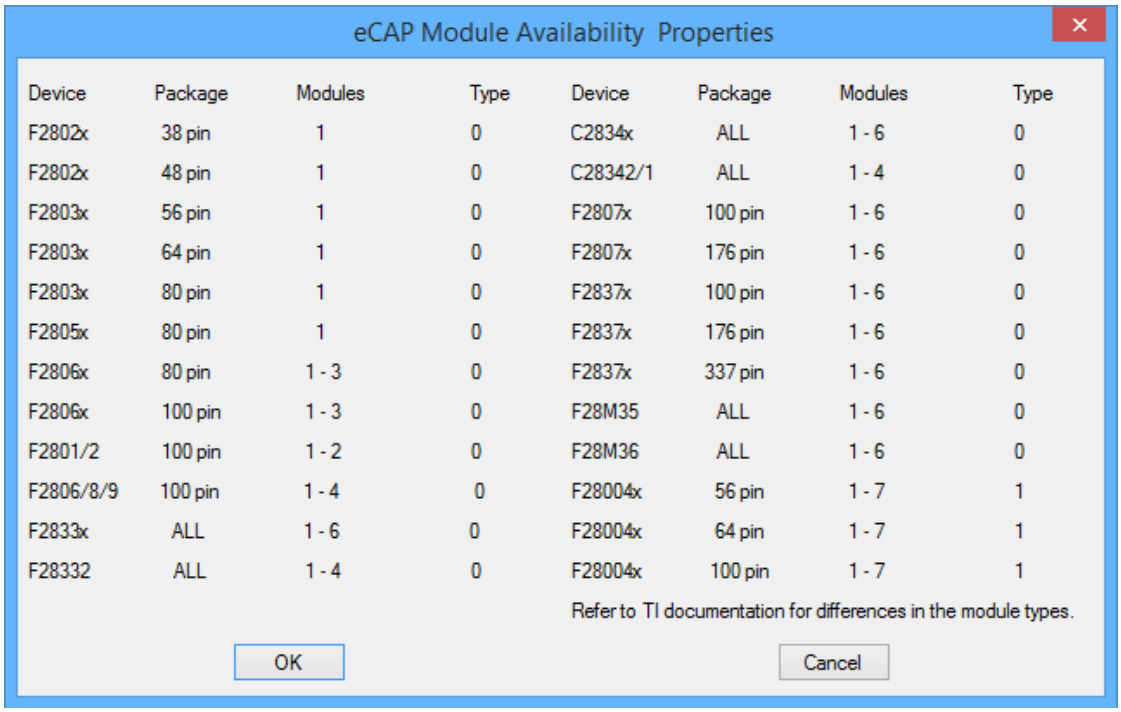
OK Cancel

ePWM peripheral availability in C2000 devices:





eCAP peripheral availability in C2000 devices:



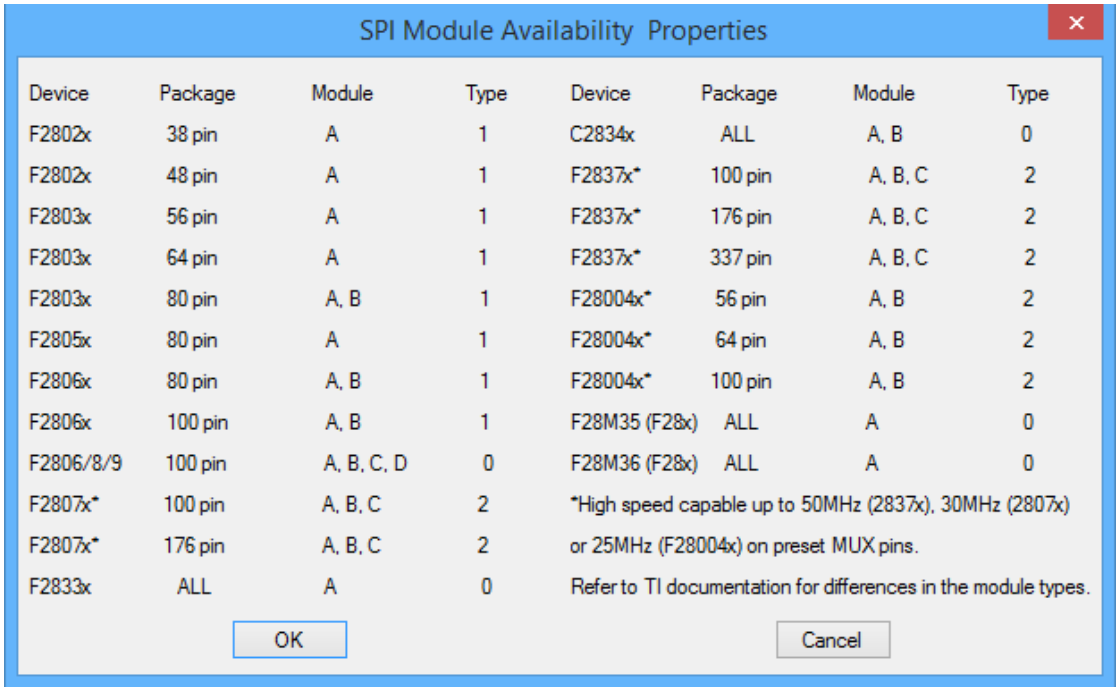
eCAP Module Availability Properties

Device	Package	Modules	Type	Device	Package	Modules	Type
F2802x	38 pin	1	0	C2834x	ALL	1 - 6	0
F2802x	48 pin	1	0	C28342/1	ALL	1 - 4	0
F2803x	56 pin	1	0	F2807x	100 pin	1 - 6	0
F2803x	64 pin	1	0	F2807x	176 pin	1 - 6	0
F2803x	80 pin	1	0	F2837x	100 pin	1 - 6	0
F2805x	80 pin	1	0	F2837x	176 pin	1 - 6	0
F2806x	80 pin	1 - 3	0	F2837x	337 pin	1 - 6	0
F2806x	100 pin	1 - 3	0	F28M35	ALL	1 - 6	0
F2801/2	100 pin	1 - 2	0	F28M36	ALL	1 - 6	0
F2806/8/9	100 pin	1 - 4	0	F28004x	56 pin	1 - 7	1
F2833x	ALL	1 - 6	0	F28004x	64 pin	1 - 7	1
F28332	ALL	1 - 4	0	F28004x	100 pin	1 - 7	1

Refer to TI documentation for differences in the module types.

OK Cancel

SPI peripheral availability in C2000 devices:



SPI Module Availability Properties

Device	Package	Module	Type	Device	Package	Module	Type
F2802x	38 pin	A	1	C2834x	ALL	A, B	0
F2802x	48 pin	A	1	F2837x*	100 pin	A, B, C	2
F2803x	56 pin	A	1	F2837x*	176 pin	A, B, C	2
F2803x	64 pin	A	1	F2837x*	337 pin	A, B, C	2
F2803x	80 pin	A, B	1	F28004x*	56 pin	A, B	2
F2805x	80 pin	A	1	F28004x*	64 pin	A, B	2
F2806x	80 pin	A, B	1	F28004x*	100 pin	A, B	2
F2806x	100 pin	A, B	1	F28M35 (F28x)	ALL	A	0
F2806/8/9	100 pin	A, B, C, D	0	F28M36 (F28x)	ALL	A	0
F2807x*	100 pin	A, B, C	2				
F2807x*	176 pin	A, B, C	2				
F2833x	ALL	A	0				

*High speed capable up to 50MHz (2837x), 30MHz (2807x) or 25MHz (F28004x) on preset MUX pins.

Refer to TI documentation for differences in the module types.

OK Cancel

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